MN4076B/MN4076BS

4-Bit D-Type Register

■ Outline

The MN4076B/S is a 3-state output register consisting of four D-type flip-flops, and controlled by the common clock input and reset input.

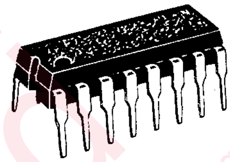
When the levels of the data enable inputs ($\overline{ED}_1$, $\overline{ED}_1$) are both "L", the data inputs (D_0~D_3) are stored in the four flip-flops are the rise of the clock input. In any other combination of the data enable input level conditions, the four flip-flops hold the previous state even if the clock input rose.

When the levels of the output enable inputs $\overline{EO}_0$, $\overline{EO}_1$) are both "L", the outputs of the respective flip-flops appear on the outputs O_0~O_3.

In any other combination of the output enable input level conditions, the respective output becomes high impedance.

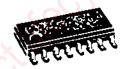
At the reset time, each outpt is asynchronously cleared. This D-type register is equivalent to Motorola's MC14076B and RCA's CD4076B.

P-3



16-pin plastic DIL package

P-4



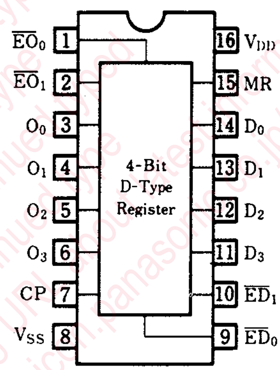
16-pin PANAFLAT package (SO-16D)

■ Truth Table

Input							Output
MR	CP	$\overline{ED}_0$	$\overline{ED}_1$	D_0	$\overline{EO}_0$	$\overline{EO}_1$	$O_{0\,n+1}$
×	×	×	×	×	H	×	Z
×	×	×	×	×	×	H	Z
H	×	×	×	×	L	L	L
L	↑	H	×	×	L	L	no change
L	↑	×	H	×	L	L	no change
L	↑	L	L	H	L	L	H
L	↑	L	L	L	L	L	L
L	↓	×	×	×	L	L	no change
L	×	×	×	×	L	L	no change

Note) × : don't care
2 : high impedance

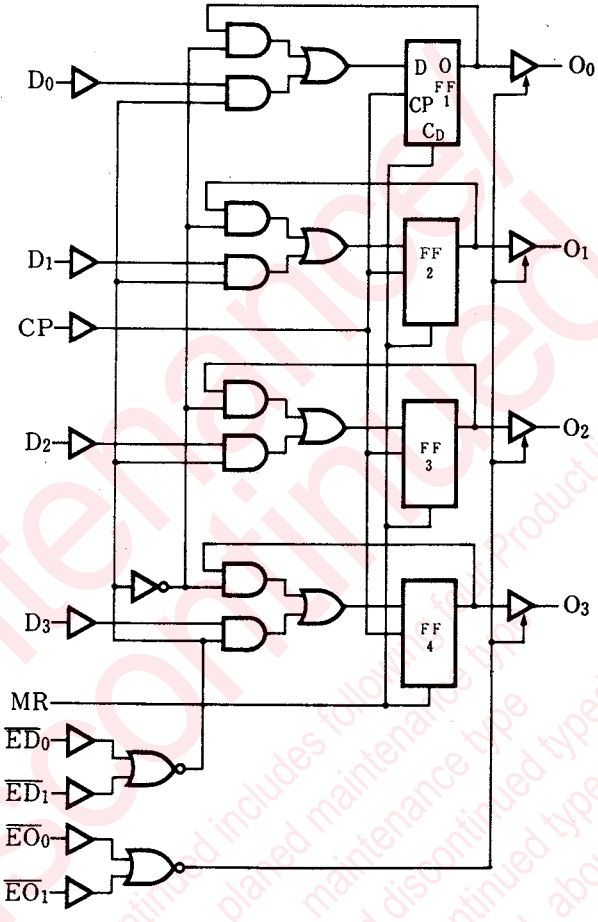
Pin Configuration



Pin description

D_0~D_3 : Data input (4 bits)
$\overline{ED}_0$, $\overline{ED}_1$: Data enable input
$\overline{EO}_0$, $\overline{EO}_1$: Output enable input
CP : Clock input
MR : Reset input
O_0~O_3 : Data output(4 bits)

■ Logic Diagram



■ Absolute Maximum Ratings (Ta=25°C)

Item		Symbol	Rating	Unit
Supply voltage		V_{DD}	−0.5~+18	V
Input voltage		V_I	−0.5~V_{DD}+0.5*	V
Output pin voltage		V_O	−0.5~V_{DD}+0.5*	V
Peak input · output pin current		$\pm I_I$	max. 10	mA
Power dissipation (per package)	Ta=−40~+60°C	P_D	max. 400	mW
	Ta=+60~+80°C		Decrease to 200mW at the rate of 8mW/°C	
Power dissipation (per output pin)		P_D	max. 100	mW
Operating ambient temperature		T_{opr}	−40~+85	°C
Storage temperature		T_{stg}	−65~+150	°C

* V_{DD}+0.5V should be lower than 18V.

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Condition	Ta=−40°C min.	Ta=−40°C max.	Ta=25°C min.	Ta=25°C max.	Ta=85°C min.	Ta=85°C max.	Unit
Static supply current	5	I_{DD}	$V_I=V_{SS}$ or V_{DD}	—	20	—	20	—	150	μA
	10			—	40	—	40	—	300	
	15			—	80	—	80	—	600	
Output voltage low level	5	V_{OL}	$V_I=V_{SS}$ or V_{DD}, $\|I_O\|<1\mu A$	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output voltage high level	5	V_{OH}	$V_I=V_{SS}$ or V_{DD}, $\|I_O\|<1\mu A$	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input voltage low level	5	V_{IL}	$\|I_O\|<1\mu A$, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		$\|I_O\|<1\mu A$, V_O=1V or 9V	—	3	—	3	—	3	
	15		$\|I_O\|<1\mu A$, V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input voltage high level	5	V_{IH}	$\|I_O\|<1\mu A$, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		$\|I_O\|<1\mu A$, V_O=1V or 9V	7	—	7	—	7	—	
	15		$\|I_O\|<1\mu A$, V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output current low level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output current high level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output current high level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input leakage current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA
3-state output pin: Leakage current high level	15	I_{OZH}	$V_O=V_{DD}$	—	1.6	—	1.6	—	12	μA
3-state output pin: Leakage current low level	15	$-I_{OZL}$	$V_O=V_{SS}$	—	1.6	—	1.6	—	12	

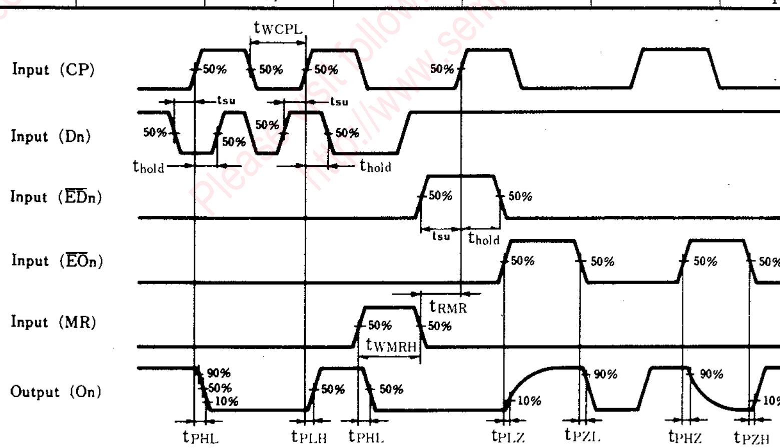
■ Switching Characteristics (Ta=25°C, V_{SS}=0V, C_L=50pF)

Item	V_{DD}(V)	Symbol	min.	typ.	max.	Unit
Output rise time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output fall time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation time CP→On (H→L)	5	t_{PHL}	—	150	450	ns
	10		—	60	180	
	15		—	45	135	
Propagation time CP→On (L→H)	5	t_{PLH}	—	160	480	ns
	10		—	65	195	
	15		—	45	135	
Propagation time MR→On (H→L)	5	t_{PHL}	—	95	285	ns
	10		—	40	120	
	15		—	30	90	

■ Switching Characteristics (cont.)

Item	V_{DD}(V)	Symbol	min.	typ.	max.	Unit
High level output disable time $\overline{EO}n \rightarrow On$ (H)	5	t_{PHZ}	—	50	150	ns
	10		—	35	105	
	15		—	30	90	
Low level output disable time $\overline{EO}n \rightarrow On$ (L)	5	t_{PLZ}	—	45	135	ns
	10		—	30	90	
	15		—	30	90	
High level output enable time $\overline{EO}n \rightarrow On$ (H)	5	t_{PZH}	—	65	195	ns
	10		—	30	90	
	15		—	20	60	
Low level output enable time $\overline{EO}n \rightarrow On$ (L)	5	t_{PZL}	—	60	180	ns
	10		—	25	75	
	15		—	20	60	
Set-up time Dn→CP	5	t_{su}	—	−15	10	ns
	10		—	−10	0	
	15		—	−5	0	
Set-up time $\overline{ED}n \rightarrow CP$	5	t_{su}	—	−50	0	ns
	10		—	−20	0	
	15		—	−15	0	
Hold time Dn→CP	5	t_{hold}	—	30	55	ns
	10		—	10	20	
	15		—	10	15	
Hold time $\overline{ED}n \rightarrow CP$	5	t_{hold}	—	−25	25	ns
	10		—	−10	10	
	15		—	−5	5	
Low level minimum clock pulse width	5	t_{WCPL}	—	60	180	ns
	10		—	20	60	
	15		—	15	45	
High level minimum MR pulse width	5	t_{WMRH}	—	25	75	ns
	10		—	15	45	
	15		—	10	30	
Maximum clock frequency	5	f_{max}	4	8	—	MHz
	10		11	22	—	
	15		16	32	—	
Input capacitance		C_I	—	—	7.5	pF

- Switching waveforms



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