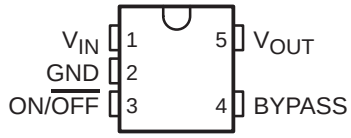
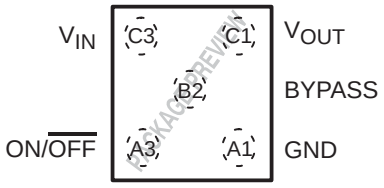
- **Available in the Texas Instruments NanoFree™ Wafer Chip Scale Packages**
- **Output Tolerance of**
  - **1% (A Grade)**
  - **1.5% (Standard Grade)**
- **Ultra-Low Dropout, Typically**
  - **280 mV at Full Load of 150 mA**
  - **7 mV at 1 mA**
- **Wide V_{IN} Range**
  - **16 V Max (DBV Package)**
  - **12 V Max (YZQ/YZU Package)**
- **Low I_Q . . . 850 μA at Full Load at 150 mA**
- **Shutdown Current . . . 0.01 μA Typ**
- **Low Noise . . . 30 μV_{RMS} With 10-nF Bypass Capacitor**
- **Stable With Low-ESR Capacitors, Including Ceramic**
- **Overcurrent and Thermal Protection**
- **High Peak-Current Capability**
- **Portable Applications**
  - **Cellular Phones**
  - **Palmtop and Laptop Computers**
  - **Personal Digital Assistants (PDAs)**
  - **Digital Cameras and Camcorders**
  - **CD Players**
  - **MP3 Players**

DBV (SOT-23) PACKAGE
(TOP VIEW)



YZQ OR YZU (WCSP) PACKAGE
(TOP VIEW)



description/ordering information

The LP2985 family of fixed-output, low-dropout regulators offers exceptional, cost-effective performance for both portable and nonportable applications. Available in voltages of 1.25 V, 1.5 V, 1.8 V, 2.5 V, 2.8 V, 2.85 V, 3 V, 3.1 V, 3.3 V, and 5 V, the family has an output tolerance of 1% for the A version (1.5% for the non-A version) and is capable of delivering 150-mA continuous load current. Standard regulator features, such as overcurrent and overtemperature protection, are included.

The LP2985 has a host of features that makes the regulator an ideal candidate for a variety of portable applications:

- Low dropout: A PNP pass element allows a typical dropout of 280 mV at 150-mA load current and 7 mV at 1-mA load.
- Low quiescent current: The use of a vertical PNP process allows for quiescent currents that are considerably lower than those associated with traditional lateral PNP regulators.
- Shutdown: A shutdown feature is available, allowing the regulator to consume only 0.01 μA when the ON/$\overline{\text{OFF}}$ pin is pulled low.
- Low-ESR-capacitor friendly: The regulator is stable with low-ESR capacitors, allowing the use of small, inexpensive, ceramic capacitors in cost-sensitive applications.
- Low noise: A BYPASS pin allows for low-noise operation, with a typical output noise of 30 μV (RMS), with the use of a 10-nF bypass capacitor.
- Small packaging: For the most space-constraint needs, the regulator is available in SOT-23 package, as well as NanoFree™ wafer chip scale packaging, offering an even smaller size with improved thermal and electrical characteristics. NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

ORDERING INFORMATION

T_J	PART GRADE	V_{OUT} (NOM)	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
−40°C to 125°C	A grade: 1% tolerance	1.25 V	SOT-23-5 (DBV)	Reel of 3000	LP2985A-125DBVR	PREVIEW
				Reel of 250	LP2985A-125DBVT	
		1.5 V		Reel of 3000	LP2985A-15DBVR	PREVIEW
				Reel of 250	LP2985A-15DBVT	
		1.8 V		Reel of 3000	LP2985A-18DBVR	PREVIEW
				Reel of 250	LP2985A-18DBVT	
		2.5 V		Reel of 3000	LP2985A-25DBVR	PREVIEW
				Reel of 250	LP2985A-25DBVT	
		2.8 V		Reel of 3000	LP2985A-28DBVR	LPJ_
				Reel of 250	LP2985A-28DBVT	
		2.85 V		Reel of 3000	LP2985A-285DBVR	PREVIEW
				Reel of 250	LP2985A-285DBVT	
		3 V		Reel of 3000	LP2985A-30DBVR	PREVIEW
				Reel of 250	LP2985A-30DBVT	
		3.1 V		Reel of 3000	LP2985A-31DBVR	PREVIEW
				Reel of 250	LP2985A-31DBVT	
		3.3 V		Reel of 3000	LP2985A-33DBVR	LPK_
				Reel of 250	LP2985A-33DBVT	
		5 V		Reel of 3000	LP2985A-50DBVR	PREVIEW
				Reel of 250	LP2985A-50DBVT	
	Standard grade: 1.5% tolerance	1.25 V	SOT-23-5 (DBV)	Reel of 3000	LP2985-125DBVR	PREVIEW
				Reel of 250	LP2985-125DBVT	
		1.5 V		Reel of 3000	LP2985-15DBVR	PREVIEW
				Reel of 250	LP2985-15DBVT	
		1.8 V		Reel of 3000	LP2985-18DBVR	PREVIEW
				Reel of 250	LP2985-18DBVT	
		2.5 V		Reel of 3000	LP2985-25DBVR	PREVIEW
				Reel of 250	LP2985-25DBVT	
		2.8 V		Reel of 3000	LP2985-28DBVR	LPG_
				Reel of 250	LP2985-28DBVT	
		2.85 V		Reel of 3000	LP2985-285DBVR	PREVIEW
				Reel of 250	LP2985-285DBVT	
		3 V		Reel of 3000	LP2985-30DBVR	PREVIEW
				Reel of 250	LP2985-30DBVT	
		3.1 V		Reel of 3000	LP2985-31DBVR	PREVIEW
				Reel of 250	LP2985-31DBVT	
		3.3 V		Reel of 3000	LP2985-33DBVR	LPF_
				Reel of 250	LP2985-33DBVT	
		5 V		Reel of 3000	LP2985-50DBVR	PREVIEW
				Reel of 250	LP2985-50DBVT	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DBV: The actual top-side marking has one additional character that designates the assembly/test site.

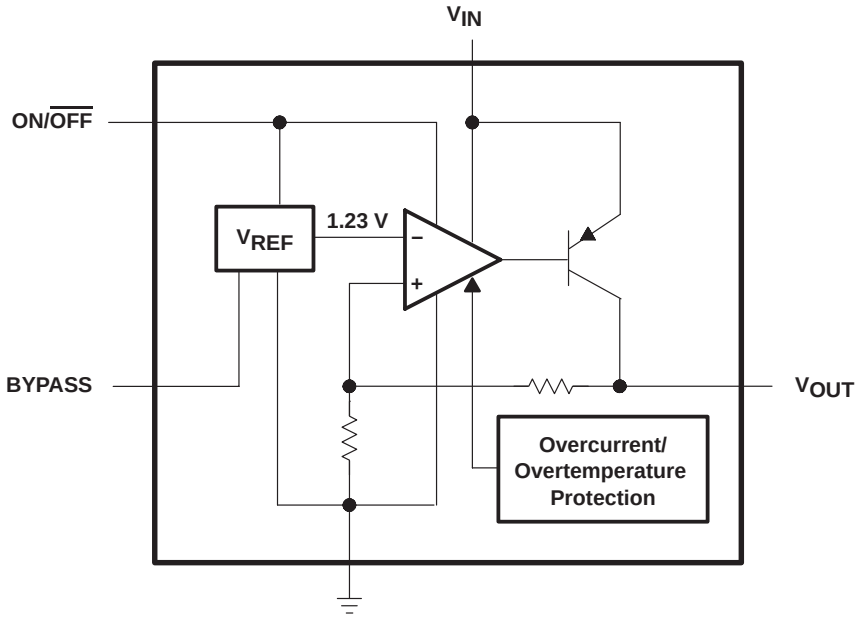
ORDERING INFORMATION (continued)

T_J	PART GRADE	V_{OUT} (NOM)	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
−40°C to 125°C	A grade: 1% tolerance	1.25 V	NanoFree™ – WCSP 0.17-mm Bump (YZQ, Pb-free)	Reel of 3000	LP2985A-125YZQR	PREVIEW
		1.5 V			LP2985A-15YZQR	
		1.8 V			LP2985A-18YZQR	
		2.5 V			LP2985A-25YZQR	
		2.8 V			LP2985A-28YZQR	
		2.85 V			LP2985A-285YZQR	
		3 V			LP2985A-30YZQR	
		3.1 V			LP2985A-31YZQR	
		3.3 V			LP2985A-33YZQR	
		5 V			LP2985A-50YZQR	
		1.25 V	NanoFree™ – WCSP 0.30-mm Bump (YZU, Pb-free)	Reel of 3000	LP2985A-125YZUR	PREVIEW
		1.5 V			LP2985A-15YZUR	
		1.8 V			LP2985A-18YZUR	
		2.5 V			LP2985A-25YZUR	
		2.8 V			LP2985A-28YZUR	
		2.85 V			LP2985A-285YZUR	
		3 V			LP2985A-30YZUR	
		3.1 V			LP2985A-31YZUR	
		3.3 V			LP2985A-33YZUR	
		5 V			LP2985A-50YZUR	
	Standard grade: 1.5% tolerance	1.25 V	NanoFree™ – WCSP 0.17-mm Bump (YZQ, Pb-free)	Reel of 3000	LP2985-125YZQR	PREVIEW
		1.5 V			LP2985-15YZQR	
		1.8 V			LP2985-18YZQR	
		2.5 V			LP2985-25YZQR	
		2.8 V			LP2985-28YZQR	
		2.85 V			LP2985-285YZQR	
		3 V			LP2985-30YZQR	
		3.1 V			LP2985-31YZQR	
		3.3 V			LP2985-33YZQR	
		5 V			LP2985-50YZQR	
		1.25 V	NanoFree™ – WCSP 0.30-mm Bump (YZU, Pb-free)	Reel of 3000	LP2985-125YZUR	PREVIEW
		1.5 V			LP2985-15YZUR	
		1.8 V			LP2985-18YZUR	
		2.5 V			LP2985-25YZUR	
		2.8 V			LP2985-28YZUR	
		2.85 V			LP2985-285YZUR	
		3 V			LP2985-30YZUR	
		3.1 V			LP2985-31YZUR	
		3.3 V			LP2985-33YZUR	
		5 V			LP2985-50YZUR	

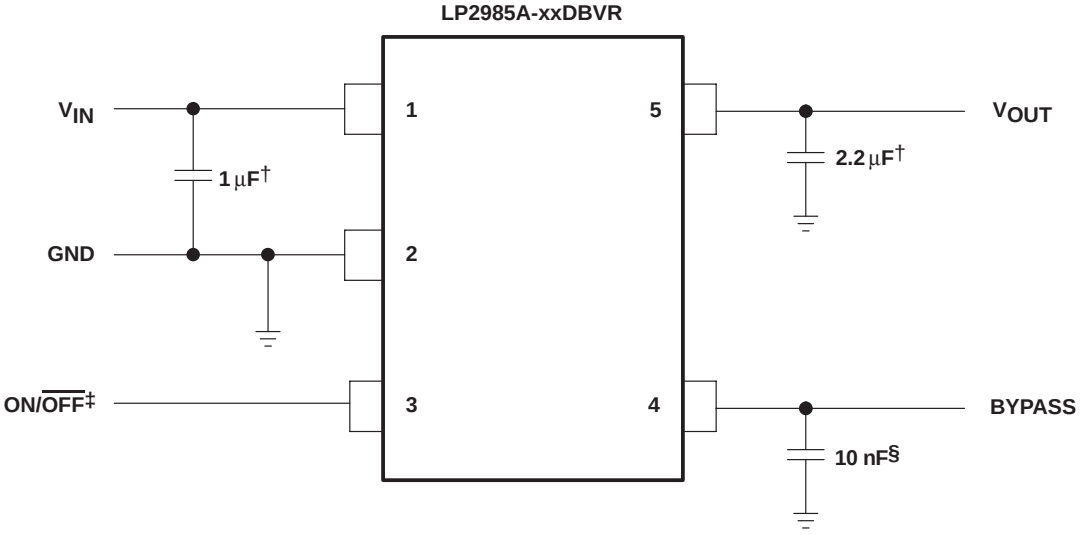
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ YZQ/YZU: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, ● = Pb-free).

functional block diagram



basic application circuit



† Minimum C_{OUT} value for stability (can be increased without limit for improved stability and transient response)
‡ ON/$\overline{\text{OFF}}$ must be actively terminated. Connect to V_{IN} if shutdown feature is not used.
§ Optional BYPASS capacitor for low-noise operation

absolute maximum ratings over the virtual junction temperature range (unless otherwise noted)†

Continuous input voltage range, V_{IN}: DBV package . . . . . −0.3 V to 16 V
YZQ/YZU package . . . . . −0.3 V to 12 V
ON/$\overline{OFF}$ input voltage range, $V_{ON/\overline{OFF}}$: DBV package . . . . . −0.3 V to 16 V
YZQ/YZU package . . . . . −0.3 V to 12 V
Output voltage range (see Note 1) . . . . . −0.3 V to 9 V
Input/output voltage differential range, V_{IN}-V_{OUT} (see Note 2): DBV package . . . . . −0.3 V to 16 V
YZQ/YZU package . . . . . −0.3 V to 12 V
Output current, I_O (see Note 3) . . . . . Internally limited (short-circuit protected)
Package thermal impedance, θ_{JA} (see Notes 3 and 4): DBV package . . . . . 206°C/W
YZQ package . . . . . TBD°C/W
YZU package . . . . . TBD°C/W
Operating virtual junction temperature . . . . . 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. If load is returned to a negative power supply in a dual-supply system, the output must be diode clamped to GND.
2. The PNP pass transistor has a *parasitic* diode connected between the input and output. This diode normally is reverse biased ($V_{IN} > V_{OUT}$), but will be forward biased if the output voltage exceeds the input voltage by a diode drop (see Application Information for more details).
3. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
4. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
V_{IN}	Supply input voltage	DBV package	2.2†	16	V
		YZQ/YZU package	2.2†	12	
$V_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input voltage		0	V_{IN}	V
I_{OUT}	Output current			150	mA
T_J	Virtual junction temperature		−40	125	°C

‡ Recommended minimum V_{IN} is the greater of:
a) 2.5 V or
b) $V_{OUT(max)}$ + rated dropout voltage (max) for operating I_L

electrical characteristics at specified virtual junction temperature range, $V_{IN} = V_{OUT}$ (nominal) + 1 V, $V_{ON/\overline{OFF}}$ = 2 V, C_{IN} = 1 µF, I_L = 1 mA, C_{OUT} = 4.7 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_J	LP2985A-XX			LP2985-XX			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
ΔV_{OUT}	Output voltage tolerance	I_L = 1 mA	25°C	−1		1	−1.5		1.5	%V_{NOM}
		1 mA ≤ I_L ≤ 50 mA	25°C	−1.5		1.5	−2.5		2.5	
			−40°C to 125°C	−2.5		2.5	−3.5		3.5	
		1 mA ≤ I_L ≤ 150 mA	25°C	−2.5		2.5	−3.0		3.0	
			−40°C to 125°C	−3.5		3.5	−4.0		4.0	
	Line regulation	DBV package: V_{IN} = [$V_{OUT(NOM)}$ + 1 V] to 16 V YZQ/YZU package: V_{IN} = [$V_{OUT(NOM)}$ + 1 V] to 12 V	25°C		0.007	0.014		0.007	0.014	%/V
			−40°C to 125°C			0.032			0.032	
V_{IN}-V_{OUT}	Dropout voltage (see Note 5)	I_L = 0	25°C		1	3		1	3	mV
			−40°C to 125°C			5			5	
		I_L = 1 mA	25°C		7	10		7	10	
			−40°C to 125°C			15			15	
		I_L = 10 mA	25°C		40	60		40	60	
			−40°C to 125°C			90			90	
		I_L = 50 mA	25°C		120	150		120	150	
			−40°C to 125°C			225			225	
		I_L = 150 mA	25°C		280	350		280	350	
			−40°C to 125°C			575			575	
I_{GND}	Ground pin current	I_L = 0	25°C		65	95		65	95	µA
			−40°C to 125°C			125			125	
		I_L = 1 mA	25°C		75	110		75	110	
			−40°C to 125°C			170			170	
		I_L = 10 mA	25°C		120	220		120	220	
			−40°C to 125°C			400			400	
		I_L = 50 mA	25°C		350	600		350	600	
			−40°C to 125°C			1000			1000	
		I_L = 150 mA	25°C		850	1500		850	1500	
			−40°C to 125°C			2500			2500	
		$V_{ON/\overline{OFF}}$ < 0.3 V (OFF)	25°C		0.01	0.8		0.01	0.8	
		$V_{ON/\overline{OFF}}$ < 0.15 V (OFF)	−40°C to 105°C		0.05	2		0.05	2	
			−40°C to 125°C			5			5	
$V_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input voltage (see Note 6)	$V_{ON/\overline{OFF}}$ = HIGH → O/P ON	25°C		1.4			1.4		V
			−40°C to 125°C	1.6			1.6			
		$V_{ON/\overline{OFF}}$ = LOW → O/P OFF	25°C		0.55			0.55		
			−40°C to 125°C			0.15			0.15	
$I_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input current	$V_{ON/\overline{OFF}}$ = 0	25°C		0.01			0.01		µA
			−40°C to 125°C			−2			−2	
		$V_{ON/\overline{OFF}}$ = 5 V	25°C		5			5		
			−40°C to 125°C			15			15	

NOTES: 5. Dropout voltage is defined as the input-to-output differential at which the output voltage drops 100 mV below the value measured with a 1-V differential.
6. The ON/$\overline{OFF}$ input must be driven properly for reliable operation (see Application Information).

electrical characteristics at specified virtual junction temperature range, $V_{IN} = V_{OUT}$ (nominal) + 1 V, $V_{ON/OFF}$ = 2 V, C_{IN} = 1 µF, I_L = 1 mA, C_{OUT} = 4.7 µF (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_J	LP2985A-XX			LP2985-XX			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_n	Output noise (RMS)	BW = 300 Hz to 50 kHz, C_{OUT} = 10 µF, C_{BYPASS} = 10 nF	25°C		30			30		µV
$\Delta V_{OUT}/\Delta V_{IN}$	Ripple rejection	f = 1kHz, C_{OUT} = 10 µF, C_{BYPASS} = 10 nF	25°C		45			45		dB
$I_{OUT(PK)}$	Peak output current	$V_{OUT} \geq V_{O(NOM)} - 5\%$	25°C		350			350		mA
$I_{OUT(SC)}$	Short-circuit current	R_L = 0 (steady state) (see Note 7)	25°C		400			400		mA

NOTE 7: See Figure 6 under *typical performance characteristics*.

APPLICATION INFORMATION

capacitors

input capacitor (C_{in})

A minimum value of 1 μF (over the entire operating temperature range) is required at the input of the LP2985. In addition, this input capacitor should be located within 1 cm of the input pin and connected to a clean analog ground. There are no Equivalent Series Resistance (ESR) requirements for this capacitor, and the capacitance can be increased without limit.

output capacitor (C_{out})

As an advantage over other regulators, the LP2985 permits the use of low-ESR capacitors at the output, including ceramic capacitors that can have an ESR as low as 5 mΩ. Tantalum and film capacitors also can be used if size and cost are not issues. The output capacitor also should be located within 1 cm of the output pin and be returned to a clean analog ground.

As with other PNP LDOs, stability conditions require the output capacitor to have a minimum capacitance and an ESR that falls within a certain range.

Minimum C_{out}: 2.2 μF (can be increased without limit to improve transient response stability margin)

ESR range: see Figure 1

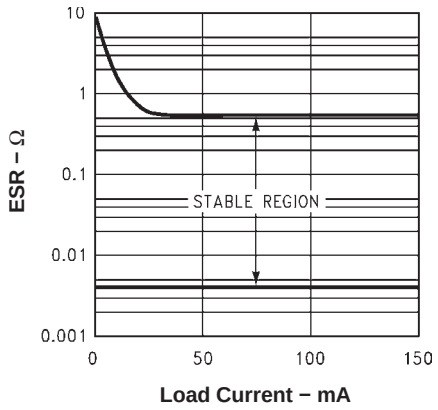


Figure 1. 2.2-V/3.3-μF ESR Curves

It is critical that both the minimum capacitance and ESR requirement be met *over the entire operating temperature range.* Depending on the type of capacitors used, both these parameters can vary significantly with temperature (see *capacitor characteristics*).

noise bypass capacitor (C_{bypass})

The LP2985 allows for low-noise performance with the use of a bypass capacitor that is connected to the internal bandgap reference via the BYPASS pin. This high-impedance bandgap circuitry is biased in the microampere range and, thus, cannot be loaded significantly, otherwise, its output − and, correspondingly, the output of the regulator − will change. Thus, for best output accuracy, dc leakage current through C_{bypass} should be minimized as much as possible and never should exceed 100 nA.

A 10-nF capacitor is recommended for C_{bypass}; ceramic and film capacitors are well suited for this purpose.

APPLICATION INFORMATION

capacitor characteristics

ceramics

Ceramic capacitors are ideal choices for use on the output of the LP2985 for several reasons. For capacitances in the range of 2.2 μF to 4.7 μF, ceramic capacitors have the lowest cost and the lowest ESR, making them choice candidates for filtering high-frequency noise. For instance, a typical 2.2-μF ceramic capacitor has an ESR in the range of 10 mΩ to 20 mΩ and, thus, satisfies minimum ESR requirements of the regulator.

Ceramic capacitors have one glaring disadvantage that must be taken into account − a poor temperature coefficient, where the capacitance can vary significantly with temperature. For instance, a large-value ceramic capacitor (≥2.2 μF) can lose more than half of its capacitance as the temperature rises from 25°C to 85°C. Thus, a 2.2-μF capacitor at 25°C will drop well below the minimum C_{out} required for stability, as ambient temperature rises. For this reason, select an output capacitor that maintains the minimum 2.2 μF required for stability over the *entire operating temperature range*. Note that there are some ceramic capacitors that can maintain a ±15% capacitance tolerance over temperature.

tantalum

Tantalum capacitors can be used at the output of the LP2985, but there are significant disadvantages that could prohibit their use:

- In the 1-μF to 4.7-μF range, tantalum capacitors are more expensive than ceramics of the equivalent capacitance and voltage ratings.
- Tantalum capacitors have higher ESRs than their equivalent-sized ceramic counterparts. Thus, to meet the ESR requirements, a higher-capacitance tantalum may be required, at the expense of larger size and higher cost.
- The ESR of a tantalum capacitor increases as temperature drops, as much as double from 25°C to −40°C. Thus, ESR margins must be maintained over the temperature range to prevent regulator instability.

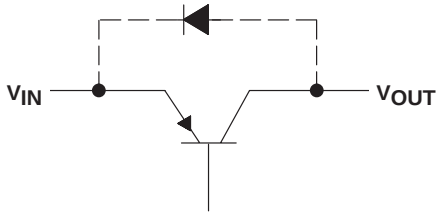
ON/$\overline{\text{OFF}}$ operation

The LP2985 allows for a shutdown mode via the ON/$\overline{\text{OFF}}$ pin. Driving the pin LOW (≤0.3 V) turns the device OFF; conversely, a HIGH (≥1.6 V) turns the device ON. If the shutdown feature is not used, ON/$\overline{\text{OFF}}$ should be connected to the input to ensure that the regulator is on at all times. For proper operation, do not leave ON/$\overline{\text{OFF}}$ unconnected, and apply a signal with a slew rate of ≥40 mV/μs.

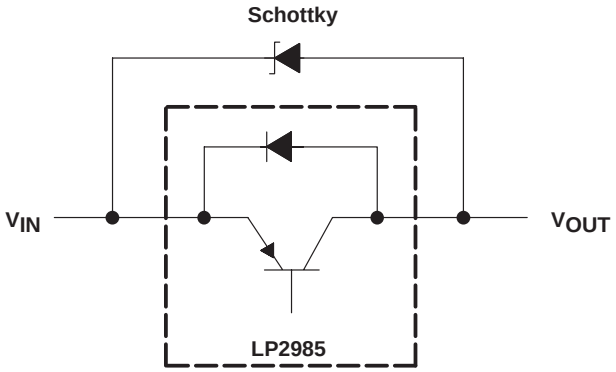
APPLICATION INFORMATION

reverse input-output voltage

There is an inherent diode present across the PNP pass element of the LP2985.



With the anode connected to the output, this diode is reverse biased during normal operation, since the input voltage is higher than the output. However, if the output is pulled higher than the input for any reason, this diode is forward biased and can cause a parasitic silicon-controlled rectifier (SCR) to latch, resulting in high current flowing from the output to the input. Thus, to prevent possible damage to the regulator in any application where the output may be pulled above the input, an external Schottky diode should be connected between the output and input. With the anode on output, this Schottky limits the reverse voltage across the output and input pins to ∼0.3 V, preventing the regulator's internal diode from forward biasing.



TYPICAL PERFORMANCE CHARACTERISTICS

C_{IN} = 1 μF, C_{OUT} = 4.7 μF, V_{IN} = $V_{OUT(NOM)}$ +1 V, T_A = 25°C, ON/OFF Pin Is Tied to V_{IN} (unless otherwise specified)

OUTPUT VOLTAGE vs TEMPERATURE

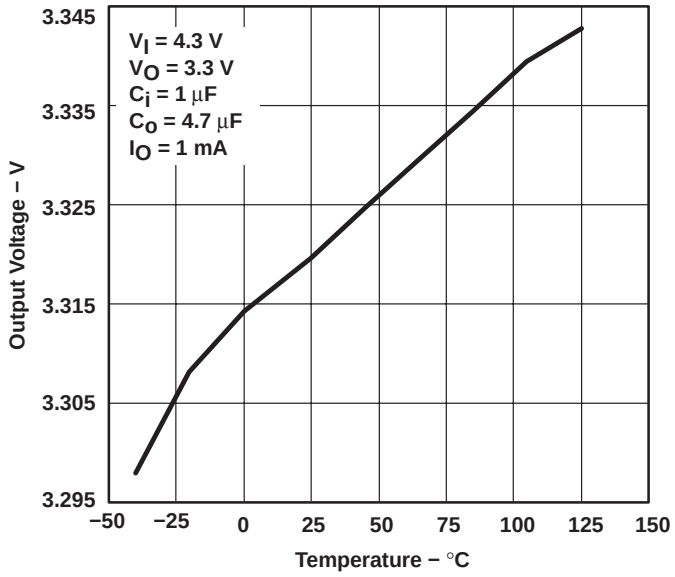


Figure 2

DROPOUT VOLTAGE vs TEMPERATURE

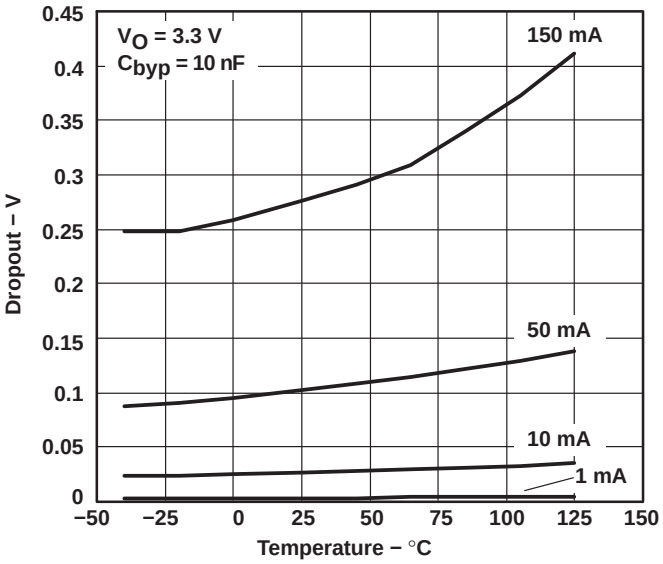


Figure 3

SHORT-CIRCUIT CURRENT vs TIME

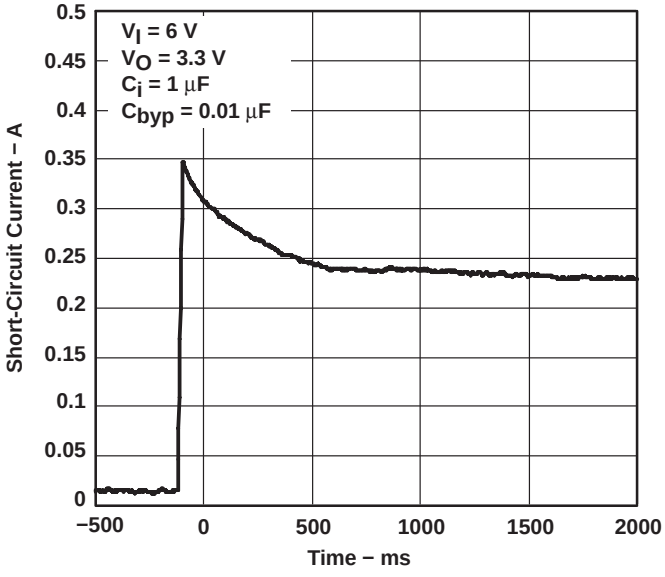


Figure 4

SHORT-CIRCUIT CURRENT vs TIME

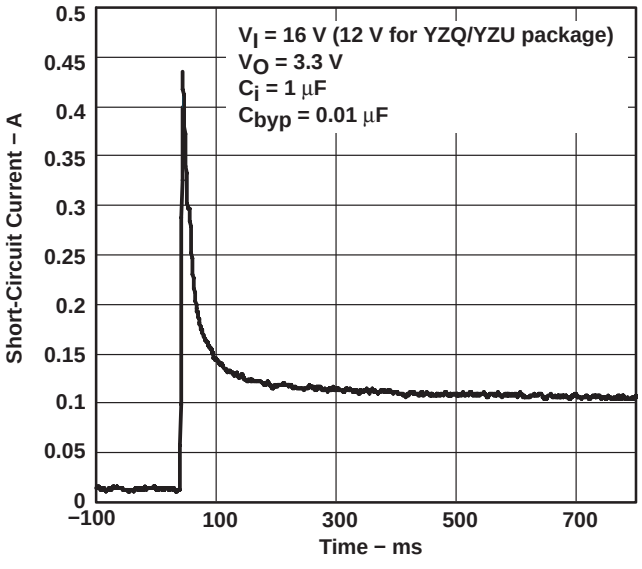


Figure 5

TYPICAL PERFORMANCE CHARACTERISTICS

C_{IN} = 1 μF, C_{OUT} = 4.7 μF, V_{IN} = $V_{OUT(NOM)}$ +1 V, T_A = 25°C, ON/$\overline{OFF}$ Pin Is Tied to V_{IN} (unless otherwise specified)

SHORT-CIRCUIT CURRENT vs OUTPUT VOLTAGE

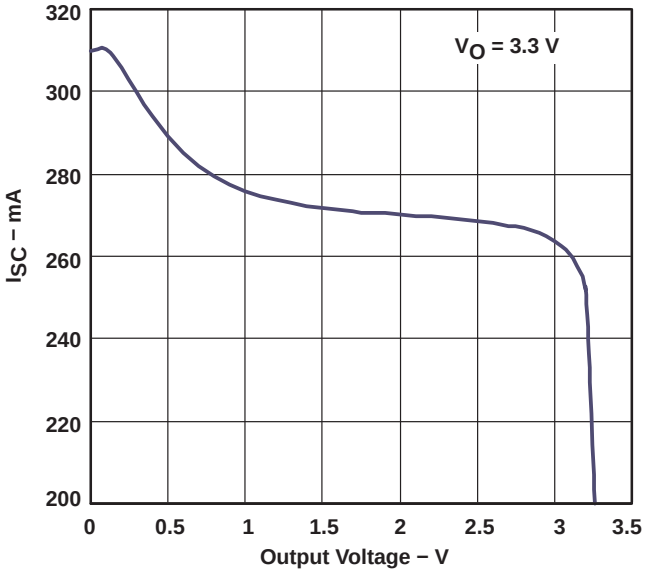


Figure 6

GROUND-PIN CURRENT vs LOAD CURRENT

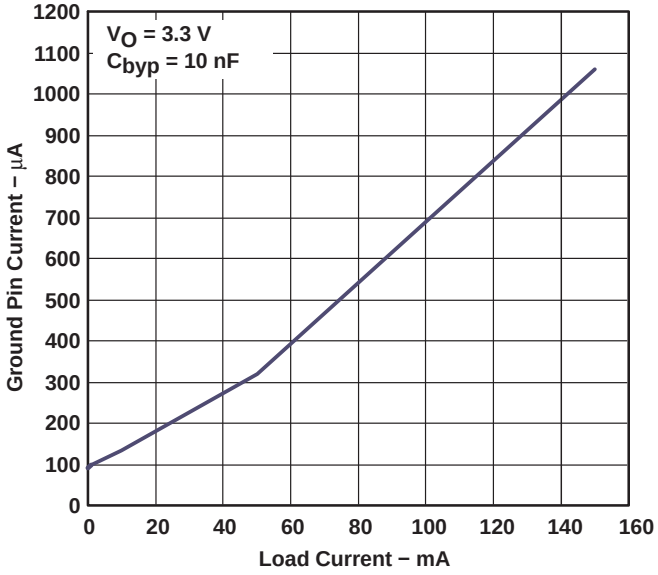


Figure 7

RIPPLE REJECTION vs FREQUENCY

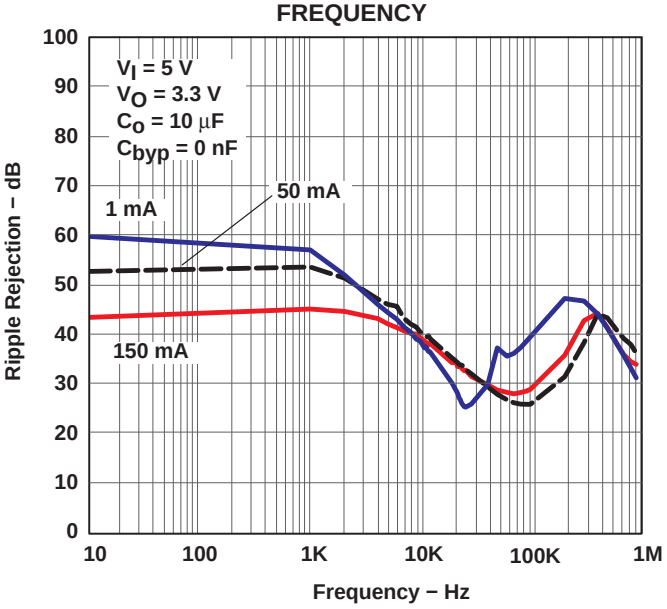


Figure 8

RIPPLE REJECTION vs FREQUENCY

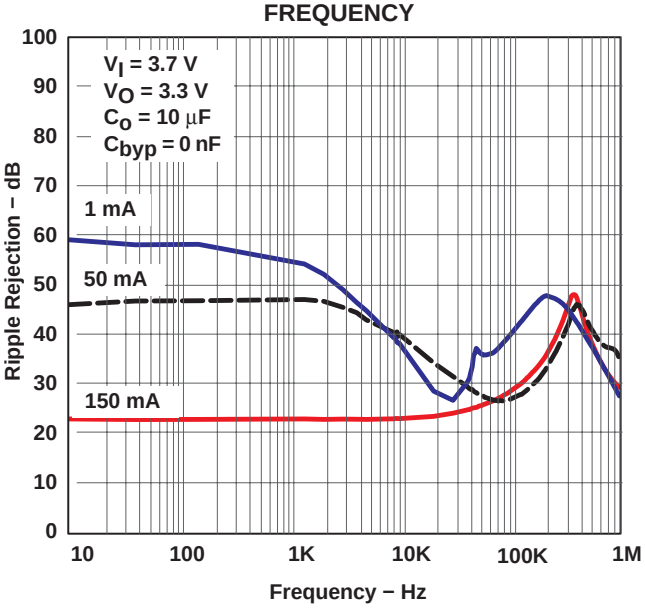


Figure 9

TYPICAL PERFORMANCE CHARACTERISTICS

C_{IN} = 1 μF, C_{OUT} = 4.7 μF, V_{IN} = $V_{OUT(NOM)}$ +1 V, T_A = 25°C, ON/OFF Pin Is Tied to V_{IN} (unless otherwise specified)

RIPPLE REJECTION
vs
FREQUENCY

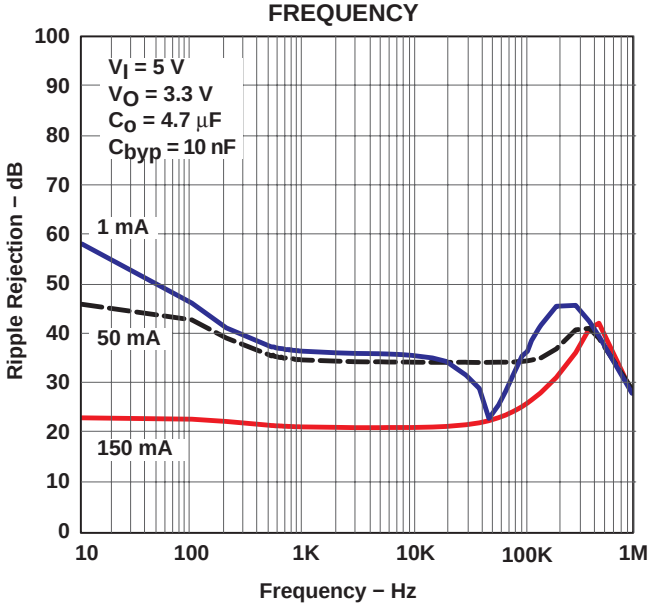


Figure 10

RIPPLE REJECTION
vs
FREQUENCY

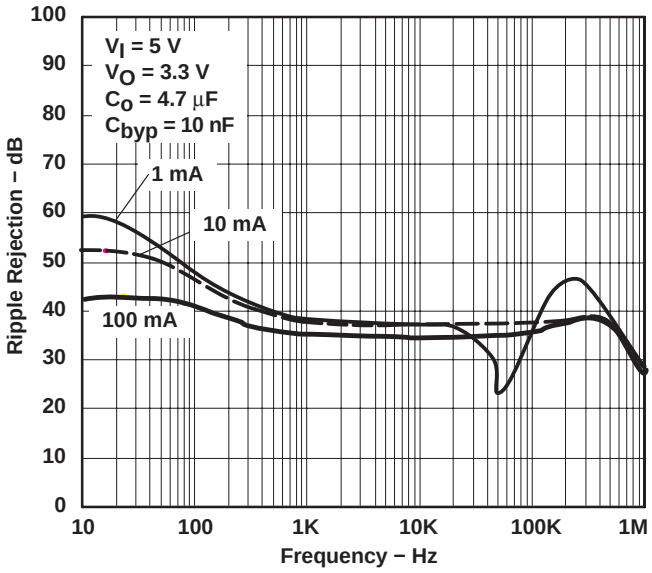


Figure 11

OUTPUT IMPEDANCE
vs
FREQUENCY

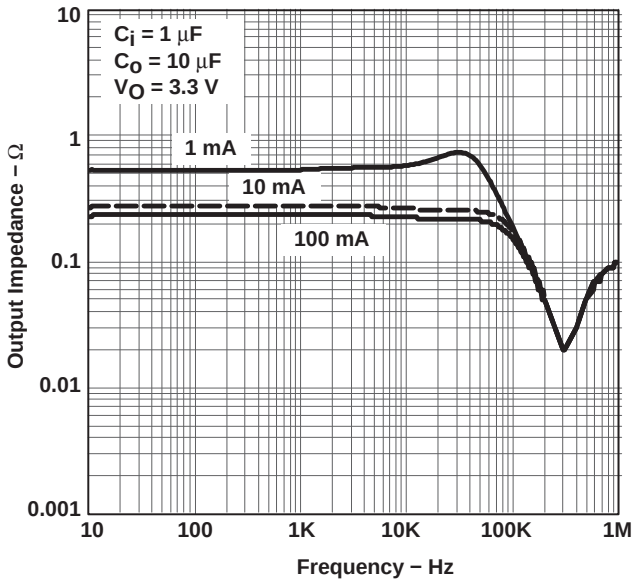


Figure 12

OUTPUT IMPEDANCE
vs
FREQUENCY

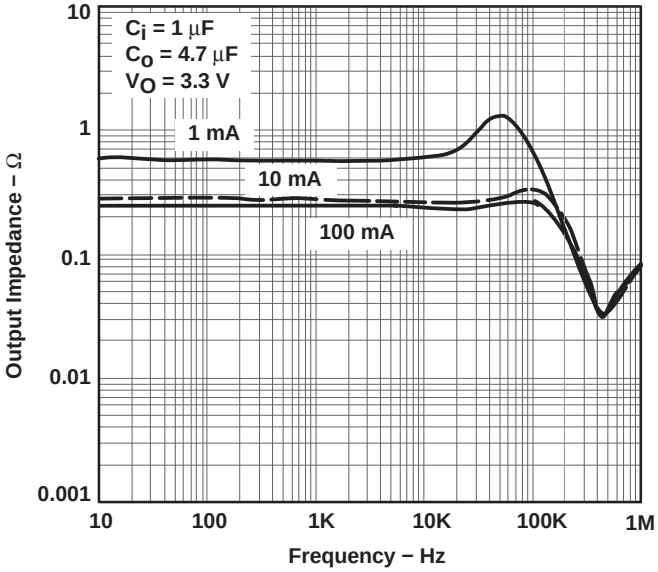


Figure 13

TYPICAL PERFORMANCE CHARACTERISTICS

C_{IN} = 1 μF, C_{OUT} = 4.7 μF, V_{IN} = $V_{OUT(NOM)}$ +1 V, T_A = 25°C, ON/$\overline{OFF}$ Pin Is Tied to V_{IN} (unless otherwise specified)

OUTPUT NOISE DENSITY vs FREQUENCY

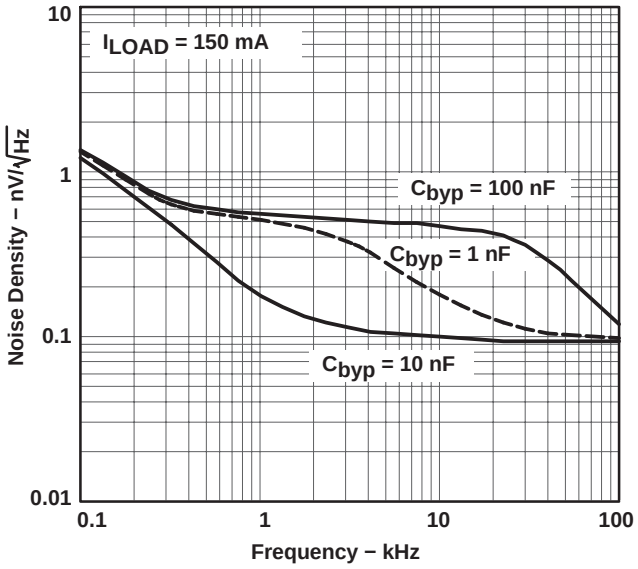


Figure 14

OUTPUT NOISE DENSITY vs FREQUENCY

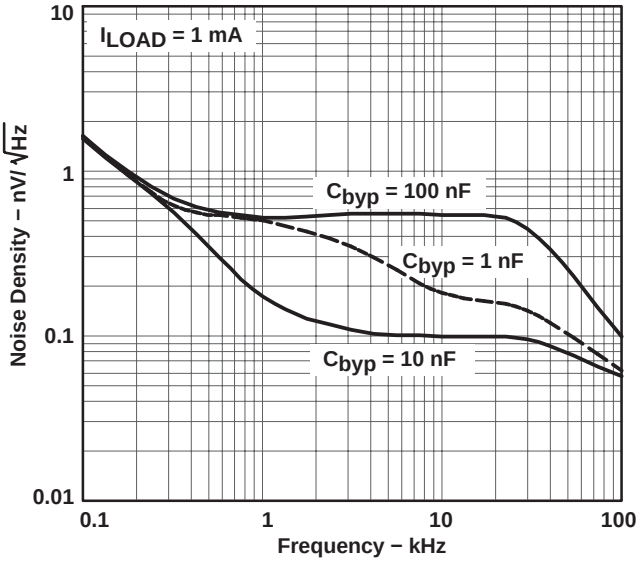


Figure 15

INPUT CURRENT vs INPUT VOLTAGE

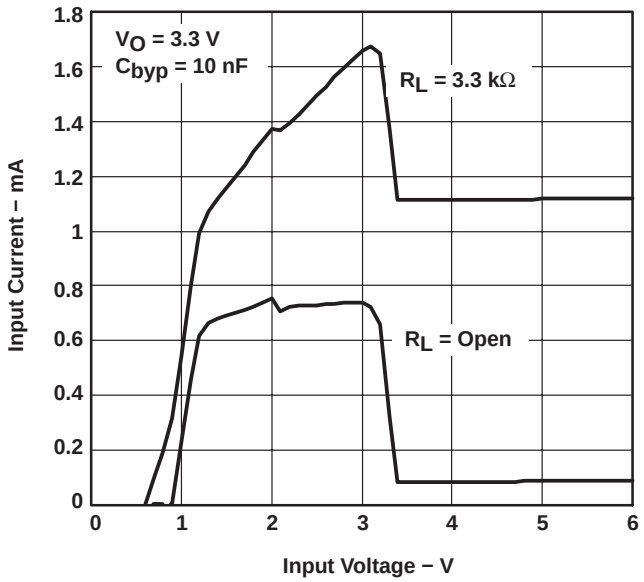


Figure 16

GROUND-PIN CURRENT vs TEMPERATURE

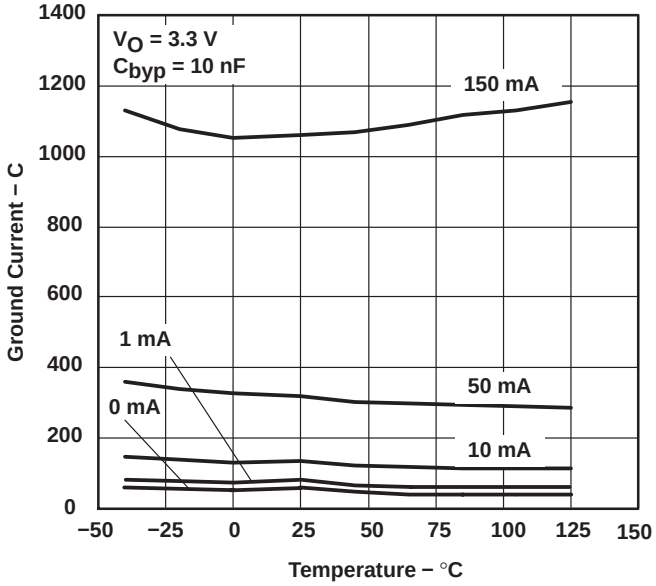


Figure 17

TYPICAL PERFORMANCE CHARACTERISTICS

C_{IN} = 1 μF, C_{OUT} = 4.7 μF, V_{IN} = $V_{OUT(NOM)}$ +1 V, T_A = 25°C, ON/OFF Pin Is Tied to V_{IN} (unless otherwise specified)

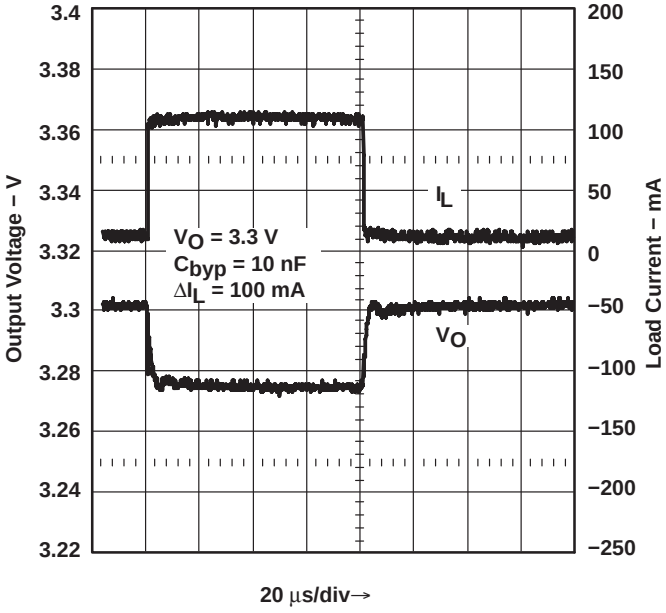


Figure 18

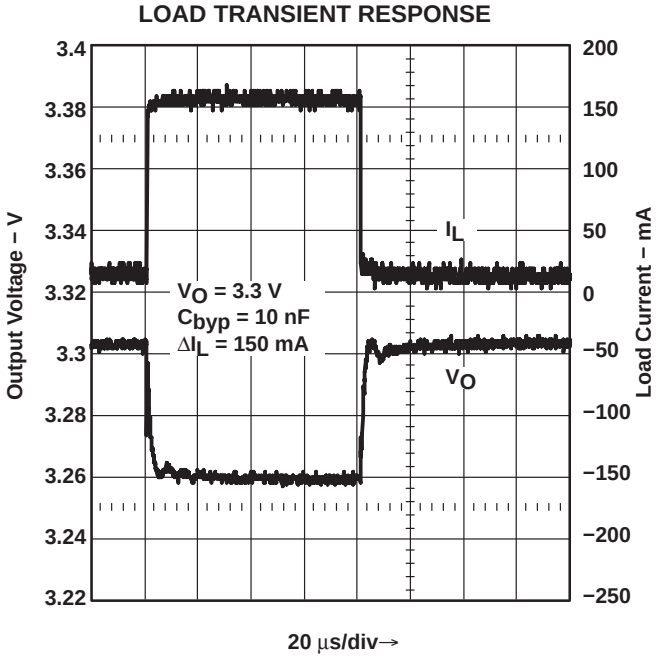


Figure 19

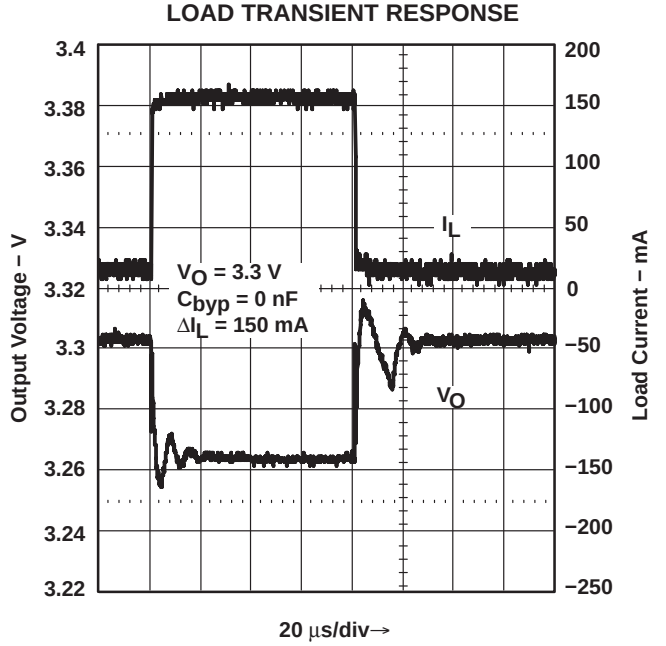


Figure 20

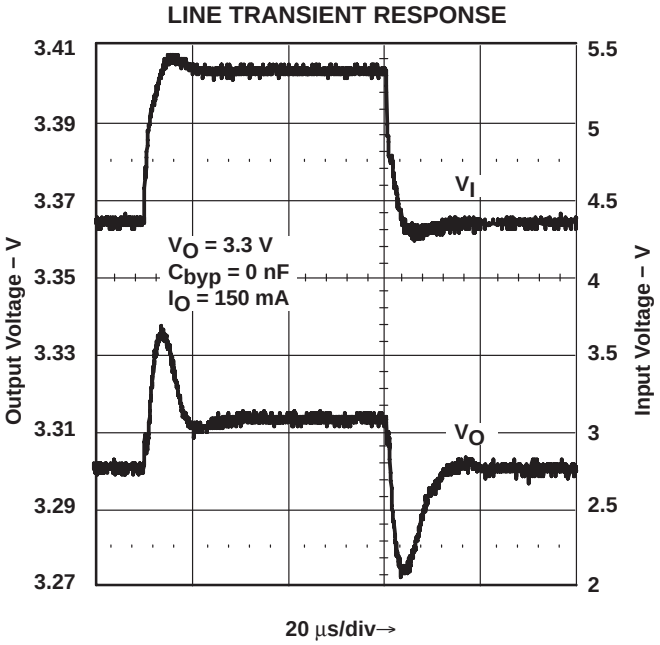


Figure 21

TYPICAL PERFORMANCE CHARACTERISTICS

C_{IN} = 1 μF, C_{OUT} = 4.7 μF, V_{IN} = $V_{OUT(NOM)}$ +1 V, T_A = 25°C, ON/$\overline{OFF}$ Pin Is Tied to V_{IN} (unless otherwise specified)

LINE TRANSIENT RESPONSE

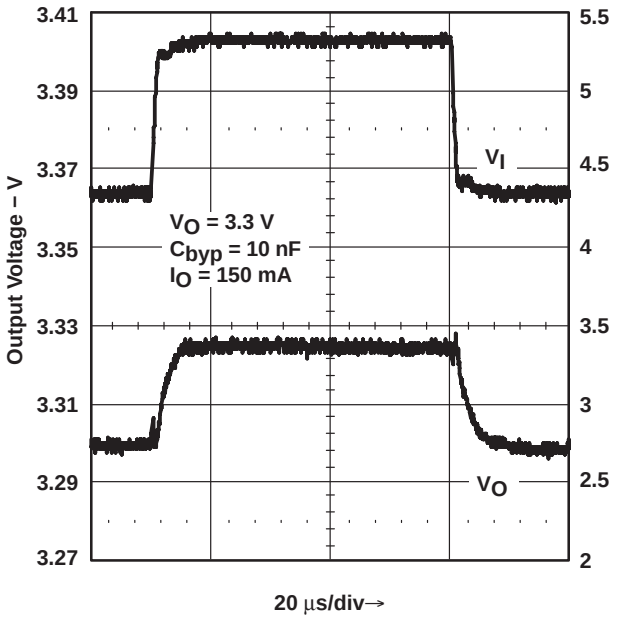


Figure 22

LINE TRANSIENT RESPONSE

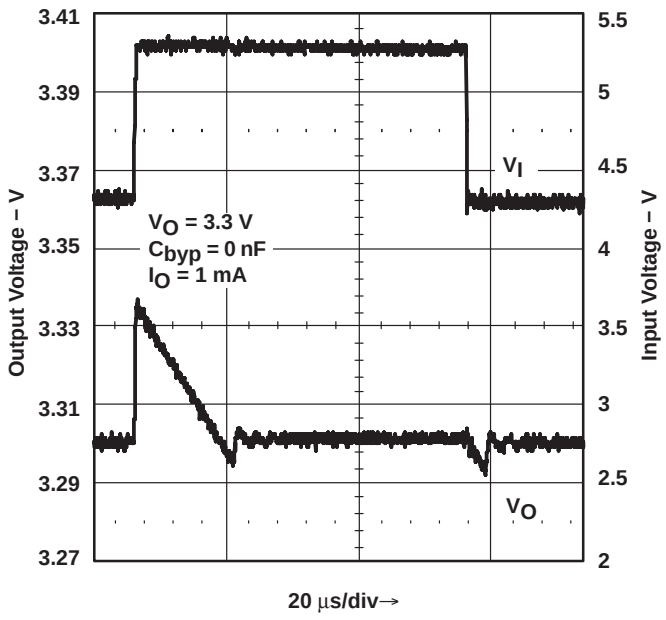


Figure 23

LINE TRANSIENT RESPONSE

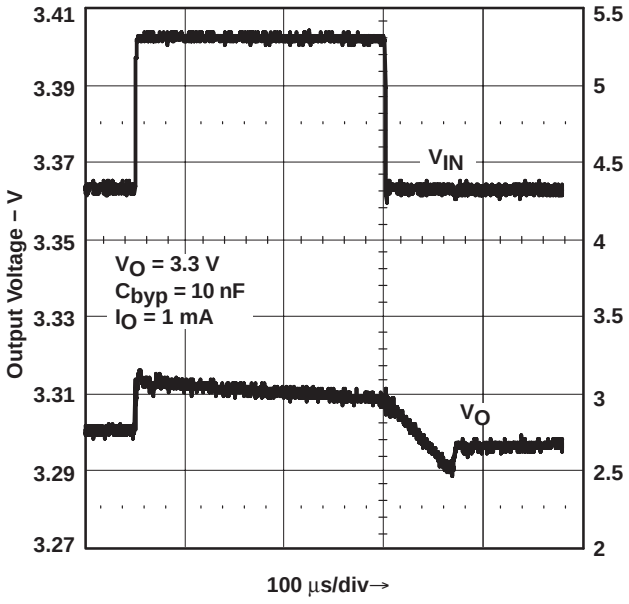


Figure 24

TURN-ON TIME

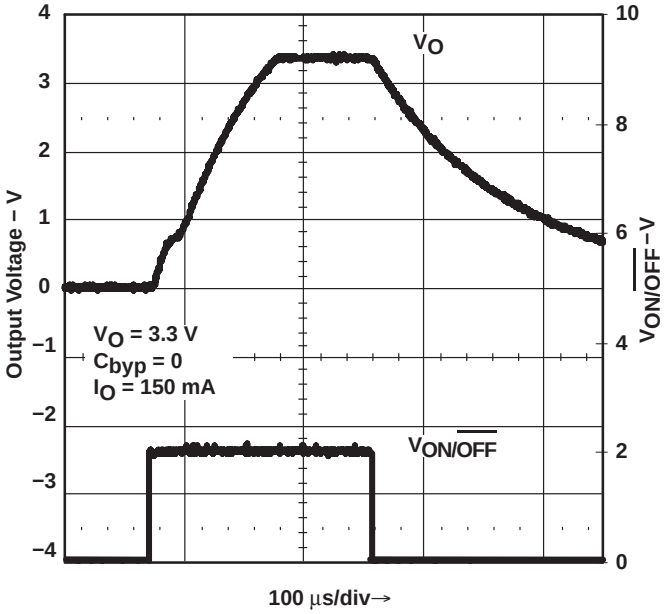


Figure 25

TYPICAL PERFORMANCE CHARACTERISTICS

C_{IN} = 1 μF, C_{OUT} = 4.7 μF, V_{IN} = $V_{OUT(NOM)}$ +1 V, T_A = 25°C, ON/$\overline{OFF}$ Pin Is Tied to V_{IN} (unless otherwise specified)

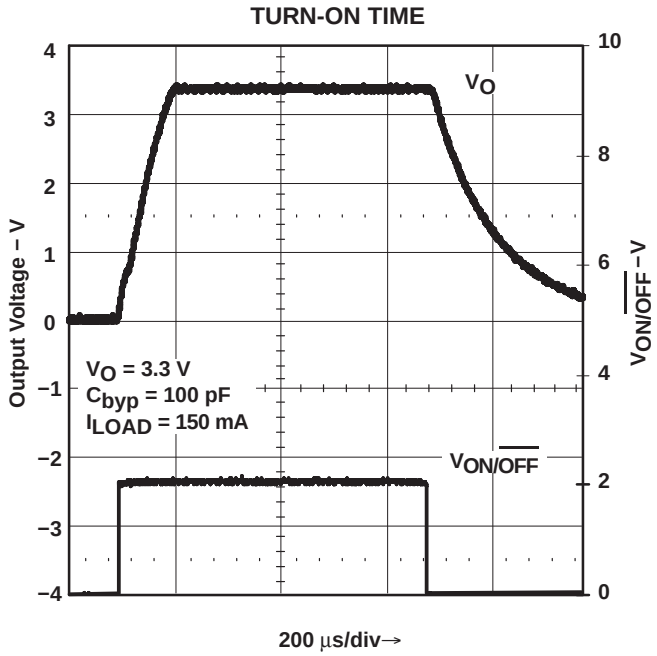


Figure 26

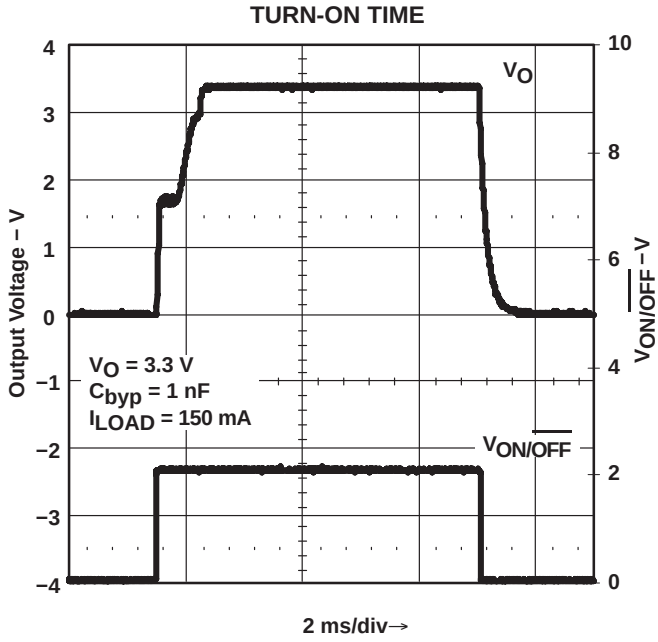


Figure 27

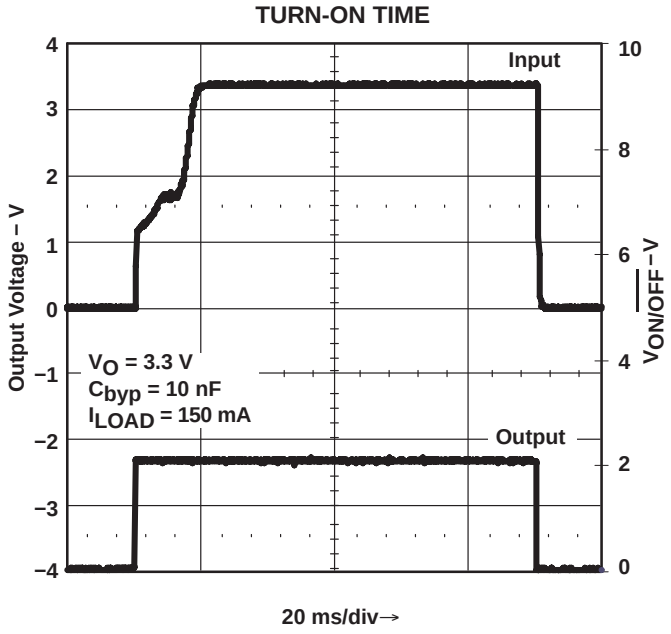
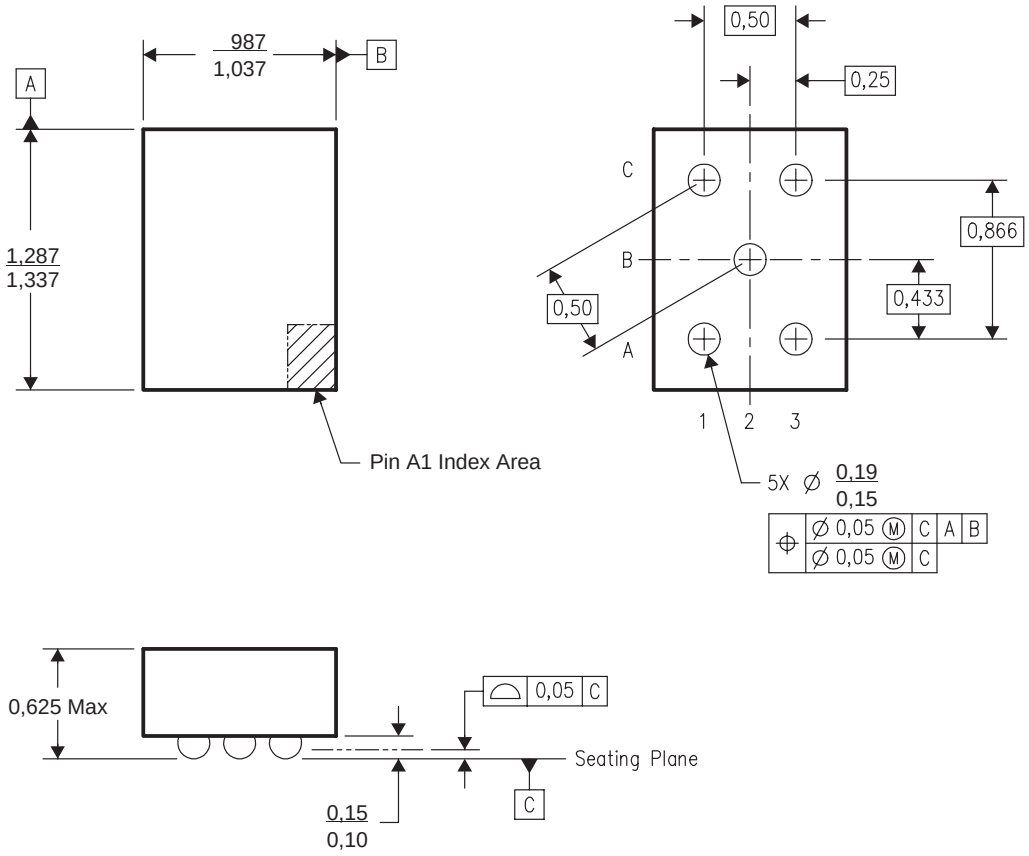


Figure 28

WAFER CHIP SCALE INFORMATION

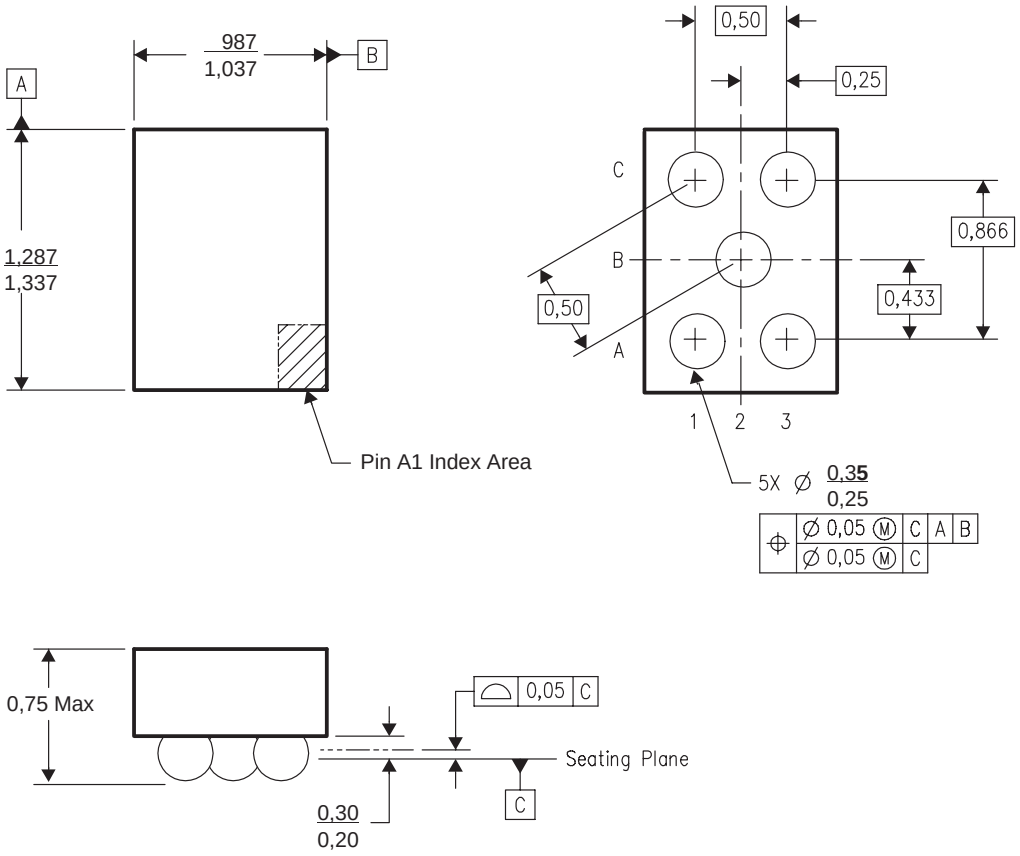
LP2985x-xxYZQ NanoFree (0.17-mm Pb-Free Bump)



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration
D. This package is tin-lead (SnPb); consult the factory for availability of lead-free material.

WAFER CHIP SCALE INFORMATION

LP2985x-xxYZU NanoFree (0.30-mm Pb-Free Bump)



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar package configuration
D. This package is tin-lead (SnPb); consult the factory for availability of lead-free material.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
LP2985-18DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP2985-18DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP2985-18DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP2985-18DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP2985-18YEUR	PREVIEW	DSBGA	YEU	5	3000	TBD	Call TI	Call TI
LP2985-28DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP2985-28DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP2985-28DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP2985-28DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP2985-28YEQR	PREVIEW	DSBGA	YEQ	5	3000	TBD	Call TI	Call TI
LP2985-28YEUR	PREVIEW	DSBGA	YEU	5	3000	TBD	Call TI	Call TI
LP2985-28YZQR	PREVIEW	DSBGA	YZQ	5	3000	TBD	Call TI	Call TI
LP2985-28YZUR	PREVIEW	DSBGA	YZU	5	3000	TBD	Call TI	Call TI
LP2985-33DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP2985-33DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP2985-33DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP2985-33DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP2985-33YEQR	PREVIEW	DSBGA	YEQ	5	3000	TBD	Call TI	Call TI
LP2985-33YEUR	PREVIEW	DSBGA	YEU	5	3000	TBD	Call TI	Call TI
LP2985-33YZQR	PREVIEW	DSBGA	YZQ	5	3000	TBD	Call TI	Call TI
LP2985-33YZUR	PREVIEW	DSBGA	YZU	5	3000	TBD	Call TI	Call TI
LP2985A-18DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP2985A-18DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP2985A-18DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP2985A-18DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP2985A-28DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP2985A-28DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP2985A-28DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP2985A-28DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIM

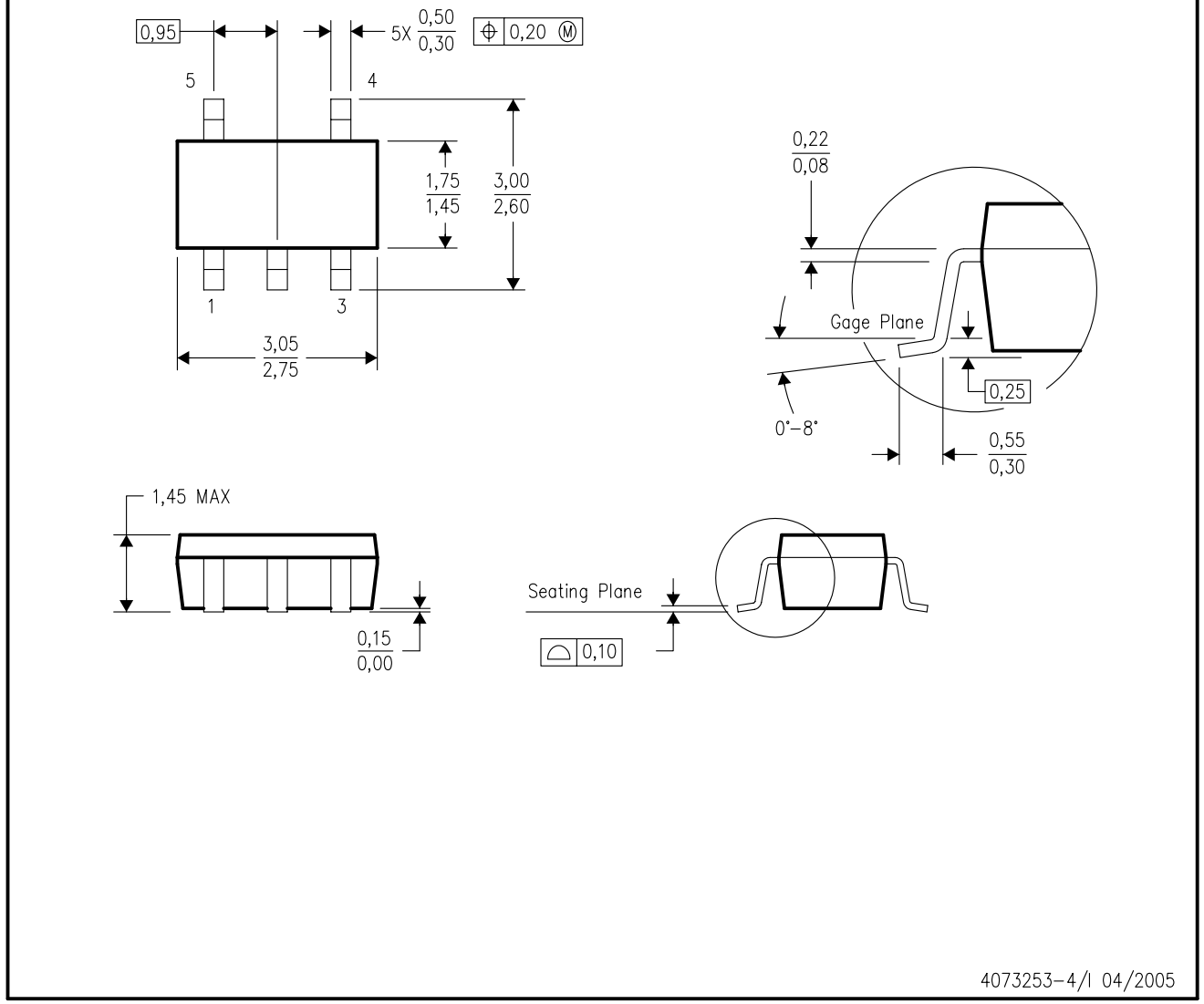
Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
						no Sb/Br)		
LP2985A-33DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP2985A-33DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP2985A-33DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP2985A-33DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

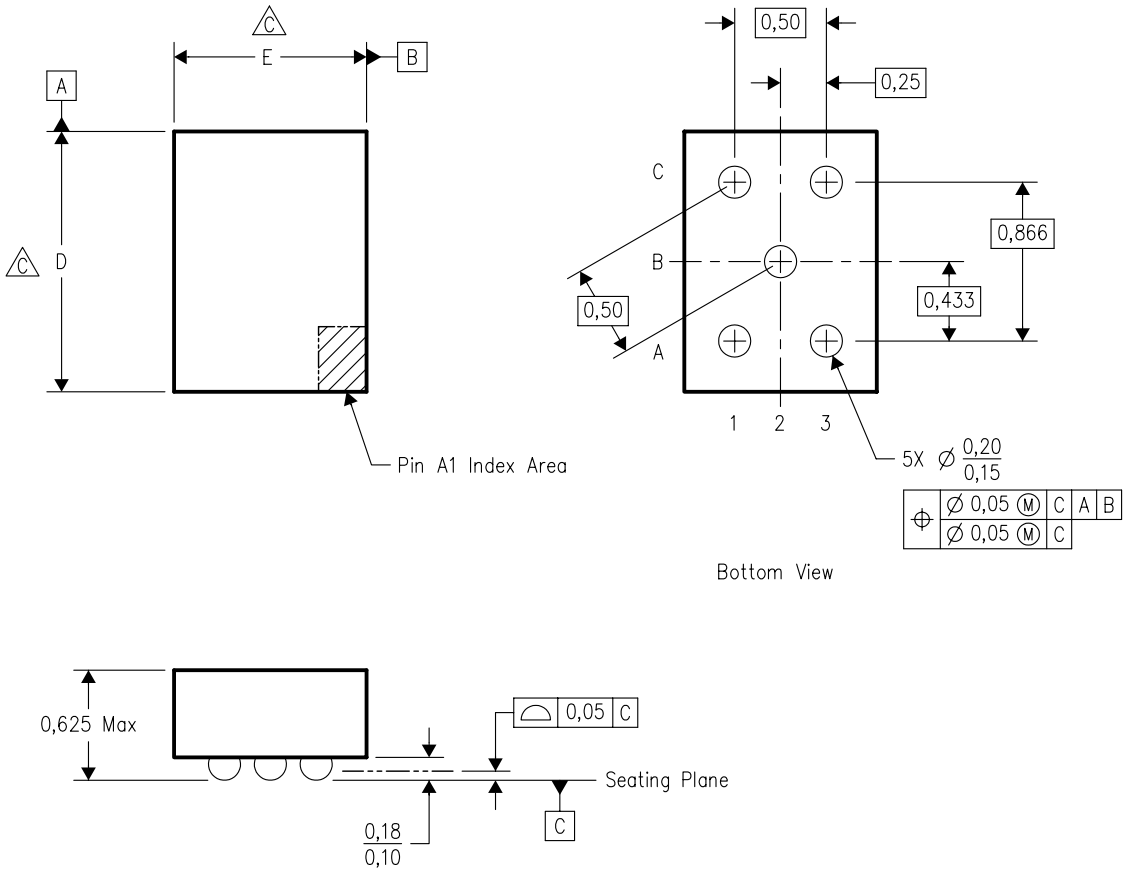
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–178 Variation AA.

YEQ (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY



4205338/C 04/2004

Notes:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Devices in this YEQ package can have dimension D ranging from 1.17 to 1.67 and dimension E ranging from 0.80 to 1.30. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
D. NanoStar™ package configuration.
E. This package contains tin–lead (SnPb) balls. Refer to the 5 YZQ package (drawing 4205677) for lead–free balls.

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