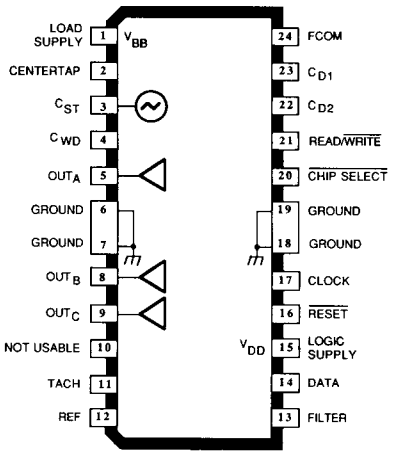
8901

3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVER WITH BACK-EMF SENSING



Dwg. PP-032A

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Load Supply Voltage, V_{BB} . . . . . **V_{DD} + 1.0 V**
Output Current, I_{OUT} . . . . . **±1.1 A**
Logic Supply Voltage, V_{DD} . . . . . **6.0 V**
Logic Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **0°C to +70°C**
Junction Temperature, T_J . . . . . **+150°C†**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

† Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.

Output current rating may be restricted to a value determined by system concerns and factors. These include: system duty cycle and timing, ambient temperature, and use of any heatsinking and/or forced cooling. For reliable operation, the specified maximum junction temperature should not be exceeded.

The A8901CLB is a three-phase brushless dc motor controller/driver for use in 5 V hard-disk drives. The three half-bridge outputs are low on-resistance n-channel DMOS devices capable of driving up to 1.25 A. The A8901CLB provides complete, reliable, self-contained back-EMF sensing motor startup and running algorithms. Linear current control circuitry provides precise motor speed regulation.

A serial port allows the user to program various features and modes of operation, startup current limit, sleep mode, and diagnostic modes.

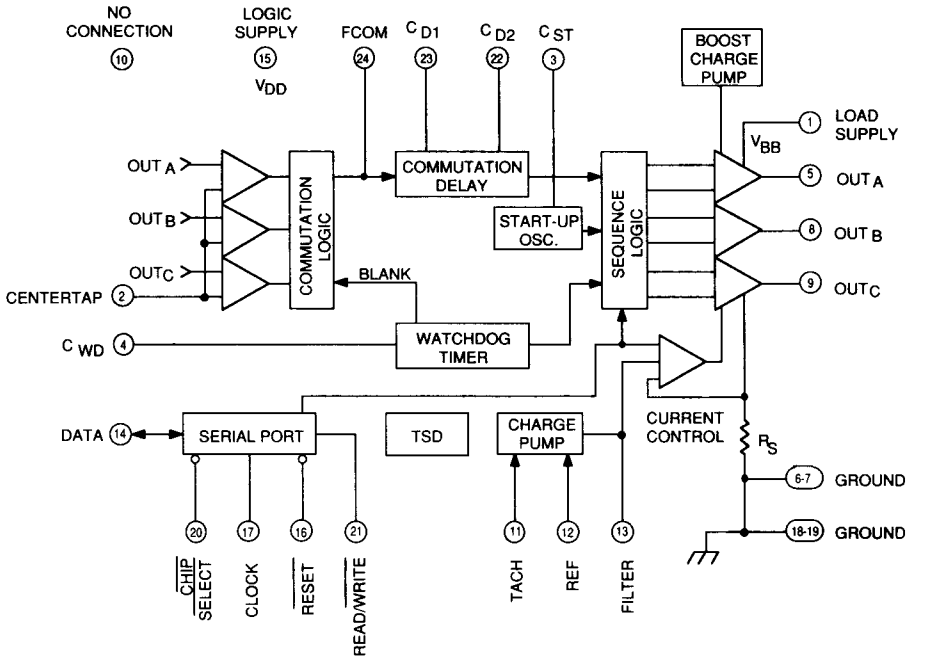
The A8901CLB is fabricated in Allegro's BCD (Bipolar CMOS DMOS) process, an advanced mixed-signal technology that combines bipolar, analog and digital CMOS, and DMOS power devices. It is provided in a 24-lead wide-body SOIC batwing package. The package provides for the smallest possible construction in surface-mount applications.

FEATURES

- DMOS Outputs
- Low $r_{DS(on)}$
- Startup Commutation Circuitry
- Back-EMF Commutation Circuitry
- Serial Port Interface
- Programmable Start-Up Current
- Diagnostics Mode
- Sleep Mode
- Linear Current Control
- Internal Current Sensing
- Internal Thermal Shutdown Circuitry

Always order by complete part number: **A8901CLB**.

FUNCTIONAL BLOCK DIAGRAM



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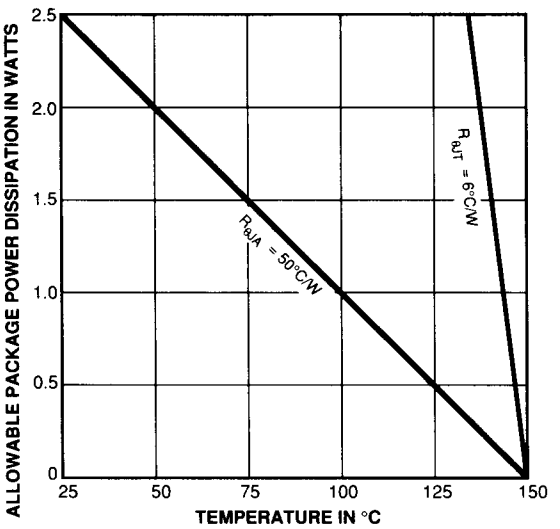


Dwg. GP-019A

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5.0 V

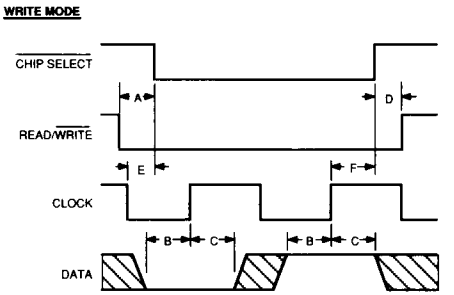
Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Logic Supply Voltage	V_{DD}	Operating	4.5	5.0	5.5	V
Logic Supply Current	I_{DD}	Operating	—	7.5	10	mA
		Sleep Mode	—	—	1.5	mA
Load Supply Voltage	V_{BB}	Operating	—	—	V_{DD} + 1	V
Thermal Shutdown	T_J		—	165	—	°C
Thermal Shutdown Hys.	ΔT_J		—	20	—	°C
Output Drivers						
Output Leakage Current	I_{DSX}	V_{BB} = 14 V, V_{OUT} = 14 V	—	1.0	300	µA
		V_{BB} = 14 V, V_{OUT} = 0 V	—	-1.0	-300	µA
Total Output ON Resistance	$r_{DS(on)}$	I_{OUT} = 600 MA	—	1.2	1.4	Ω
Output Sustaining Voltage	$V_{DS(sus)}$	V_{BB} = 6 V, I_{OUT} = 900 mA, L = 3 mH	6.0	—	—	V
Clamp Diode Forward Voltage	V_F	I_F = 1.0 A	—	1.25	1.5	V
Control Logic						
Logic Input Voltage	$V_{IN(0)}$	DATA, RESET, CLK, REF, R/W,	-0.3	—	1.5	V
	$V_{IN(1)}$	CHIP SELECT, TACH	3.5	—	5.3	V
Logic Input Current	$I_{IN(0)}$	V_{IN} = 0 V	—	—	-0.5	µA
	$I_{IN(1)}$	V_{IN} = 5.0 V	—	—	1.0	µA
DATA Output Voltage	$V_{OUT(0)}$	I_{OUT} = 250 µA	—	—	1.5	V
	$V_{OUT(1)}$	I_{OUT} = -100 µA	3.5	—	—	V
FCOM Output Voltage	$V_{OUT(0)}$	I_{OUT} = 500 µA	—	—	1.5	V
	$V_{OUT(1)}$	I_{OUT} = -200 µA	3.5	—	—	V
C_{ST} Current	I_{CST}	Charging	16	20	28	µA
		Discharging	-16	-20	-28	µA
C_{ST} Threshold	V_{CSTH}		2.1	2.5	2.9	V
	V_{CSTL}		—	500	—	mV
Filter Current	I_{FILTER}	Charging	8.0	10	15	µA
		Discharging	-8.0	-10	-15	µA
		Leakage, V_{FILTER} = 2.5 V	—	5.0	—	nA
C_D Current (C_{D1} or C_{D2})	I_{CD}	Charging	16	23	30	µA
		Discharging	-35	-53	-72	µA
C_D Current Matching	—	$I_{CD(DISCHRG)}/I_{CD(CHRG)}$	2.0	2.2	2.4	—
C_D Threshold	V_{CD}		—	2.5	—	V
C_{WD} Current	I_{CWD}	Charging	16	22	28	µA

Continued next page...

ELECTRICAL CHARACTERISTICS continued

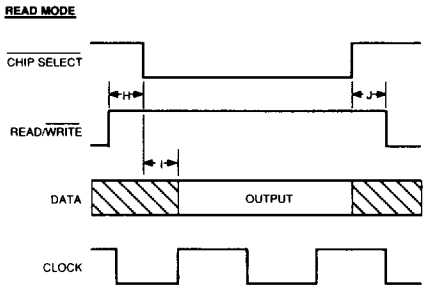
Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
C_{WD} Threshold Voltage	V_{TL}		1.4	1.5	1.55	V
	V_{TH}		2.25	2.5	2.75	V
I_{OUT}(MAX) Accuracy	—	I_{OUT} = 1 A	—	±20	—	%
Transconductance Gain	g_m		0.4	0.5	0.6	A/V
Centertap Resistors	R_{CT}		5.5	10	12	kΩ
Back-EMF Hysteresis	—	$V_{BEMF} - V_{CTAP}$ at	15	25	40	mV
		FCOM Transition	-15	-25	-40	mV

SERIAL PORT TIMING CONDITIONS



Dwg. WP-014A

A. Minimum READ/WRITE setup time before CHIP SELECT ..... **150 ns**
B. Minimum DATA setup time before CLOCK rising edge ..... **100 ns**
C. Minimum DATA hold time after CLOCK rising edge ..... **100 ns**
D. Minimum READ/WRITE hold time after CHIP SELECT disable ..... **100 ns**
E. Minimum CLOCK low time before CHIP SELECT ..... **50 ns**
F. Minimum CHIP SELECT hold time after CLOCK rising edge ..... **150 ns**
G. Maximum CLOCK frequency ..... **3.3 MHz**



Dwg. WP-023

H. Minimum READ/WRITE setup time before CHIP SELECT ..... **150 ns**
I. Minimum time until output DATA valid ..... **150 ns**
J. Minimum READ/WRITE hold time after CHIP SELECT disable ..... **150 ns**

TERMINAL FUNCTIONS

Term.	Terminal Name	Function
1	LOAD SUPPLY	V_{BB}; the 5 V motor supply.
2	CENTERTAP	Motor centertap connection for back-EMF detection circuitry.
3	C_{ST}	Startup oscillator timing capacitor.
4	C_{WD}	Timing capacitor used by the watchdog circuit to disable the back-EMF comparators during commutation transients, and to detect incorrect motor position.
5	OUT_A	Power amplifier A output to motor.
6-7	GROUND	Power and logic ground and thermal heat sink.
8	OUT_B	Power amplifier B output to motor.
9	OUT_C	Power amplifier C output to motor.
10	NC	No internal connection; may be used as tie point or wired through.
11	TACH	Logic-level tachometer input for speed control loop.
12	REF	Logic-level reference input for speed control loop.
13	FILTER	Analog voltage input to control motor current. Also, compensation node for speed control loop.
14	DATA	Serial port data input/output line.
15	LOGIC SUPPLY	V_{DD}; the 5 V logic supply.
16	$\overline{\text{RESET}}$	When pulled low forces the chip into sleep mode; clears all serial port bits.
17	CLOCK	Clock input for serial port.
18-19	GROUND	Power and logic ground and thermal heat sink.
20	$\overline{\text{CHIP SELECT}}$	Strobe input (active low) for data word.
21	READ/$\overline{\text{WRITE}}$	Logic-level input to control direction of serial-port data; logic high = read, logic low = write.
22	C_{D2}	One of two capacitors used to generate the ideal commutation points from the back-EMF zero crossing points.
23	C_{D1}	One of two capacitors used to generate the ideal commutation points from the back-EMF zero crossing points.
24	FCOM	Logic-level signal that changes state at every back-EMF zero crossing.

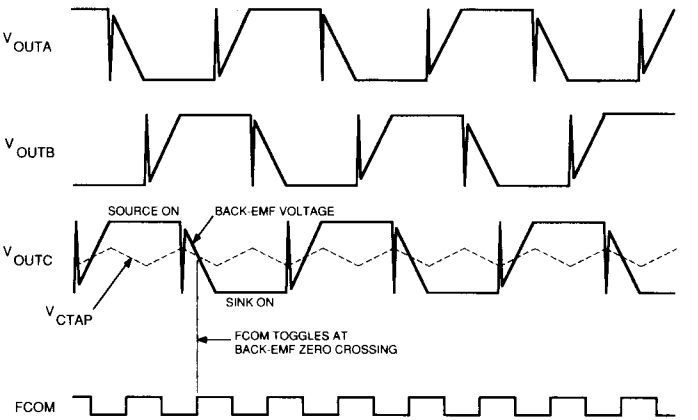
FUNCTIONAL DESCRIPTION

Power Outputs. The power outputs of the A8901CLB are n-channel DMOS transistors with a total source plus sink $r_{DS(on)}$ of typically 1.1 Ω. Internal charge pump boost circuitry provides voltage above supply for driving the high-side DMOS gates. Intrinsic ground clamp and flyback diodes provide protection when switching inductive loads and may be used to rectify motor back-EMF in power-down conditions. An external Schottky power diode or pass FET is required in series with the load supply to allow motor back-EMF rectification in power down conditions.

Back-EMF Sensing Motor Startup and Running Algorithm. The A8901CLB provides a complete self-contained back-EMF sensing startup and running commutation scheme. The three half-bridge outputs are controlled by a state machine. There are six possible combinations. In each state, one output is high (sourcing current), one low (sinking current), and one is OFF (high impedance or 'Z'). Motor back-EMF is sensed at the OFF output. The truth table for the output drivers sequencing is:

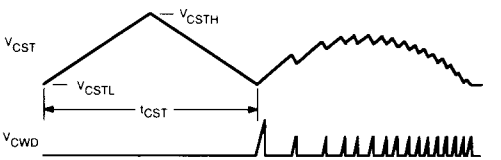
Sequencer State	OUT_A	OUT_B	OUT_C
1	High	Low	Z
2	Z	Low	High
3	Low	Z	High
4	Low	High	Z
5	Z	High	Low
6	High	Z	Low

At startup, the outputs are enabled in one of the sequencer states shown. The back-EMF is examined at the OFF output by comparing the output voltage to the motor centertap voltage at CENTERTAP. The motor will then either step forward, step backward, or remain stationary (if in a null-torque position). If the motor moves, the back-EMF detection circuit waits for the correct polarity back-EMF zero crossing (output crossing through centertap). True back-EMF zero crossings are used by the adaptive commutation delay circuit to advance the state sequencer (commutate) at the proper time to synchronously run the motor. Back-EMF zero crossings are indicated by FCOM, an internal signal that toggles at every zero crossing. FCOM is available at the DATA terminal via the programmable data out multiplexer.



Dwg. WP-016-1

Startup Oscillator. If the motor does not move at the initial startup state, then it is in a null-torque position. In this case, the outputs are commutated automatically by the startup oscillator after a period set by the external capacitor at C_{ST}.

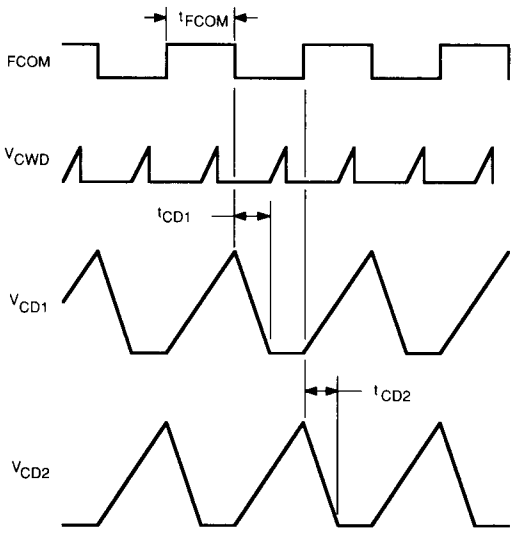


Dwg. WP-020

where $$t_{CST} = \frac{4(V_{CSTH} - V_{CSTL}) \times C_{ST}}{I_{ST(charge)} + I_{ST(discharge)}}$$

In the next state, the motor will move, back EMF will be detected, and the motor will accelerate synchronously. Once normal synchronous back-EMF commutation occurs, the startup oscillator is defeated by pulses of pulldown current at C_{ST} at each commutation, which prevents C_{ST} from reaching its upper threshold and thus completing a cycle and commutating.

Adaptive Commutation Delay. The adaptive commutation delay circuit uses the back-EMF zero-crossing indicator signal (FCOM) to determine an optimal commutation time for efficient synchronous operation. This circuit commutates the outputs, delayed from the last zero crossing, using two external timing capacitors, C_{D1} and C_{D2}, to measure the time between crossings.

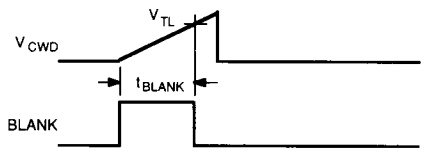


Dwg. WP-016-2

where $$t_{CD} = t_{FCOM} \times \frac{I_{CD(charge)}}{|I_{CD(discharge)}|}$$

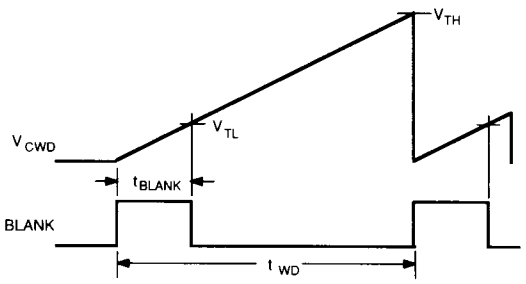
C_{D1} charges up with a fixed current from its 2.5 V reference while FCOM is high. When FCOM goes low at the next zero crossing, C_{D1} is discharged at approximately twice the charging current. When C_{D1} reaches the CD threshold, a commutation occurs. C_{D2} operates similarly except on the opposite phase of FCOM . Thus the commutations occur approximately halfway between zero crossings. The actual delay is slightly less than halfway to compensate for electrical delays in the motor, which improves efficiency.

NORMAL COMMUTATION



Dwg. WP-022

WATCHDOG-TRIGGERED COMMUTATION



Dwg. WP-021

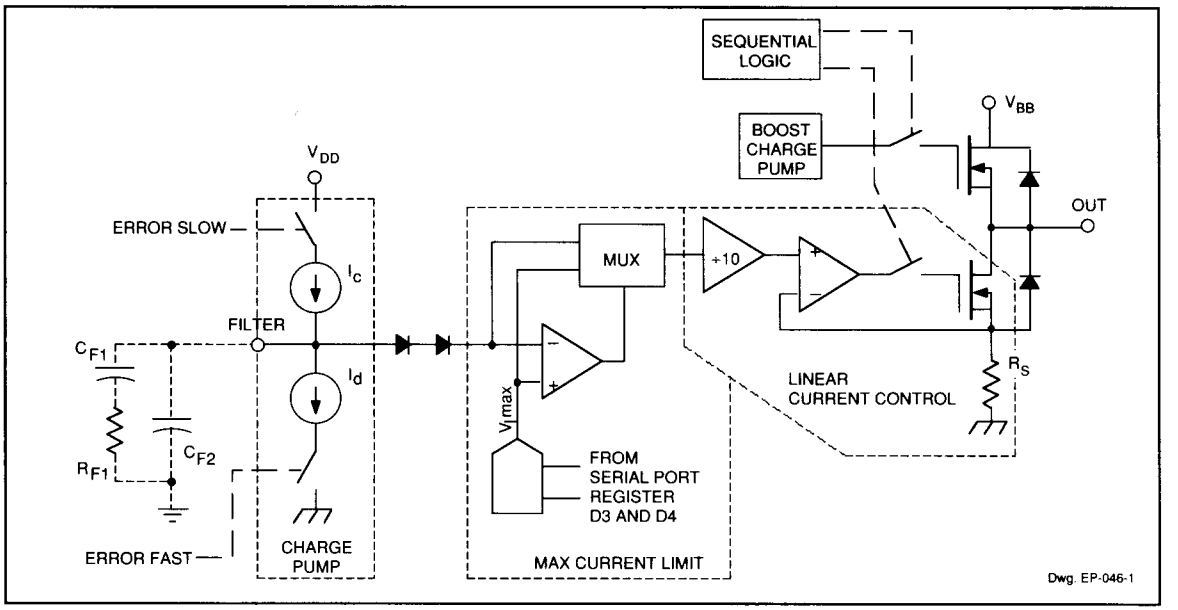
Blanking and Watchdog Timing Functions. The blanking and watchdog timing functions are derived from one timing capacitor, C_{WD}.

where $$t_{BLANK} = \frac{V_{TL} \times C_{WD}}{I_{CWD}}$$

and $$t_{WD} = \frac{V_{TH} \times C_{WD}}{I_{CWD}}$$

The CWD capacitor begins charging at each commutation, initiating the BLANK signal. BLANK is an internal signal that inhibits the back-EMF comparators during the commutation transients, preventing errors due to inductive recovery and voltage settling transients.

The watchdog timing function allows time to detect correct motor position by checking the back-EMF polarity after each commutation. If the correct polarity is not observed between t_{BLANK} and t_{WD}, then the watchdog timer commutates the outputs to the next state to synchronize the motor. This function is useful in preventing excessive reverse rotation, and helps in resynchronizing (or starting) with a moving spindle.



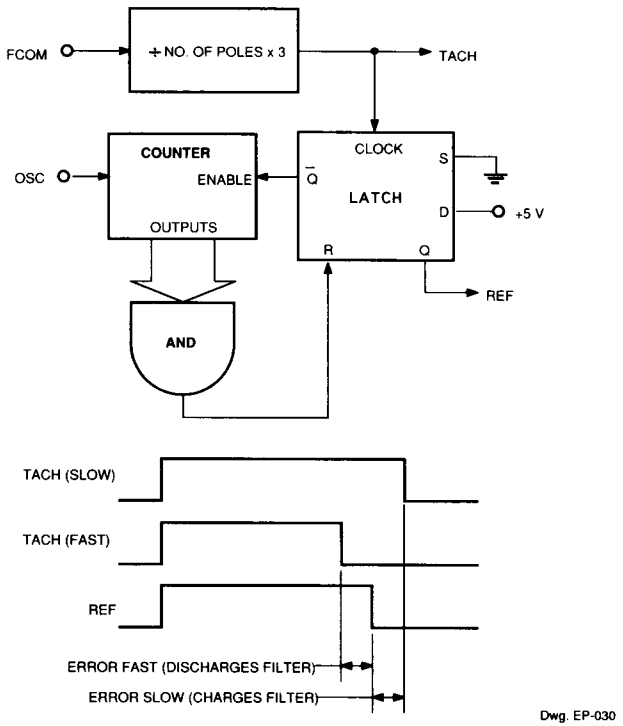
Current Control. The A8901CLB provides linear current control of the sink drivers during start-up and running modes. In the start-up mode, the maximum load current can be programmed via the serial port (see Serial Port). During the running mode, the output current is linearly controlled for low noise in frequency-locked or phase-locked speed-control systems. To accomplish this the load current is monitored by an internal sense resistor (RS). The voltage across the sense resistor is compared to one-tenth the voltage at the FILTER terminal less two diode drops (see Figure 1), generating an error voltage to drive the gate of the appropriate output sink transistor. This creates a load current that is proportional to the voltage at the FILTER terminal less two diode drops. This transconductance function is $I_{OUT} = (V_{FILTER} - 2V_D) / 10R_S$. Where R_S is nominally 0.2 Ω, and V_D is approximately 0.7 V.

Speed Control. The A8901CLB has been configured to operate in conjunction with external digital circuitry to provide frequency-locked loop speed control of spindle motors. The TACH and REF inputs are used to turn on current sources Ic and I_d to charge and discharge a lead/lag loop filter compensation network (see Figure 2). The truth table for this function is:

REF	TACH	I_c	I_d
0	0	off	off
0	1	on	off
1	0	off	on
1	1	off	off

The external circuitry required for implementation of the speed control loop is shown in Figure 2. The operation of this circuit is as follows: the FCOM signal is a logic signal that changes state every time the A8901CLB detects a back-EMF zero crossing. By dividing the FCOM signal by three times the number of poles in the motor, a TACH signal is developed that changes state every mechanical revolution. This is done to develop a low-jitter tachometer signal. The low jitter is achieved because each time the TACH signal changes state the back-EMF circuitry is looking at the same magnet pole pair.

Figure 2
EXTERNAL DIGITAL CIRCUITRY REQUIRED FOR FREQUENCY-LOCK LOOP SPEED CONTROL



The derived TACH signal is compared to the desired time (REF) for one revolution. This is done by using the positive-going edge of the TACH signal to trigger a latch that enables a counter. The counter is driven by an accurate oscillator signal and (in conjunction with an AND gate) is used to count the desired number of oscillator cycles in a single revolution. When the counter reaches its desired number the latch is reset and the REF signal goes low (see Figure 2). The TACH and REF signals are fed back to the A8901CLB to charge and discharge the filter compensation network. If the TACH signal goes low before REF an Error-Fast signal turns on I_d lowering the current in the motor and thereby reducing its speed. If the REF signal goes low before TACH an Error-Slow signal turns on I_c which increases the load current and thereby the speed of the motor. The loop filter components are used to dampen the response of the loop and achieve optimal settling time.

Response time to disturbances in speed can be improved by synchronizing to sector data once information is being read from the disc. This change can be made by changing the count number in the counter and switching TACH to a sector tachometer signal. This should be done when TACH and REF are in the low state so as not to generate an erroneous error signal.

Microprocessor controlled phase-locked loop speed control systems can use the FILTER terminal as a transconductance input by omitting the loop filter components and connecting TACH and REF to ground.

Serial Port. The serial port functions to read or write various operational and diagnostic modes from or to the A8901CLB. The serial port DATA is enabled/disabled by the CHIP SELECT terminal; its direction is controlled by the READ/WRITE terminal. When CHIP SELECT is high the serial port is disabled and the chip is not affected by changes in data at the DATA or CLOCK terminals.

There are five bits in the serial input port. D0 will be the last bit written to the serial port. Their functions are:

Serial Port Bit Definitions.

D0 - Sleep/Run Mode;
LOW = Sleep, HIGH = Run
This bit allows the A8901CLB to be powered down when not in use.

D1 - Step Mode;
LOW = Normal Operation,
HIGH = Step Only
When in the step-only mode the back-EMF detection circuitry is disabled and the power outputs are stepped through their normal commutation sequence by the start-up oscillator. This mode is intended to facilitate device and system testing.

D2 - Read Output Select;
LOW = Thermal Shutdown Status,
HIGH = Start-Up Oscillator.

D3 and D4 - These two bits set the maximum output current according to the following truth table:

D3	D4	I_{OUT}(MAX)
0	0	1 A
0	1	800 mA
1	0	600 mA
1	1	400 mA

Write Mode (READ/$\overline{\text{WRITE}}$ Low). To write data to the serial port, the READ/$\overline{\text{WRITE}}$ terminal and the CLOCK terminal should be low prior to the CHIP SELECT terminal going low. Once CHIP SELECT goes low, information on the DATA terminal is read into the shift register on the positive-going transition of the CLOCK. Data written into the serial port is latched and becomes active on the low-to-high transition of the CHIP SELECT terminal at the end of the write cycle.

Read Mode (READ/$\overline{\text{WRITE}}$ High). The transitions of the start-up oscillator or the status of the thermal shutdown of the A8901CLB can be read from the serial port DATA terminal. The choice between these two functions is selected by the D2 bit in the serial port's latches. To read data the READ/$\overline{\text{WRITE}}$ terminal must be high prior to CHIP SELECT going low. When CHIP SELECT goes low the DATA terminal will register the status of the selected function. If the status of the selected function is changing, the data output will reflect this as long chip select is held low and READ/$\overline{\text{WRITE}}$ is held high.

Thermal Shutdown Status: LOW = No Fault, HIGH = Fault

Oscillator: Each change represents a step to the next state in the six step output sequence.

The READ/$\overline{\text{WRITE}}$ terminal should be held high until the CHIP SELECT terminal has returned high to avoid erroneous data being written to the device.

Reset. The $\overline{\text{RESET}}$ terminal when pulled low clears all serial port bits, including the D0 latch, which puts the A8901CLB in the sleep mode.

Centertap. The A8901CLB internally simulates the centertap voltage of the motor. To obtain reliable start-up performance from motor to motor, the motor centertap should be connected to this terminal.

External Component Selection. Applications information is available from the factory for external component selection, frequency-locked loop speed control, and commutation delay capacitor selection.

TYPICAL APPLICATION