32Kx8 Bit Extended Voltage Operating Static RAM

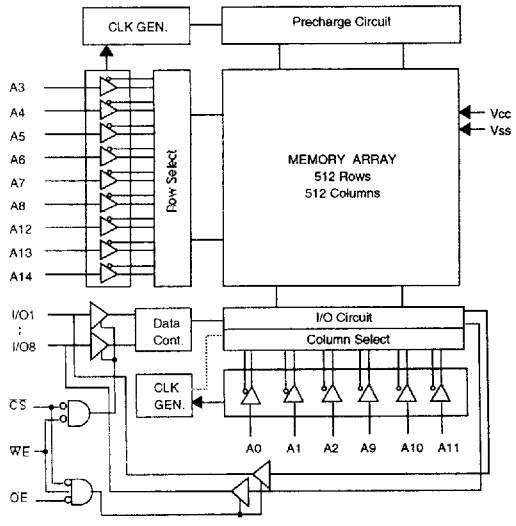
FEATURES

- Extended Operating Voltage : 3.0~5.5V
- Fast Access Time
  - 3.3V Operation : 100ns (Max.)
  - 5V Operation : 70ns (Max.)
- Low Power Dissipation Standby / Operating
  - 3.3V Operation: 13.2μW / 66mW (Typ.)
  - 5V Operation : 50μW / 275mW (Typ.)
- TTL compatible inputs and outputs
- Fully Static Operation
  - No clock or refresh required
- Three state Outputs
- Standard Pin Configuration
  KM62256CLG-LV : 28-pin SOP(450 mil)
  KM62256CLTG-LV : 28-PinTSOP(Standard)
  KM62256CLRG-LV : 28-PinTSOP(Reverse)

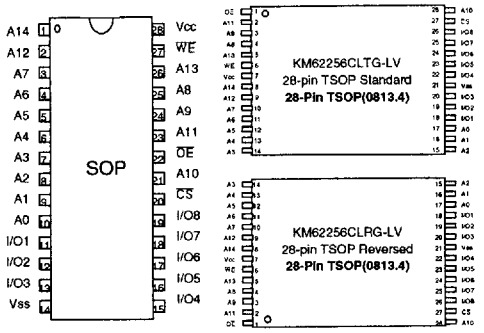
GENERAL DESCRIPTION

The KM62256CL-LV is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits.
The device is fabricated using Samsung's advanced CMOS process and high-speed circuit technology.
The KM62256CL-LV has an output enable input for precise control of the data outputs.
It also has a chip enable input for the minimum current power down mode.
The KM62256CL-LV is particularly well suited for use in low voltage (3.0~5.5V) operation and battery back-up applications.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(TOP VIEW)*



Pin Name	Pin Function
A_0-A_{14}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O_1~I/O_8	Data Inputs/Outputs
V_{CC}	Power(3.0 ~ 5.5V)
V_{SS}	Ground

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ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5 to Vcc+0.5	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	T_{solder}	260°C, 10sec (Lead Only)	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	3.0	3.3	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5	V
Input Low Voltage	V_{IL}	-0.3 *	-	0.4	V

* V_{IL}(Min.)= -3.0V for ≤50 ns Pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, unless otherwise specified)

Item	Symbol	Test Condition	Vcc=3.3V±0.3			Vcc=5V±0.5			Unit
			Min.	*Typ.	Max.	Min.	**Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc	-1		1	-1		1	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=Vss to Vcc	-1		1	-1		1	μA
DC Operating Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}, $I_{I/O}$=0mA	-	1.0	2.0	-	4	15	mA
Average Operating Current	I_{CC1}	Cycle Time=1μs, 100%Duty $\overline{CS}$≤0.2V, V_{IH}≥Vcc-0.2V V_{IL}≤0.2V, $I_{I/O}$=0mA	-	2.5	5	-	5	7	mA
	I_{CC2}	Min Cycle, 100% Duty, $\overline{CS}$=V_{IL} V_{IN}=V_{IL} or V_{IH}, $I_{I/O}$=0mA	-	25	30	-	55	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	-		0.3	-		1	mA
	I_{SB1}	$\overline{CS}$≥Vcc-0.2V V_{IN}≥Vcc-0.2V or V_{IN}≤0.2V	-	1.5	10	-	2	20	μA
Output Low Voltage	V_{OL}	Iol=2.1 mA			0.4			0.4	V
Output High Voltage	V_{OH}	Ioh=-1.0 mA	2.2			2.4			V

* Typ; Vcc=3.3V, Ta=25°C ** Typ; Vcc=5V, Ta=25°C

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CAPACITANCE *(f=1MHz, T_A=25 °C)

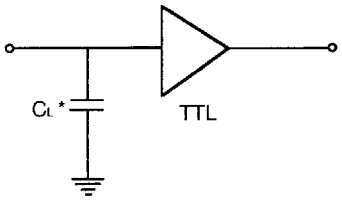
Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS

(T_A=0 to 70 °C, V_{CC}=3.3V±0.3, unless otherwise specified.)

Parameter	Value	
	Vcc=3.3V	Vcc=5.0V
Input Pulse Level	2.2 to 0.4V	2.4 to 0.8V
Input Rise and Fall Time	5 ns	5 ns
Input and Output Timing Reference Levels	1.5V	1.5V
Output Load	C_L=100pF+1TTL	C_L=100pF+1TTL



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	Vcc=3.3V± 0.3		Vcc=5.0V± 0.5		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	100		70	-	ns
Address Access Time	t_{AA}	-	100	-	70	ns
Chip Select to Output	t_{CO}	-	100	-	70	ns
Output Enable to Valid Output	t_{OE}	-	50	-	35	ns
Chip Select to Low-Z Output	t_{LZ}	10	-	10	-	ns
Output Enable to Low-Z Output	t_{OLZ}	5	-	5	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	35	0	30	ns
Output Disable to High-Z Output	t_{OHZ}	0	35	0	30	ns
Output Hold from Address Change	t_{OH}	15	-	5	-	ns

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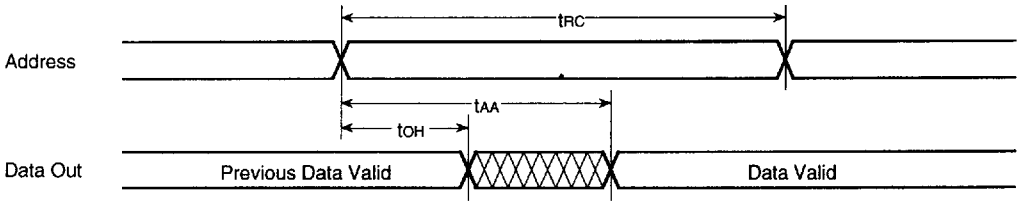
WRITE CYCLE

Farameter	Symbol	Vcc=3.3V± 0.3		Vcc=5.0V± 0.5		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	tWC	100	-	70	-	ns
Chip Select to End of Write	tCW	70	-	60	-	ns
Address Valid to End of Write	tAW	70	-	60	-	ns
Address Set-up Time	tAS	0	-	0	-	ns
Write Pulse Width	tWP	60	-	50	-	ns
Write Recovery Time	tWR	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	30	0	25	ns
Data to Write Time Overlap	tDW	50	-	30	-	ns
Data Hold from Write Time	tDH	0	-	0	-	ns
End Write to Output Low-Z	tOW	10	-	5	-	ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



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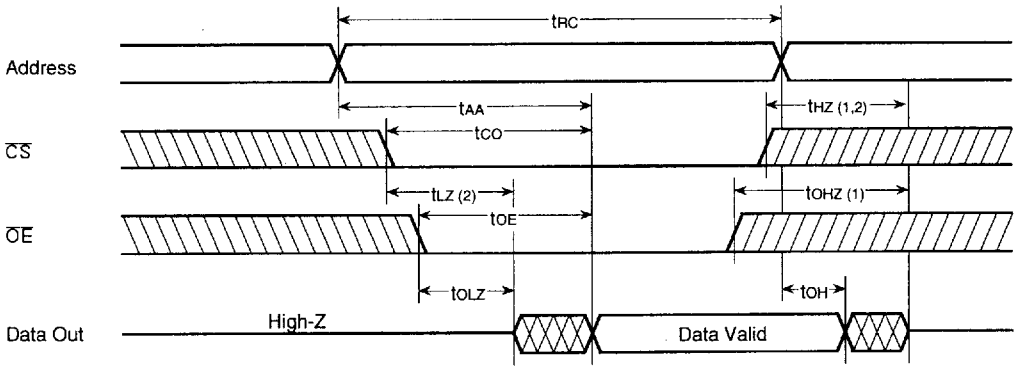
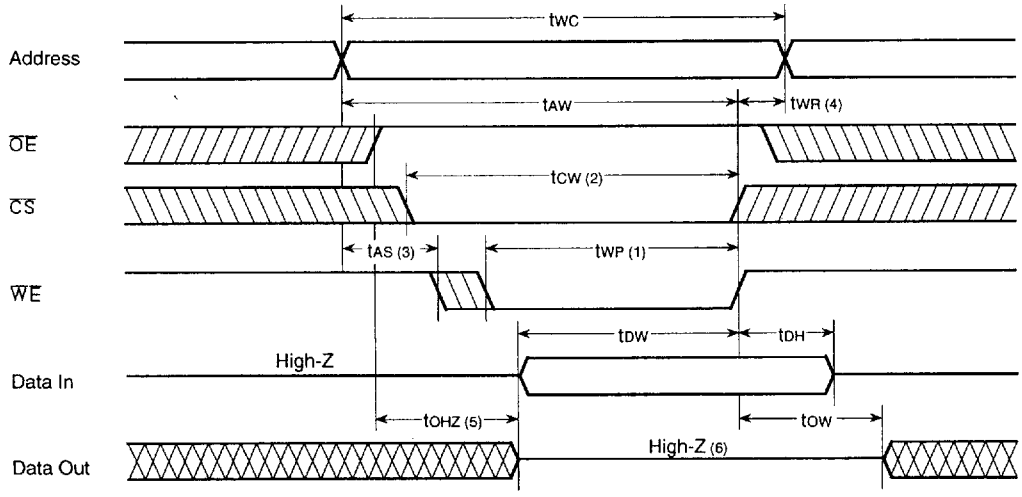
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES (READ CYCLE)

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are referenced to the VOH or VOL.
2. At any given temperature and voltage condition tHZ(max) is less than tLZ(min) both for a given device and from device to device.
3. $\overline{WE}$ is high for read cycle.
4. Address valid prior to or coincident with $\overline{CS}$ transition Low.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



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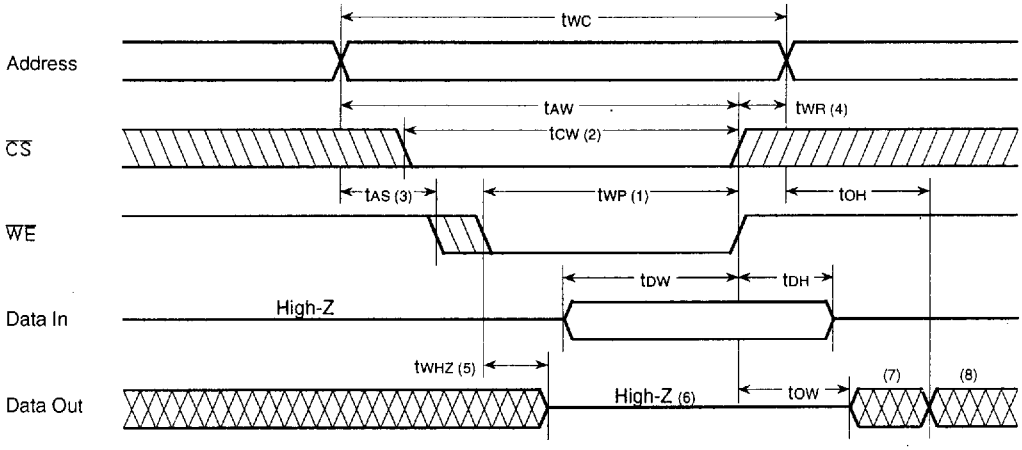
TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ Fixed)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(tWP) of a low $\overline{CS}$ and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low : A write end at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high, tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of $\overline{CS}$ going low to end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change.
5. If $\overline{OE}$,$\overline{WE}$ are in the read mode during this period, the I/O pins are in the outputs Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
7. Dout is the same phase of the latest written data in this write cycle
8. Dout is the read data of new address

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Vcc Current
H	X	X	Power down	High-Z	ISB, ISB1
L	H	H	Output Disable	High-Z	ICC
L	H	L	Read	DOUT	ICC
L	L	X	Write	DIN	ICC

Note : X means Don't Care.

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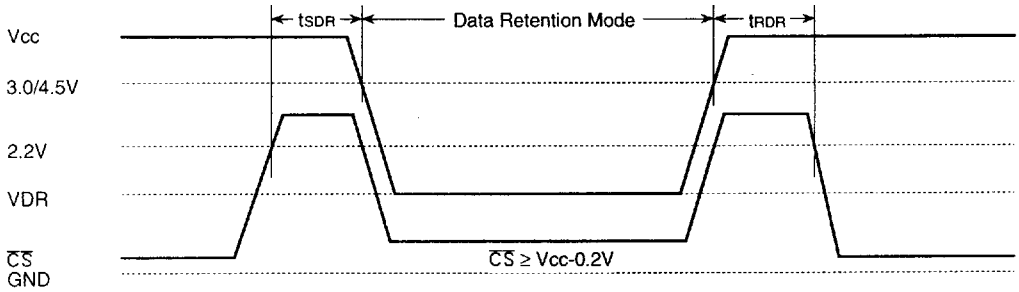
DATA RETENTION CHARACTERISTICS (Ta= 0 to 70 °C)

PARAMETER	SYMBOL	TEST CONDITION	MIN	*TYP	MAX	UNIT
Vcc for Data Retention	Vdr	$\overline{CS}$≥Vcc-0.2V	2.0		5.5	V
Data Retention Current	Idr	Vcc=3.0V $\overline{CS}$≥VCC-0.2V		2*	10	µA
Data Retention Set-up Time	tSDR	See Data Retention	0			ns
Recovery Time	tRDR	Waveforms (below)	5			ms

* Vcc=5.0V, TA=25°C

DATA RETENTION WAVEFORM 1 ($\overline{CS}$ Controlled)



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