

8 K x 8 / 3.3 Volts High Speed CMOS SRAM

Description

The L 65764 is a high speed CMOS static RAM organized as 8192×8 bits. It is manufactured using MHS high performance CMOS technology.

Access times as fast as 25 ns are available with maximum power consumption of only 216 mW.

The L 65764 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 73 % when the circuit is deselected.

Easy memory expansion is provided by active low chip select ($\overline{CS1}$), an active high chip select (CS2), an active low output enable (\overline{OE}) and three state drivers.

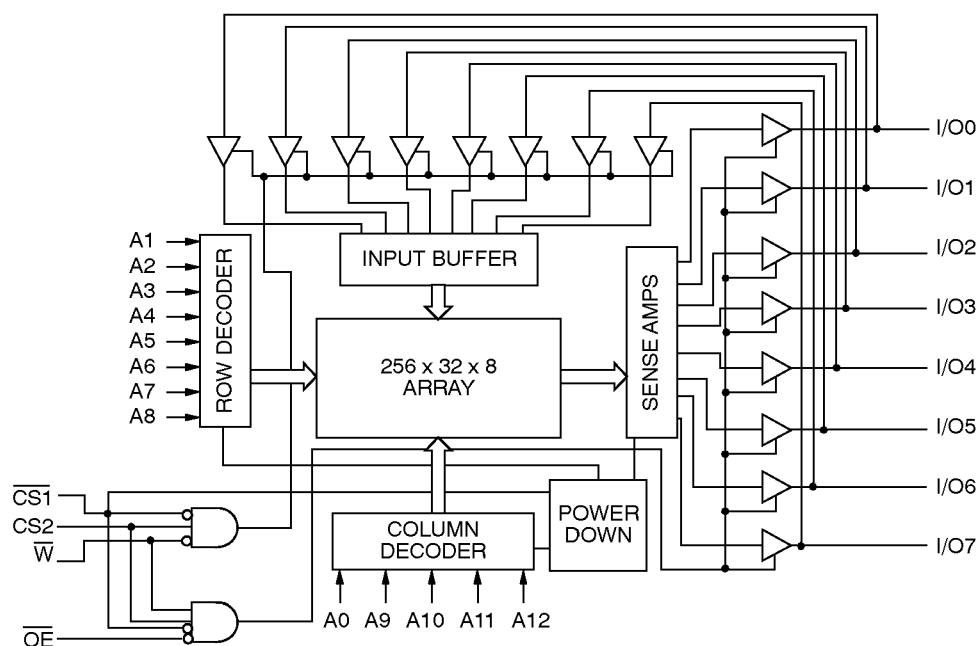
L 65764 provides fast access time with 3,3 volts power supply, perfectly designed for portable applications (PC cache memory... etc).

Features

- Single supply 3.3 V \pm 0.3 V
- Fast access time
Commercial : 25/35/45/55 ns (max)
- Low power consumption
Active : 216 mW (typ)
Standby : 36 mW (typ)
- 300 and 600 mils width package
- Asynchronous
- Capable of withstanding greater than 2000 V electrostatic discharge

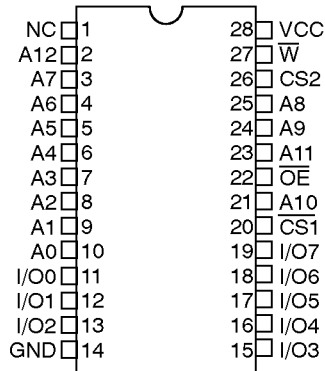
Interface

Block Diagram



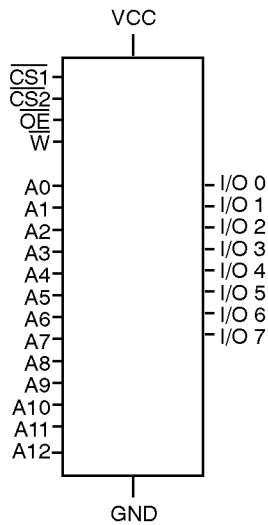
Pin Configuration

SOIC & SOJ 300 mils, 28 pins, DIL.
 SOIC 330 mils, 28 pins
 Plastic 300 & 600 mils, 28 pins, DIL
 Ceramic 300 mils, 600 mils, 28 pins, DIL



Pinout DIL/SOIC/SOJ 28 pins (top view)

Logic Symbol



Pin Names

A0-A13	: Address inputs	$\overline{CS1}$: Chip-select 1
I/O0-I/O7	: Inputs/Outputs	$\overline{CS2}$: Chip-select 2
VCC	: Power	\overline{OE}	: Output enable
GND	: Ground	\overline{W}	: Write enable

Truth Table

$\overline{CS1}$	$\overline{CS2}$	\overline{OE}	\overline{W}	DATA-IN	DATA-OUT	MODE
H	X	X	X	Z	Z	Deselect
L	H	L	H	Z	Valid	Read
L	H	X	L	Valid	Z	Write
L	H	H	H	Z	Z	Output disable

L = Low - H = High - X = H or L - Z = High impedance.

Electrical Characteristics

Absolute Maximum Ratings

Supply voltage to GND potential : -0.5 V to +7.0 V Storage temperature : -65°C to +150°C
 DC input voltage : -3.0 V to +7.0 V Output current into outputs (low) : 20 mA
 DC output voltage in high Z state : -0.5 V to +7.0 V Electro Static Discharge Voltage > 2000 V
 (MIL STD 883C METHOD 3015-2)

Operating Range

	OPERATING VOLTAGE	OPERATING TEMPERATURE
Commercial	3.3 V ± 0.3 V	0°C to +70°C

Recommended DC Operating Conditions

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply Voltage	3	3.3	3.6	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	-0.3	0.0	0.7	V
VIH	Input high voltage	1.4	-	VCC	V

Capacitance

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin (1)	Input capacitance	-	-	5	pF
Cout (1)	Output capacitance	-	-	7	pF

Note : 1. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not tested.

Electrical Characteristics DC Parameters

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX (2)	Input leakage current	-10.0	-	10.0	µA
IOZ (3)	Output leakage current	-10.0	-	10.0	µA
IOS (3)	Output short circuit current	-	-	-300.0	mA
VOL (4)	Output low voltage	-	-	0.4	V
VOH (5)	Output high voltage	1.8	-	-	V

Note : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
 3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds.
 Not more than 1 output should be shorted at one time.
 4. Vcc min, IOL = 4.0 mA.
 5. Vcc min, IOH = -0.25 mA.

Consumption for Commercial Specification (-5)

SYMBOL	PARAMETER	L 65764 - 25	L 65764 - 35	L 65764 - 45	L 65764 - 55	UNIT	VALUE
ICCSB (6)	Standby supply current	10	10	10	10	mA	max
ICCSB1 (7)	Standby supply current	5	5	5	5	mA	max
ICCOP (8)	Dynamic operating current	60	60	60	60	mA	max

AC Parameters

AC Conditions

Input pulse levels : Gnd to 3.0 V Input timing reference levels : 1.5 V
 Input rise : 10 ns Output loading IOL/IOH (see figure 1a and 1b): +30 pF

AC Test Loads and Waveforms

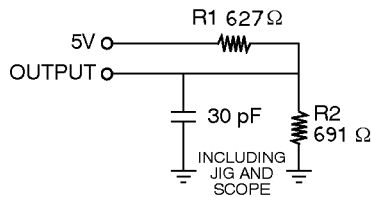


Figure 1
a

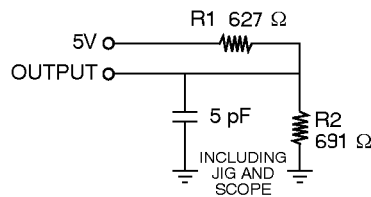


Figure 1 b

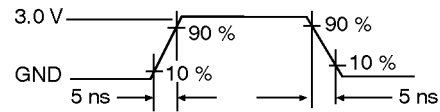
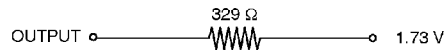


Figure 2

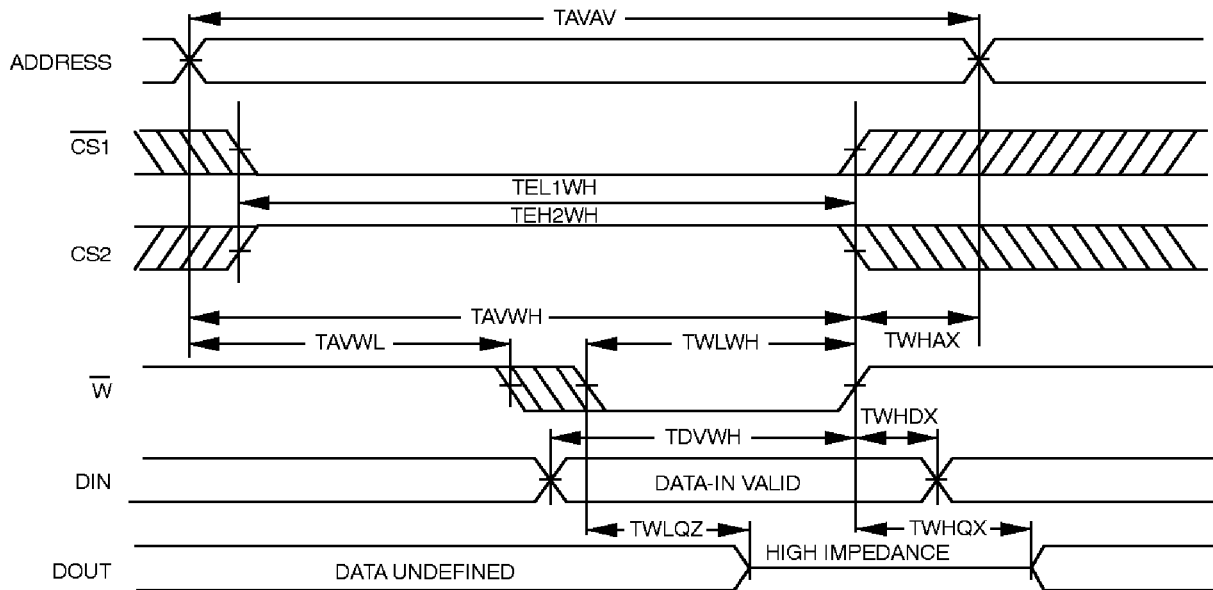
Equivalent to : THEVENIN EQUIVALENT



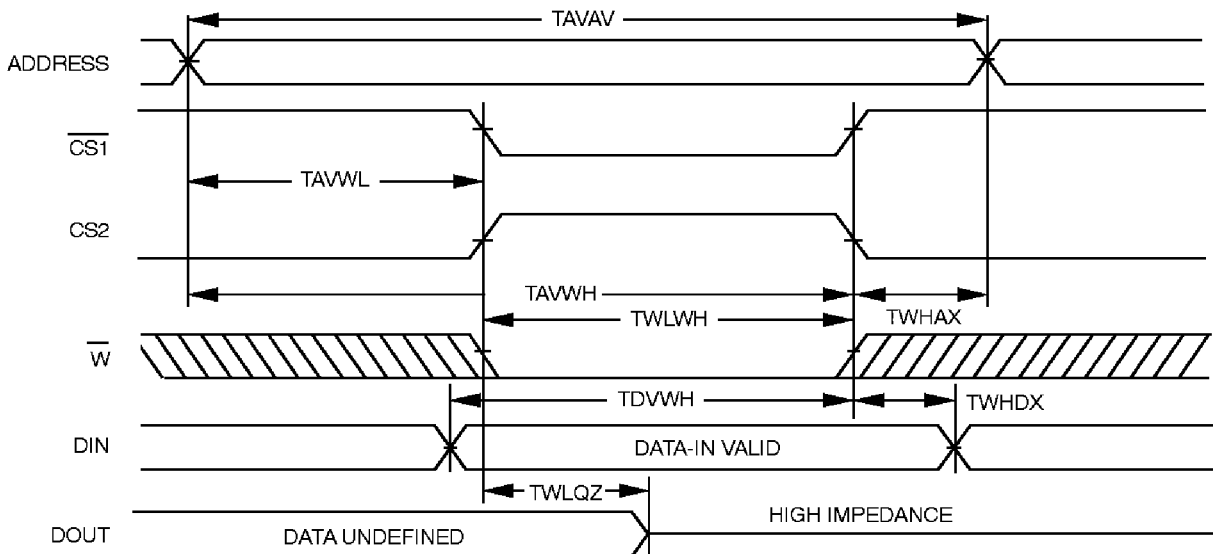
Write Cycle : Commercial Specification

SYMBOL	PARAMETER	L 65764 - 25	L 65764 - 35	L 65764 - 45	L 65764 - 55	UNIT	VALUE
TAVAV	Write cycle time	25	35	45	50	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end write	20	25	30	40	ns	min
TDVWH	Data set-up time	17	20	20	25	ns	min
TEL1WH	$\overline{CS1}$ low to write end	20	25	30	40	ns	min
TEH2WH	CS2 high to write end	20	20	25	30	ns	min
TWLQZ(9)	Write low to high Z	12	12	15	20	ns	max
TWLWH	Write pulse width	20	20	20	25	ns	min
TWHAX	Address hold from end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (8, 9)	Write high to low Z	5	5	5	5	ns	min

Write Cycle 1 \overline{W} Controlled (note 9)



Write Cycle 2 $\overline{CS1}$ controlled (note 9)

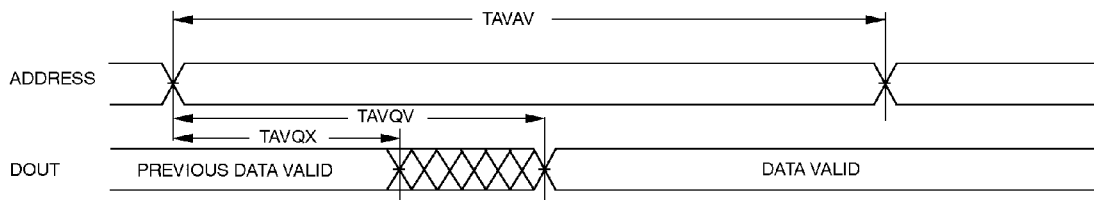


Note : 9. The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write. Data out is HIGH impedance if $\overline{OE} = V_{IH}$.

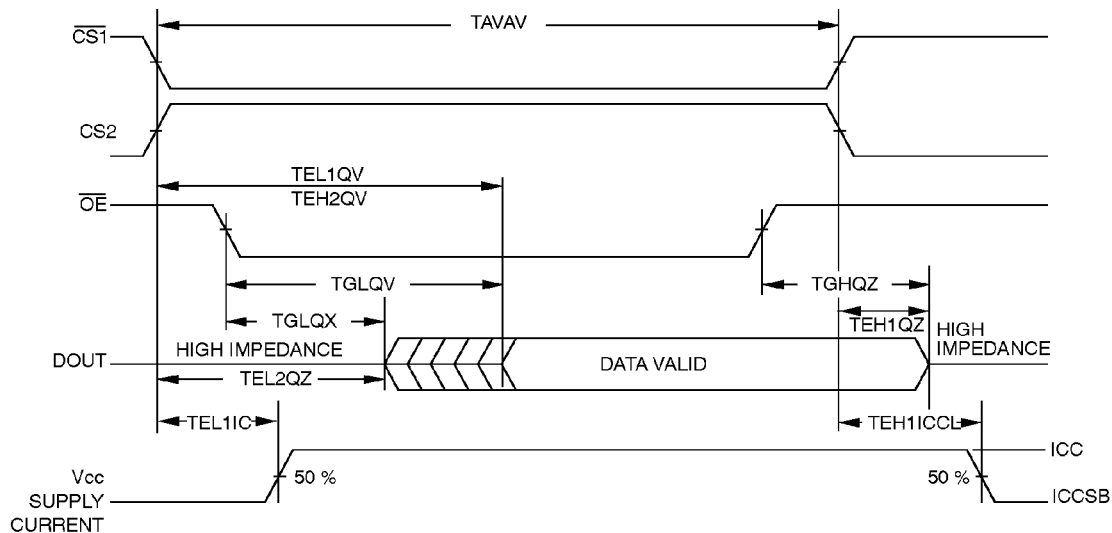
Read Cycle : Commercial Specification

SYMBOL	PARAMETER	L 65764 - 25	L 65764 - 35	L 65764 - 45	L 65764 - 55	UNIT	VALUE
TAVAV	READ cycle time	25	35	45	55	ns	min
TAVQV	Address access time	25	35	45	55	ns	max
TAVQX	Address valid to low Z	5	5	5	5	ns	min
TEL1QV	Chip-select 1 access time	25	35	45	55	ns	max
TEH2QV	Chip-select 2 access time	20	25	30	40	ns	max
TEL1QX	$\overline{CS1}$ low to low Z	5	5	5	5	ns	min
TEH2QX	CS2 high to high Z	3	3	3	3	ns	min
TEH1QZ (11)	$\overline{CS1}$ high to high Z	10	15	15	20	ns	max
TEL2QZ (11)	CS2 low to high Z	10	15	15	20	ns	max
TEL1IC	$\overline{CS1}$ low to power up	0	0	0	0	ns	min
TEH1ICCL	CS1 high to power down	20	20	25	25	ns	max
TGLQV	Output enable access time	20	20	25	25	ns	max
TGLQX	\overline{OE} low to low Z	5	5	5	5	ns	min
TGHQZ	\overline{OE} high to high Z	10	12	15	20	ns	max

Read Cycle nb 1 (notes 10, 11)

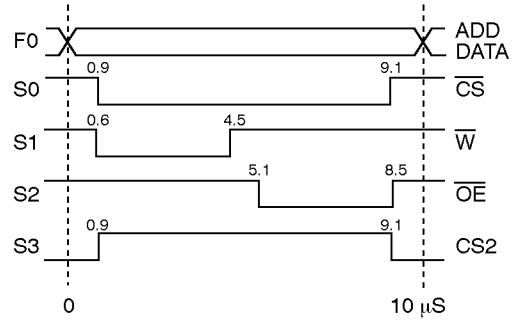
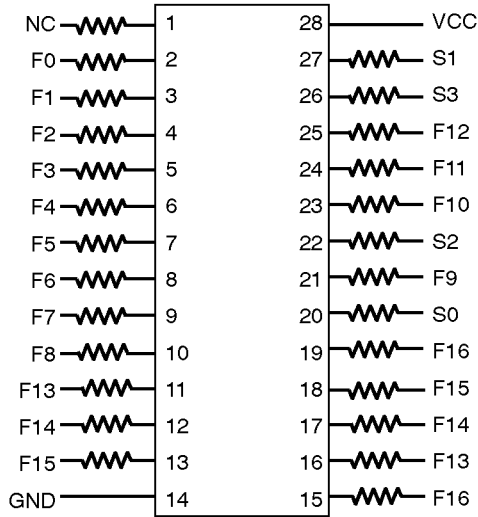


Read Cycle nb 2 (notes 10, 12)



- Notes :**
- \overline{W} is HIGH for read cycle.
 - Device is continuously selected. $\overline{CS1}$ & $\overline{OE} = VIL$ and $CS2 = VIH$.
 - Address valid prior to or coincident with $\overline{CS1}$ transition LOW.

Burn-In Schematics



VCC = 5 V (-0, +0.5)

R = 1 KΩ per pin

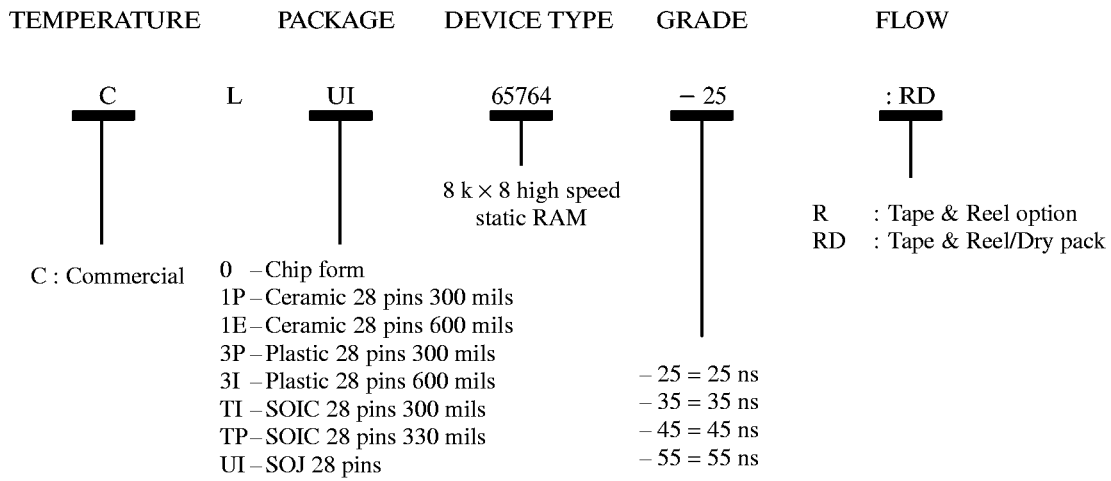
FO = 50 KHz ± 20 %

F_n = 1/2 F_{n-1}

S0 to S3 : programmable signals for write/read cycles

NC = Not connected

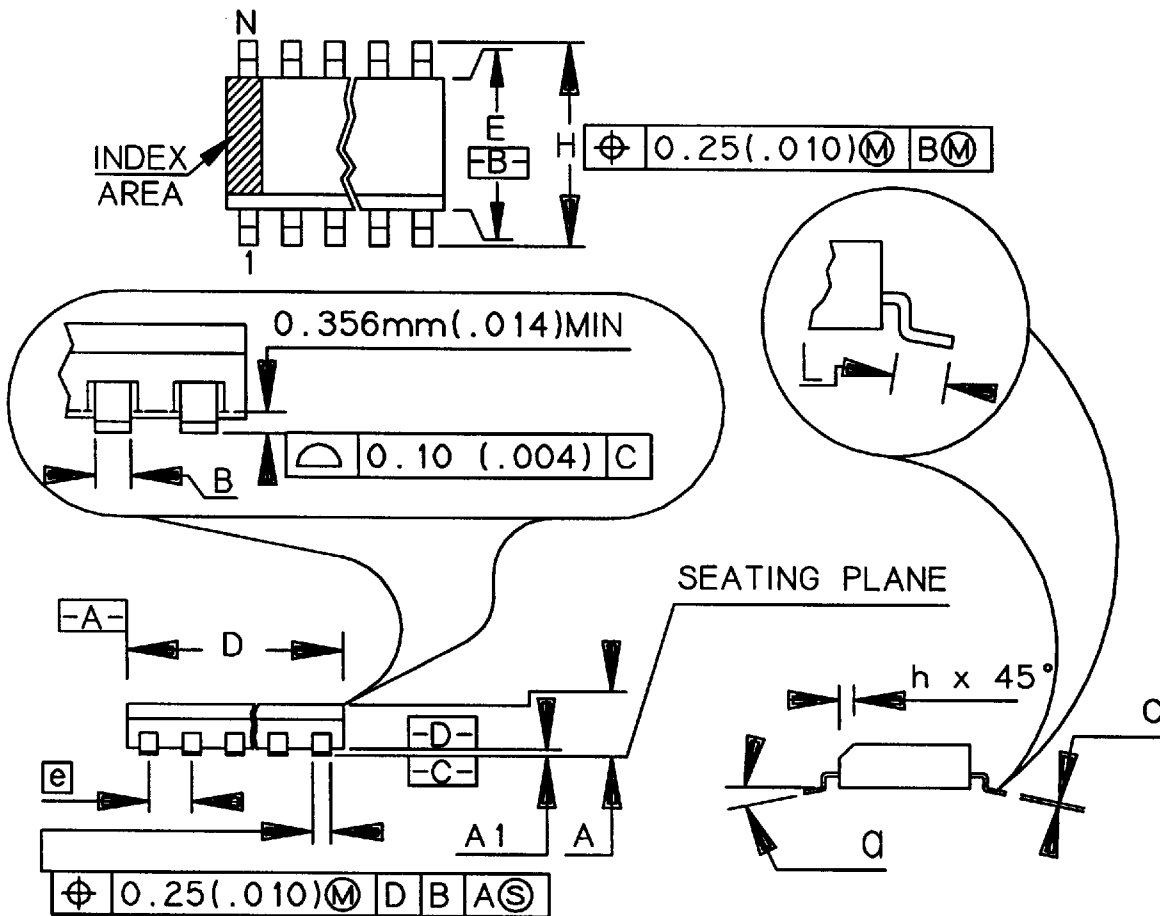
Ordering Information



Temp. range	Packages	Access Time (ns)					Std process 65764
		20 (F)	25 (H)	35 (K)	45 (M)	55 (N)	
							Mil flows (including SMD5962-38294)
M	1 1E 4 0	1 1 1 X	1 1 1 X	1 1 1 X	1 1 1 X	1 1 1 1	1 1 1 1

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28 PINS SO .300

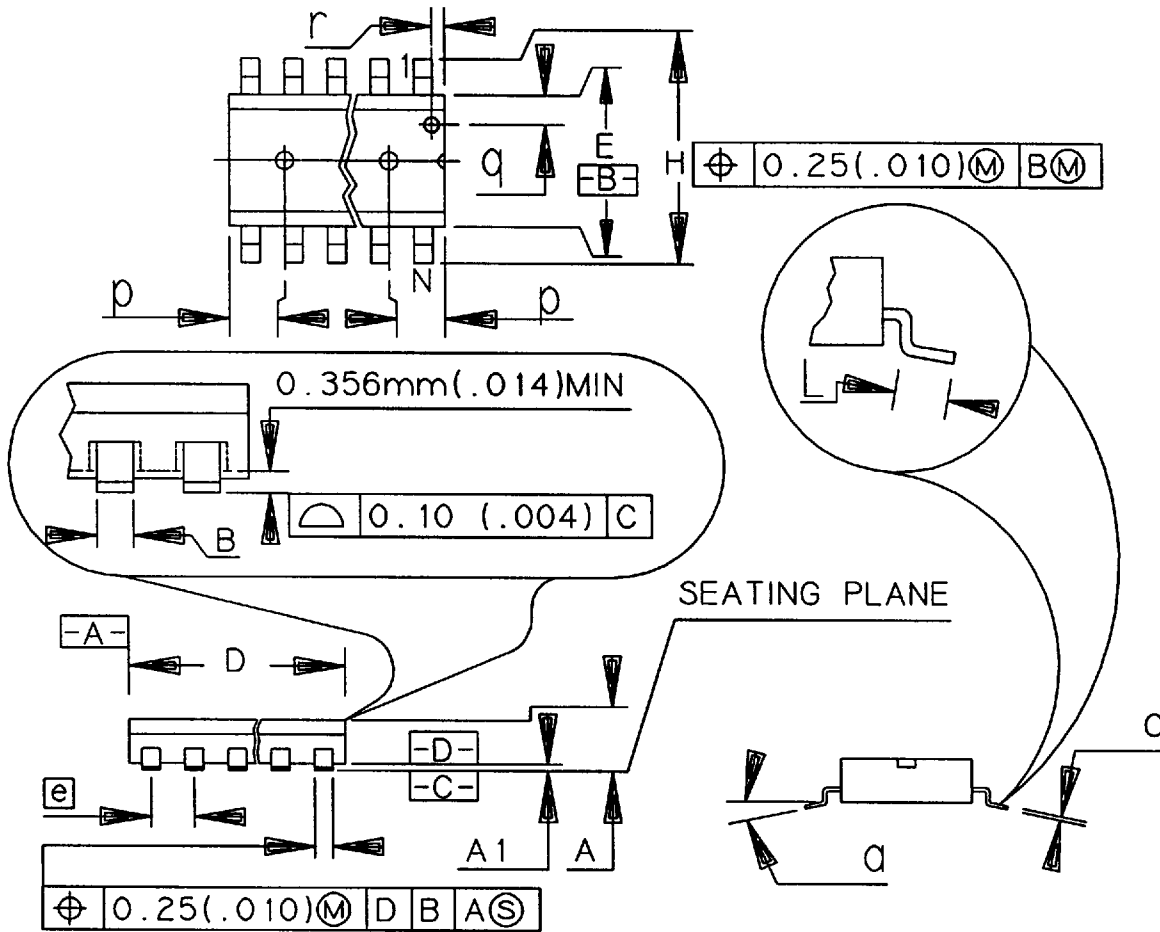


	MM		INCH	
A	2.35	2.65	.093	.104
A1	0.10	0.30	.004	.012
B	0.35	0.49	.014	.019
C	0.23	0.32	.009	.013
D	17.70	18.10	.697	.713
E	7.40	7.60	.291	.299
e	1.27	BSC	.050	BSC
H	10.00	10.65	.394	.419
h	0.25	0.75	.010	.029
L	0.40	1.27	.016	.050
N	28		28	
a	0°		8°	

CODE : TI

REV :K DATE : 05-10-95

28 PINS SO .330 MIL BODY

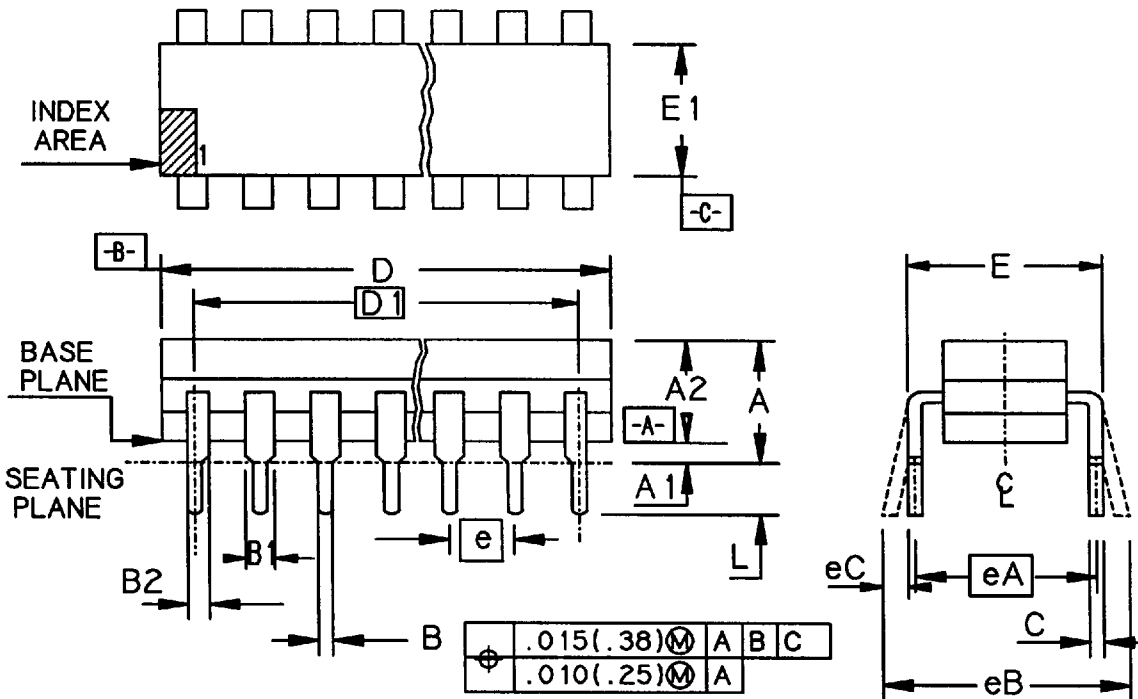


	MM		INCH	
A	2.39	2.79	.094	.110
A1	0.05	0.35	.002	.014
B	0.35	0.50	.014	.020
c	0.20	0.30	.008	.012
D	18.29	18.49	.720	.728
E	8.58	8.79	.338	.346
e	1.27	TYP	.050	TYP
H	11.68	12.19	.460	.480
L	0.76	1.27	.030	.050
N	28		28	
p	2.54		.100	
q	1.90	DIA	.075	DIA
r	1.78	DIA	.070	DIA
a	0°		8°	

CODE : TP

REV : C | DATE : 07-06-91

28 PINS PLASTIC .300



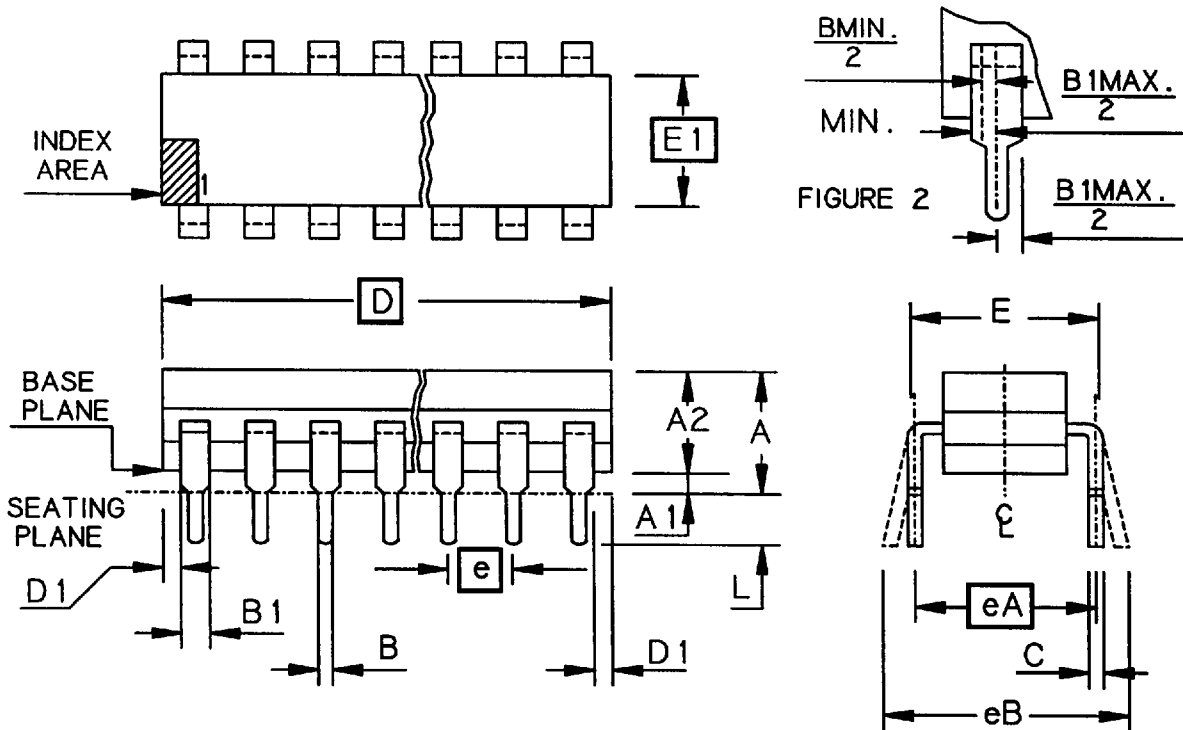
	MM		INCH	
A	-	4.57	-	.180
A1	0.38	-	.015	-
A2	3.05	3.81	.120	.150
B	0.36	0.56	.014	.022
B1	1.14	1.52	.045	.060
B2	0.76	1.14	.030	.045
C	0.20	0.38	.008	.015
D	34.16	35.18	1.345	1.385
D1	33.02 BSC		1.300 BSC	
E	7.62	8.26	.300	.325
E1	6.99	7.49	.275	.295
e	2.54	BSC	.100	BSC
eA	7.62	BSC	.300	BSC
eB	-	10.92	-	.430
eC	0.00	1.52	.000	.060
L	2.79	3.81	.110	.150

COMPLIANT JEDEC MO-095 ISSUE A

CODE : 3P

REV : E | DATE : 16-06-94

28 PINS PLASTIC .600



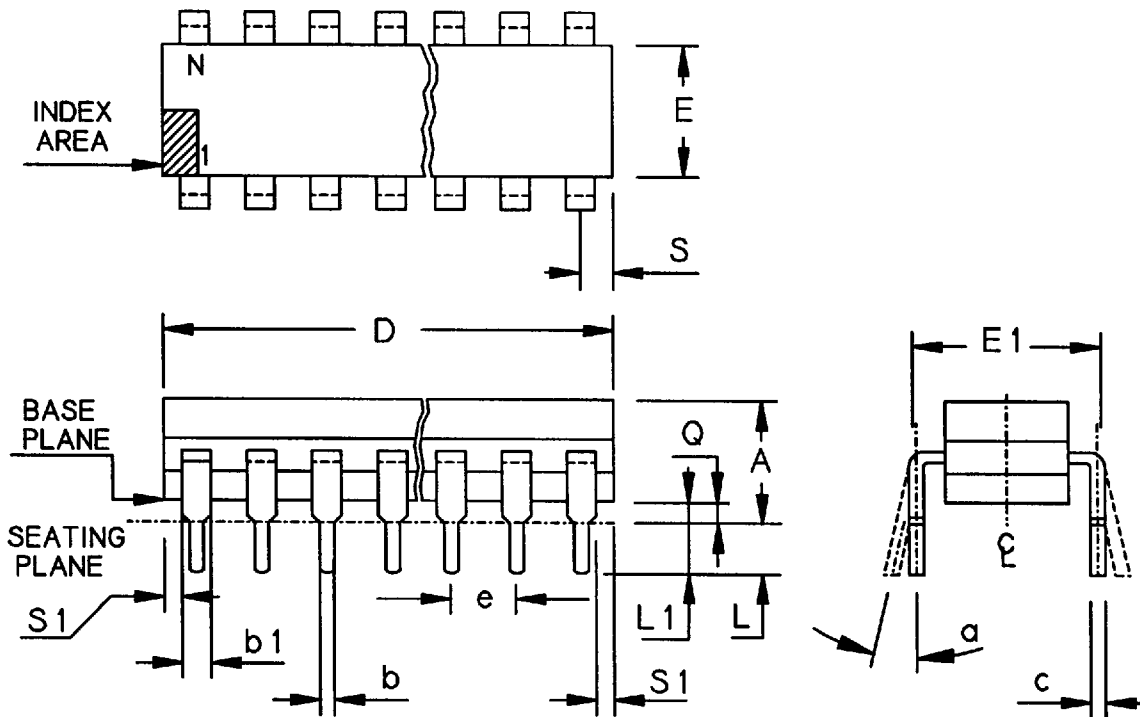
	MM		INCH	
A	-	6.35	-	.250
A1	0.38	-	.015	-
A2	3.18	4.95	.125	.195
B	0.36	0.56	.014	.022
B1	0.76	1.78	.030	.070
C	0.20	0.38	.008	.015
D	35.05	39.75	1.380	1.565
E	15.24	15.87	.600	.625
E1	12.32	14.73	.485	.580
e	2.54	B.S.C	.100	B.S.C
eA	15.24	B.S.C	.600	B.S.C
eB	-	17.78	-	.700
L	2.93	5.08	.115	.200
D1	0.13	-	.005	-
PKG STD		02		

CODE : 31

022 025 074 077

REV : H | DATE : 03-08-95

28 LEADS CERDIP .300



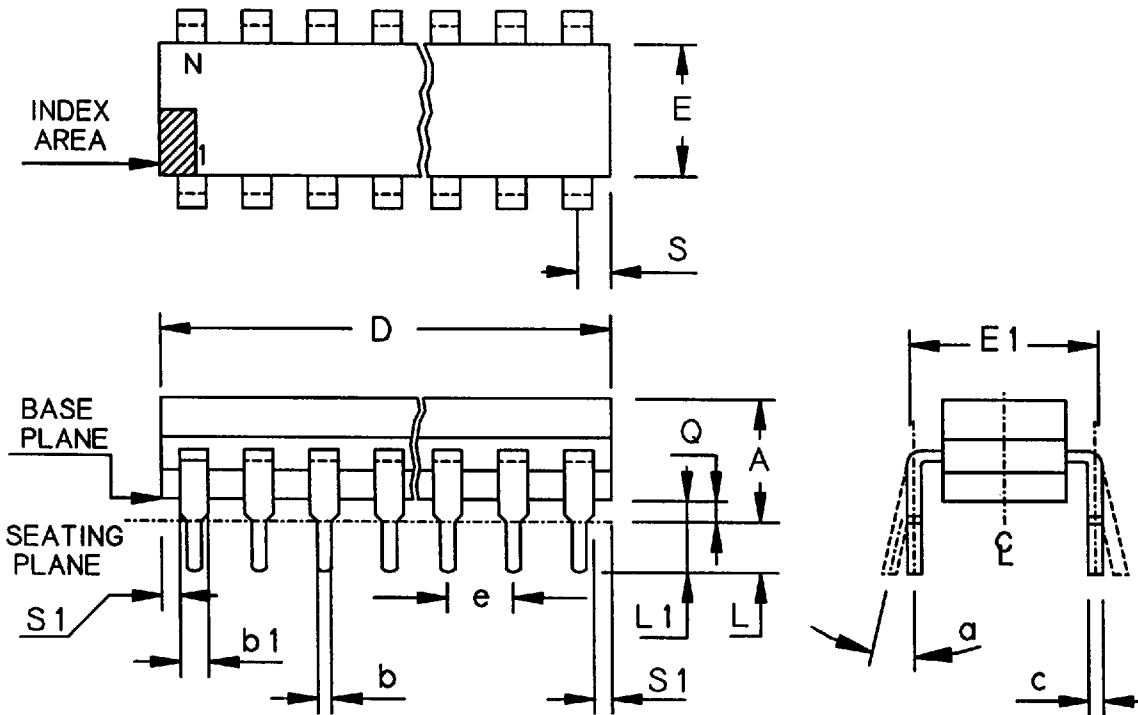
	MM		INCH	
	min	max	min	max
A	3.30	5.84	.130	.230
b	0.36	0.58	.014	.023
b1	0.96	1.65	.038	.065
c	0.20	0.38	.008	.015
D	-	37.72	-	1.485
E	6.10	7.87	.240	.310
E1	7.36	8.13	.290	.320
e	2.54 B.S.C		.100 B.S.C	
L	2.92	5.08	.115	.200
L1	3.30	-	.130	-
Q	0.38	2.54	.015	.100
S	-	2.54	-	.100
S1	0.13	-	.005	-
a	0° - 15°		0° - 15°	
N	28			

COMPLIANT MIL-M-38510H (D-15).

CODE : 1P

REV : D DATE : 29-06-94

28 LEADS CERDIP .600



	MM		INCH	
	min	max	min	max
A	-	5.89	-	.232
b	0.36	0.58	.014	.023
b1	0.96	1.65	.038	.065
c	0.20	0.38	.008	.015
D	-	37.85	-	1.490
E	12.70	15.49	.500	.610
E1	14.99	15.75	.590	.620
e	2.54 B.S.C		.100 B.S.C	
L	3.18	5.08	.125	.200
L1	3.81	-	.150	-
Q	0.38	1.52	.015	.060
S	-	2.54	-	.100
S1	0.13	-	.005	-
a	0° - 15°		0° - 15°	
N	28			

COMPLIANT MIL-M-38510H (D-10)

CODE : 11

REV : 1 | DATE : 04-10-94