LF155/LF156

Monolithic JFET Input Operational Amplifiers

DISTINCTIVE CHARACTERISTICS

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance – very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- Internal compensation and large differential input voltage capability

GENERAL DESCRIPTION

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors. These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

The LF155, LF156 series are direct replacements for National LF155, LF156 series.

COMMON FEATURES
(LF155A, LF156A)

Low input bias current	30pA
Low input offset current	3.0pA
High input impedance	$10^{12}\Omega$
Low input offset voltage	1.0mV
Low input offset voltage temperature drift	3.0μV/°C
Low input noise current	0.01pA/√Hz
High common-mode rejection ratio	100dB
Large dc voltage gain	106dB

APPLICATIONS

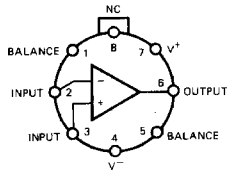
- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

UNCOMMON FEATURES

	LF155A	LF156A	Units
Extremely fast settling time to 0.01%	4.0	1.5	μs
Fast slew rate	5.0	12	V/μs
Wide gain bandwidth	2.5	5.0	MHz
Low input noise voltage	20	12	nV/√Hz

CONNECTION DIAGRAM
Top View

Metal Can
H-8-1



Note: 1. Pin 4 is connected to case.

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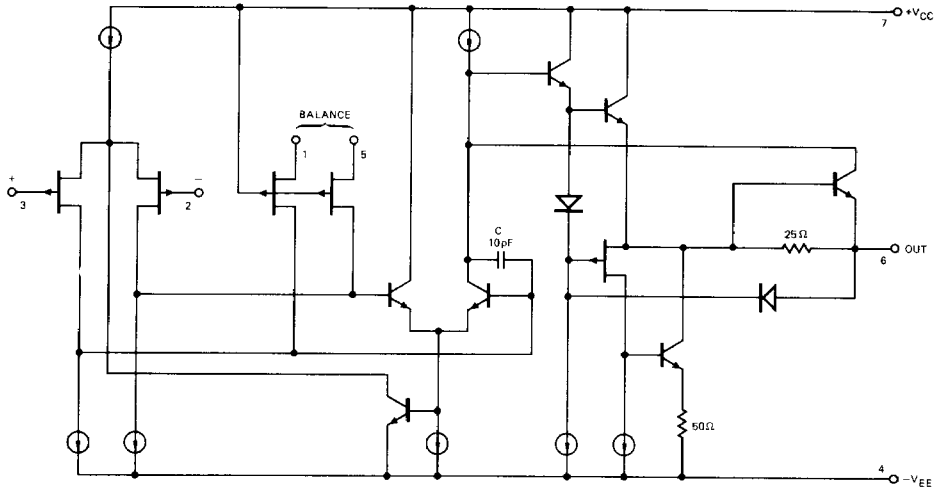
ORDERING INFORMATION*

Part Number	Package Type	Temperature Range	Order Number
LF355	Metal Can	0°C to +70°C	LF355H
	Dice	0°C to +70°C	LD355
LF255	Metal Can	−25°C to +85°C	LF255H
LF155	Metal Can	−55°C to +125°C	LF155H
	Dice	−55°C to +125°C	LD155
LF355A	Metal Can	0°C to +70°C	LF355AH
	Dice	0°C to +70°C	LD355A
LF155A	Metal Can	−55°C to +125°C	LF155AH
	Dice	−55°C to +125°C	LD155A
LF356	Metal Can	0°C to +70°C	LF356H
	Dice	0°C to +70°C	LD356
LF256	Metal Can	−25°C to +85°C	LF256H
LF156	Metal Can	−55°C to +125°C	LF156H
	Dice	−55°C to +125°C	LD156
LF356A	Metal Can	0°C to +70°C	LF356AH
	Dice	0°C to +70°C	LD356A
LF156A	Metal Can	−55°C to +125°C	LF156AH
	Dice	−55°C to +125°C	LD156A

*Also available with burn-in processing. To order, add suffix B to part number.

SIMPLIFIED SCHEMATIC



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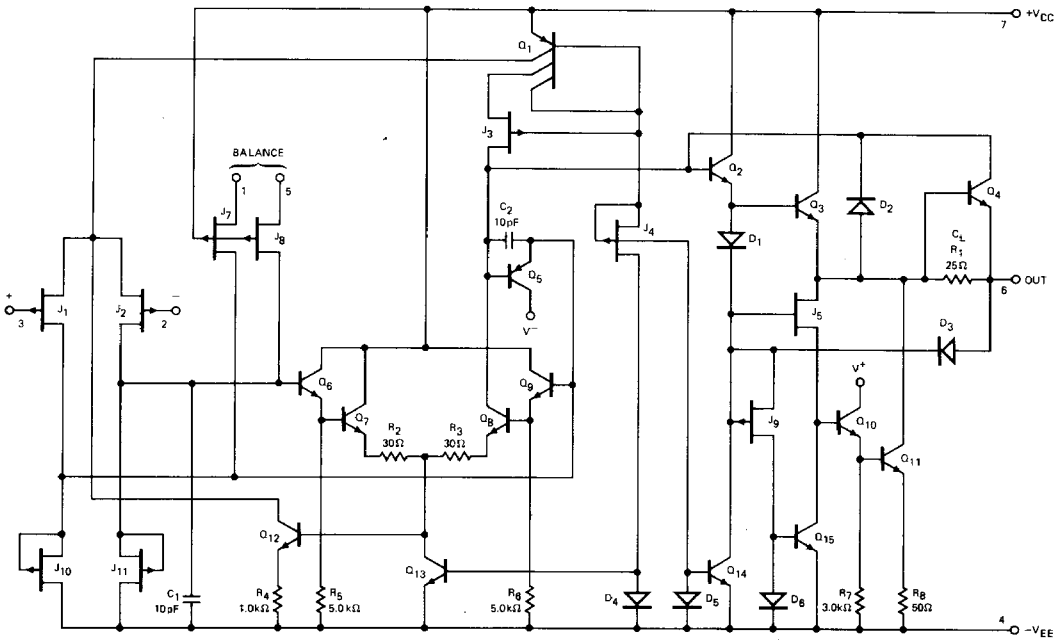
DETAILED SCHEMATIC



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LF155/LF156
ABSOLUTE MAXIMUM RATINGS

	LF155A/6A	LF155/6	LF355A/6A	LF355/6
Supply Voltage	±22V	±22V	±22V	±18V
Power Dissipation (Note 1) TO-99 (H Package)	670mW	670mW	570mW	500mW
Operating Temperature Range	−55°C to +125°C	−55°C to +125°C	−25°C to +85°C	0°C to +70°C
T_J(Max.)	150°C	150°C	115°C	100°C
Differential Input Voltage	±40V	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±20V	±16V
Output Short Circuit Duration	Continous	Continuous	Continuous	Continuous
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C	300°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Note 3)
DC CHARACTERISTICS

Parameters	Description	Test Conditions	LF155A/6A Min.	LF155A/6A Typ.	LF155A/6A Max.	LF355A/6A Min.	LF355A/6A Typ.	LF355A/6A Max.	Units
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$		1.0	2.0		1.0	2.0	mV
		Over Temperature			2.5			2.3	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		3.0			3.0		µV/°C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5		µV/°C per mV
I_{OS}	Input Offset Current	$T_J = 25°C$, (Note 3, 5)		3.0	10		3.0	10	pA
		$T_J \leq T_{HIGH}$			10			1.0	nA
I_B	Input Bias Current	$T_J = 25°C$, (Notes 3, 5)		30	50		30	50	pA
		$T_J < T_{HIGH}$			25			5.0	nA
R_{IN}	Input Resistance	$T_J = 25°C$		10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm15V$, $T_A = 25°C$	50	200		50	200		V/mV
		$V_O = \pm10V$, $R_L = 2k\Omega$ Over Temperature	25			25			V/mV
V_O	Output Voltage Swing	$V_S = \pm15V$, $R_L = 10k\Omega$	±12	±13		±12	±13		Volts
		$V_S = \pm15V$, $R_L = 2k\Omega$	±10	±12		±10	±12		Volts
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm15V$	±11	+15.1 −12		±11	+15.1 −12		Volts
CMRR	Common-Mode Rejection Ratio		85	100		85	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		dB

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE
AC CHARACTERISTICS ($T_A = +25°C$, $V_S = \pm15V$)

Parameters	Description	Test Conditions	LF155A/355A Min.	LF155A/355A Typ.	LF155A/355A Max.	LF156A/356A Min.	LF156A/356A Typ.	LF156A/356A Max.	Units
SR	Slew Rate	LF155A/6A: $A_V = 1$,	3.0	5.0		10	12		V/µs
GBW	Gain-Bandwidth Product			2.5		4.0	4.5		MHz
t_S	Settling Time to 0.01%	(Note 7)		4.0			1.5		µs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$, f = 100Hz		25			15		nV/√Hz
		f = 1000Hz		20			12		
i_n	Equivalent Input Noise Current	f = 100Hz		0.01			0.01		pA/√Hz
		f = 1000Hz		0.01			0.01		
C_{IN}	Input Capacitance			3.0			3.0		pF

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

DC CHARACTERISTICS (Note 3)

Parameters	Description	Test Conditions	LF155/6 Min.	LF155/6 Typ.	LF155/6 Max.	LF255/6 Min.	LF255/6 Typ.	LF255/6 Max.	LF355/6 Min.	LF355/6 Typ.	LF355/6 Max.	Units
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$		3.0	5.0		3.0	5.0		3.0	10	mV
		Over Temperature			7.0			6.5			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		5.0			5.0			5.0		$\mu V/°C$
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5			0.5		$\mu V/°C$ per mV
I_{OS}	Input Offset Current	$T_J = 25°C$, (Notes 3, 5)		3.0	20		3.0	20		3.0	50	pA
		$T_J \leq T_{HIGH}$			20			1.0			2.0	nA
I_B	Input Bias Current	$T_J = 25°C$, (Notes 3, 5)		30	100		30	100		30	200	pA
		$T_J \leq T_{HIGH}$			50			5.0			8.0	nA
R_{IN}	Input Resistance	$T_J = 25°C$		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm15V$, $T_A = 25°C$	50	200		50	200		25	200		V/mV
		$V_O = \pm10V$, $R_L = 2k\Omega$ Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	$V_S = \pm15V$, $R_L = 10k\Omega$	±12	±13		±12	±13		±12	±13		Volts
		$V_S = \pm15V$, $R_L = 2k\Omega$	±10	±12		±10	±12		±10	±12		Volts
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm15V$	±11	+15.1 −12		±11	+15.1 −12		±11	+15.1 −12		Volts
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		80	100		dB

DC CHARACTERISTICS ($T_A = 25°C$, $V_S = \pm15V$)

Parameters	LF155A/355A LF155/255 Typ.	LF155A/355A LF155/255 Max.	LF355 Typ.	LF355 Max.	LF156A LF156/256 Typ.	LF156A LF156/256 Max.	LF356A/356 Typ.	LF356A/356 Max.	Units
Supply Current	2.0	4.0	2.0	4.0	5.0	7.0	5.0	10	mA

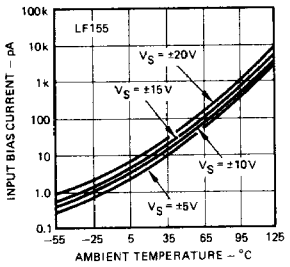
AC CHARACTERISTICS ($T_A = +25°C$, $V_S = \pm15V$)

Parameters	Description	Test Conditions	LF155/255/ LF355 Typ.	LF156/256 Min.	LF156/256/ LF356 Typ.	Units
SR	Slew Rate	LF155/6: $A_V = 1$, LF157: $A_V = 5$	5.0	7.5	12	V/μs
GBW	Gain-Bandwidth Product		2.5		5.0	MHz
t_s	Settling Time to 0.01%	(Note 7)	4.0		1.5	μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$, f = 100Hz	25		15	nV/√Hz
		f = 1000Hz	20		12	nV/√Hz
i_n	Equivalent Input Noise Current	f = 100Hz	0.01		0.01	pA/√Hz
		f = 1000Hz	0.01		0.01	pA/√Hz
C_{IN}	Input Capacitance		3.0		3.0	pF

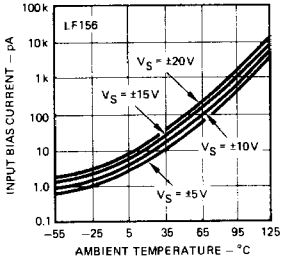
Notes:
1. The TO-99 package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case; for the DIP package, the device must be derated based on thermal resistance of 175°C/W junction to ambient.
2. Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
3. These specifications apply for $\pm15V \leq V_S \leq \pm20V$, $-55°C \leq T_A \leq +125°C$ and $T_{HIGH} = +125°C$ unless otherwise stated for the LF155A/6A and the LF155/6. For the LF255/6, these specifications apply for $\pm15V \leq V_S \leq \pm20V$, $-25°C \leq T_A \leq +85°C$ and $T_{HIGH} = 85°C$ unless otherwise stated. For the LF355A/6A, these specifications apply for $\pm15V \leq V_S \leq \pm20V$, $0°C \leq T_A \leq +70°C$ and $T_{HIGH} = +70°C$, and for the LF355/6 these specifications apply for $V_S = \pm15V$ and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.
4. The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5μV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.
5. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \theta_{jA}Pd$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
6. Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.
7. Settling time is defined here, for a unity gain inverter connection using 2kΩ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter.

TYPICAL DC PERFORMANCE CHARACTERISTICS

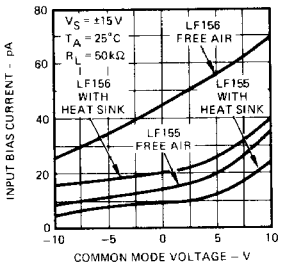
Input Bias Current



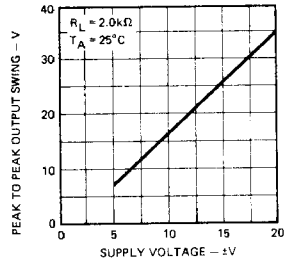
Input Bias Current



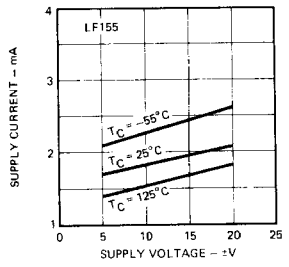
Input Bias Current



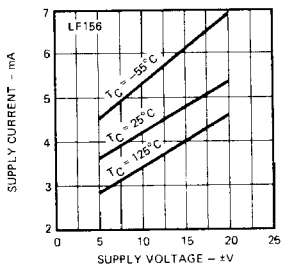
Voltage Swing



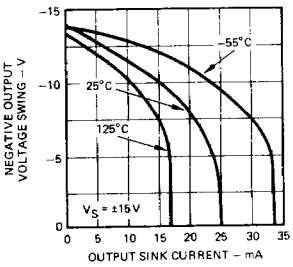
Supply Current



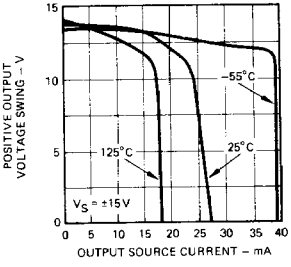
Supply Current



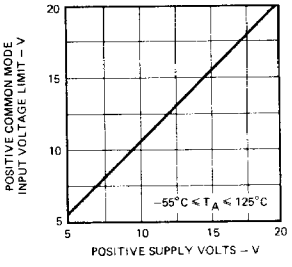
Negative Current Limit



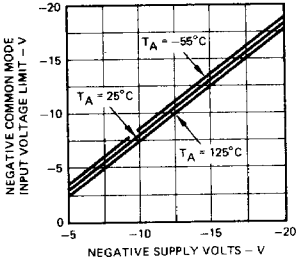
Positive Current Limit



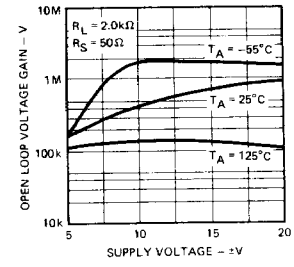
Positive Common-Mode Input Voltage Limit



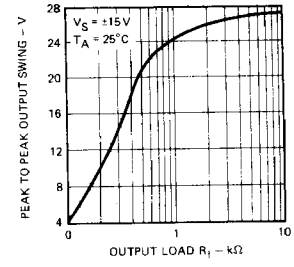
Negative Common-Mode Input Voltage Limit



Open Loop Voltage Gain



Output Voltage Swing



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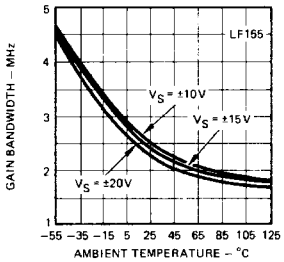
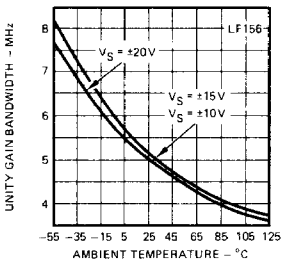
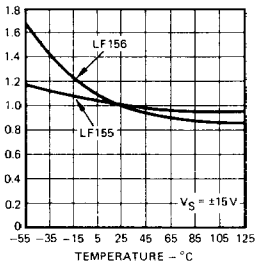
TYPICAL AC PERFORMANCE CHARACTERISTICS

Gain Bandwidth

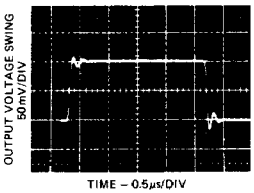




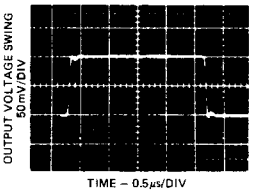
Normalized Slew Rate



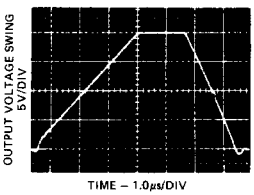
LF155 Small Signal Pulse Response, A_V = +1



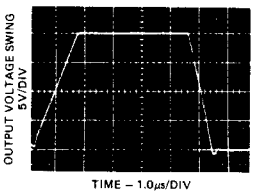
LF156 Small Signal Pulse Response, A_V = +1



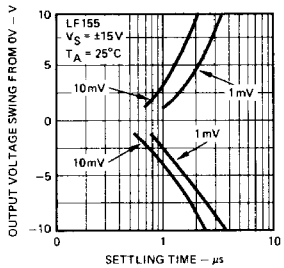
LF155 Large Signal Pulse Response, A_V = +1



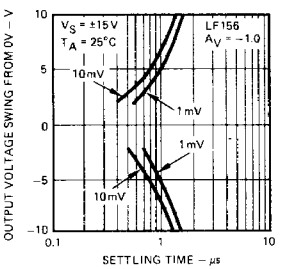
LF156 Large Signal Pulse Response, A_V = +1



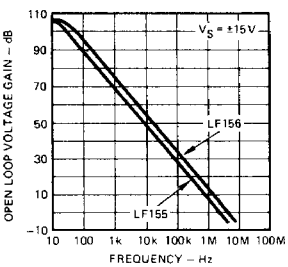
Inverter Settling Time



Inverter Settling Time



Open Loop Frequency Response



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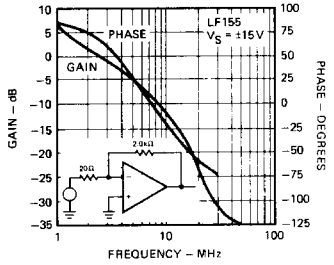
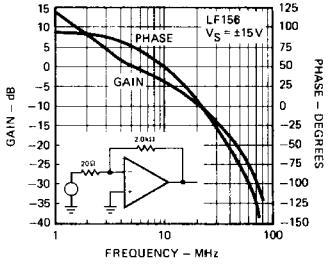
TYPICAL AC PERFORMANCE CHARACTERISTICS (Cont.)

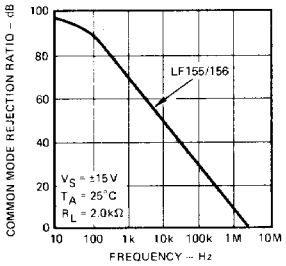
Bode Plot



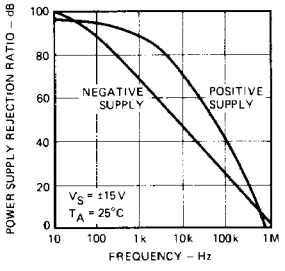
Bode Plot



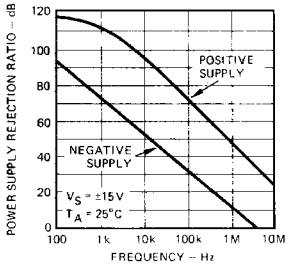
Common-Mode Rejection Ratio



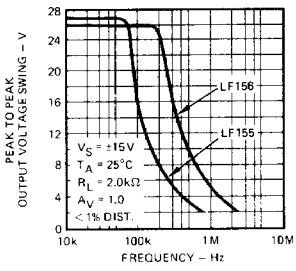
Power Supply Rejection Ratio (LF155)



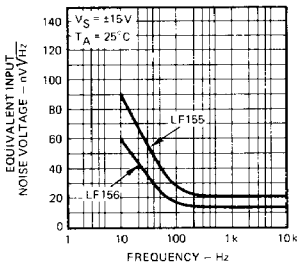
Power Supply Rejection Ratio (LF156)



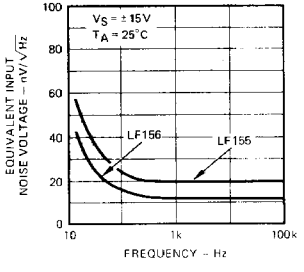
Undistorted Output Voltage Swing



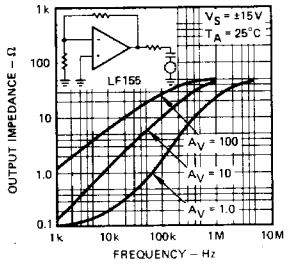
Equivalent Input Noise Voltage



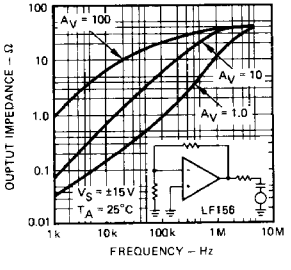
Equivalent Input Noise Voltage (Expanded Scale)



Output Impedance



Output Impedance



LIC-719

APPLICATION HINTS

The LF155/6 series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accomodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

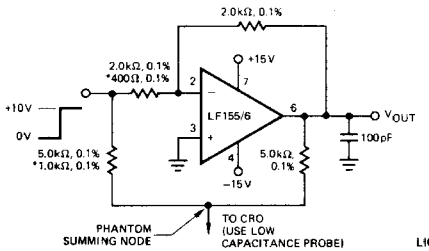
As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

5

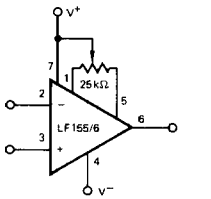
TYPICAL CIRCUIT CONNECTIONS AND PAD LAYOUT

Settling Time Test Circuit



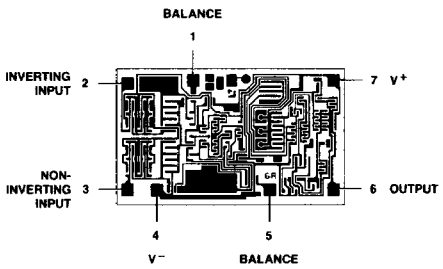
Settling time is tested with the LF155/156 connected as unity gain inverter Output = 10V step.

V_{OS} Adjustment



V_{OS} is adjusted with a 25 k potentiometer. The potentiometer wiper is connected to V^+.

Metallization and Pad Layout



75 x 45 Mils