HY638100 Series

128K x 8-bit CMOS FAST SRAM

PRELIMINARY

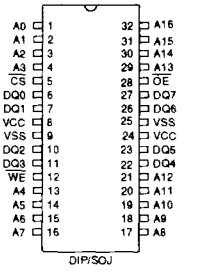
DESCRIPTION

The HY638100 is a high speed, low power and 131,072 x 8-bits CMOS static RAM fabricated using Hyundai's high performance twin tub CMOS process. This high reliability process coupled with innovative circuit design techniques, yields maximum access time of 15ns. The HY638100 has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0 volt. Using CMOS technology, supply voltages from 2.0 to 5.5 volt have little effect on supply current in data retention mode. Reducing the supply voltage to minimize current drain is unnecessary with the HY638100 series.

FEATURES

- **High speed - 15 / 17 / 20 / 25ns**
- **Low power consumption**
  - **Active 700mW (Typ.)**
  - **Stand-by 200μW (Typ.)**
- **Center Power/Ground Pin Connection**
- **Battery back up (L-part)**
  2.0V data retention
- **Fully static operation**
  No clock or refresh required
- **TTL compatible inputs and outputs**
- **Tri-state output**
- **High reliability 32 pin 400 mil PDIP/SOJ**

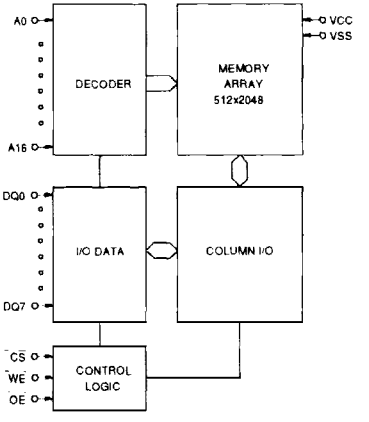
PIN CONNECTION



PIN DESCRIPTION

$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
A0-A16	Address Input
DQ0-DQ7	Data Input/Output
Vcc	Power(+ 5V)
Vss	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS NOTE 1

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}, V_{IN}, V_{OUT}	Power Supply, Input/Output Voltage	- 0.5 to 7.0	V
T_{BIAS}	Temperature under Bias	- 10 to 125	°C
T_{STG}	Storage Temperature	- 55 to 125	°C
P_D	Power Dissipation	1.0	W
I_{OUT}	Data Output Current	50	mA
T_{SOLDER}	Lead Soldering Temperature & Time	260•10	°C•sec

NOTE :

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating range of this specification is not implied. Exposure to absolute maximum ratings conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	-	0.8	V

NOTE :

1. V_{IL}= -3.0V for pulse width less than 20ns.

TRUTH TABLE

MODE	DQ OPERATION	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$
Standby	High-Z	H	X	X
Output Disabled	High-Z	L	H	H
Read	Data Out	L	H	L
Write	Data In	L	L	X

NOTE : H= V_{IH}, L= V_{IL}, X= Don't Care.

DC CHARACTERISTICS

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	POWER/ SPEED	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{CC}$		-2	-	2	μA
I_{LO}	Output Leakage Current	$V_{SS} \leq V_{OUT} \leq V_{CC}$ Output Disabled		-2	-	2	μA
I_{CC}	Static Operating Current	V_{CC}= MAX., $I_{I/O}$= 0mA f= 0, $\overline{CS}$= V_{IL}		-	-	100	mA
I_{CC1}	Dynamic Operating Current	$\overline{CS}$= V_{IL}, Min Duty Cycle= 100% $I_{I/O}$= 0mA	15	-	-	200	mA
			17	-	-	200	
			20	-	-	180	
			25	-	-	160	
I_{SB}	TTL Standby Current (TTL Inputs)	V_{CC}= MAX., V_{IN}= V_{IH} or V_{IL}, $\overline{CS} \geq V_{IH}$, f= 0		-	-	30	mA
I_{SB1}	CMOS Standby Current (CMOS Inputs)	V_{CC}= MAX., f= O $\overline{CS} \geq V_{CC}$– 0.2V,	-	-	-	2	mA
		$V_{IN} \geq V_{CC}$– 0.2V or $V_{IN} \leq$ 0.2V	L-part	-	40	200	μA
V_{OL}	Output Low Voltage	V_{CC}= MIN., I_{OL}= 8.0mA		-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC}= MIN., I_{OH}= -4.0mA		2.4	-	-	V

NOTE :
1. Typical values are at V_{CC}= 5.0V, T_A= 25°C and specified loading.

AC CHARACTERISTICS

(TA= 0°C to 70°C)

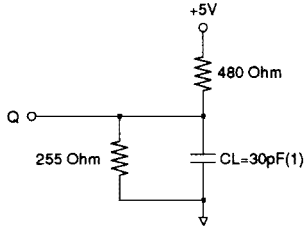
#	SYMBOL	PARAMETER	HY638100								UNIT
			-15		-17		-20		-25		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
	READ CYCLE										
1	tRC	Read Cycle Time	15	-	17	-	20	-	25	-	ns
2	tAA	Address Access Time	-	15	-	17	-	20	-	25	ns
3	tACS	Chip Select Access Time	-	15	-	17	-	20	-	25	ns
4	tOE	Output Enable to Output Valid	-	8	-	8	-	9	-	10	ns
5	tCLZ	Chip Select to Low-Z Output	3	-	3	-	3	-	3	-	ns
6	tOLZ	Output Enable to Low-Z Output	3	-	3	-	3	-	3	-	ns
7	tCHZ	Chip Disable to High-Z Output	-	8	-	8	-	9	-	10	ns
8	tOHZ	Output Disable to High-Z Output	-	8	-	8	-	9	-	10	ns
9	tOH	Output Hold from Address Change	3	-	3	-	3	-	3	-	ns
	WRITE CYCLE										
10	tWC	Write Cycle Time	15	-	17	-	20	-	25	-	ns
11	tCW	Chip Select to Write End	12	-	13	-	15	-	17	-	ns
12	tAW	Address Valid to Write End	12	-	13	-	15	-	17	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width	12	-	13	-	15	-	17	-	ns
15	tWR	Write Recovery Time	2	-	2	-	2	-	2	-	ns
16	tWHZ	Write to High-Z Output	-	8	-	8	-	9	-	10	ns
17	tDW	Data to Write Time Overlap	8	-	10	-	12	-	14	-	ns
18	tDH	Data Hold from Write End	0	-	0	-	0	-	0	-	ns
19	tOW	Output Active from Write End	3	-	3	-	3	-	3	-	ns

AC TEST CONDITIONS

(T_A= 0°C to 70°C)

Parameter	Value
Input Pulse Level	0V to 3.0V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Level	1.5V

AC TEST LOADS



NOTE :
1. Including jig and scope Capacitance.

CAPACITANCE

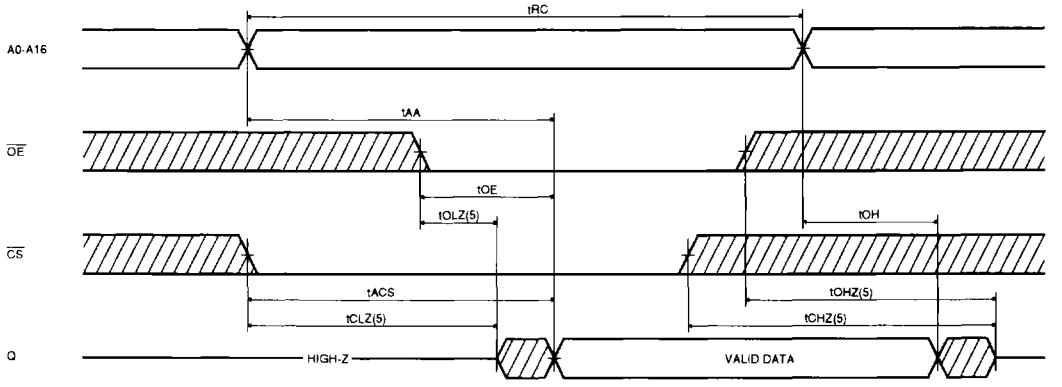
(T_A= 25°C, f= 1MHz)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}= 0V	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$= 0V	10	pF

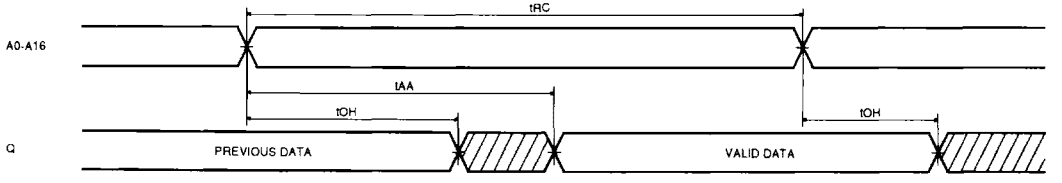
NOTE : This parameter is determined by device characterization but is not production tested.

TIMING DIAGRAM

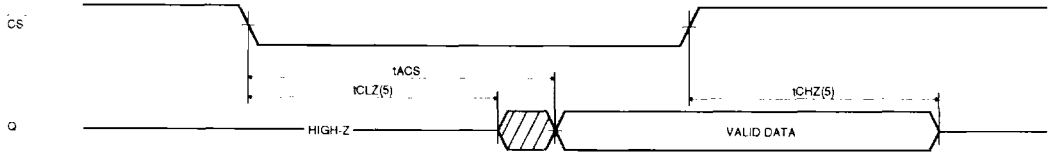
READ CYCLE 1 NOTE 1



READ CYCLE 2 NOTE 1, 2, 4

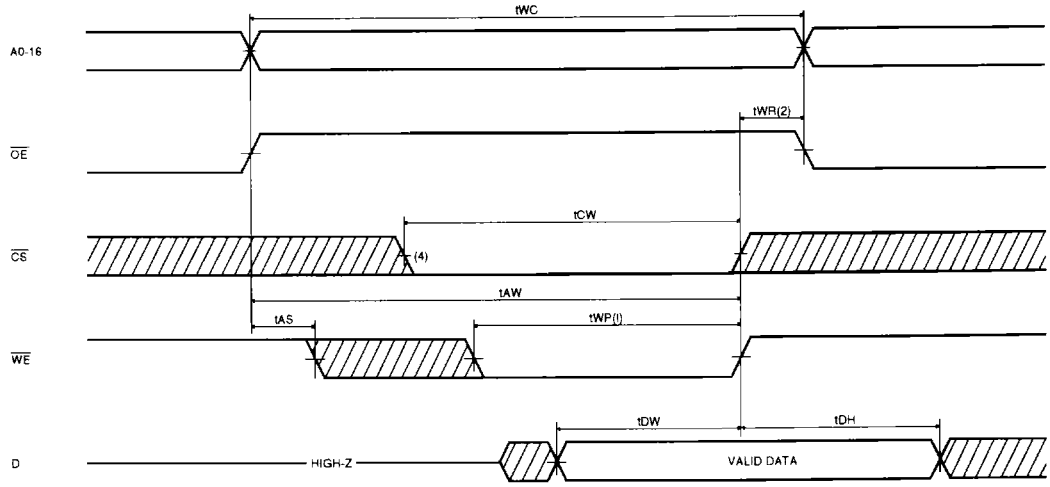


READ CYCLE 3 NOTE 1, 3, 4

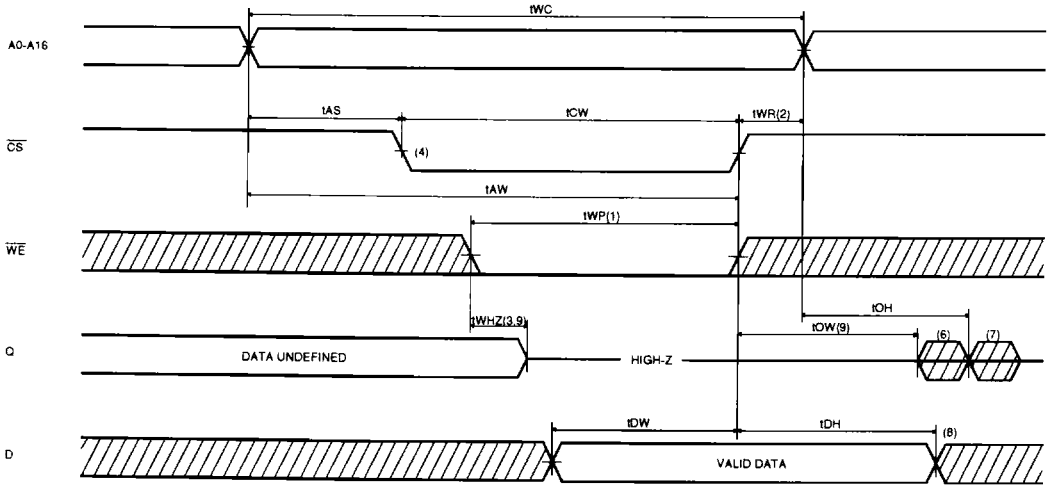


NOTES :
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected $\overline{CS}$= VIL.
3. Addresses are valid prior to coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$= VIL.
5. Transition is measured ± 500mV from steady state.
   This parameter is sampled and not 100% tested.

WRITE CYCLE 1



WRITE CYCLE 2



NOTES :

1. A write occurs during the overlap (tWP) of low $\overline{CS}$ and low $\overline{WE}$.
2. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high at the end of write cycle.
3. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low Transitions or after $\overline{WE}$ transition, outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low ($\overline{OE}$= VIL).
6. Q is the same phase of write data of this write cycle.
7. Q is the read data of next address.
8. If $\overline{CS}$ is low during this period, DQ pins are in the output state.
   Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ± 500mV from steady state.
   This parameter is sampled and not 100% tested.

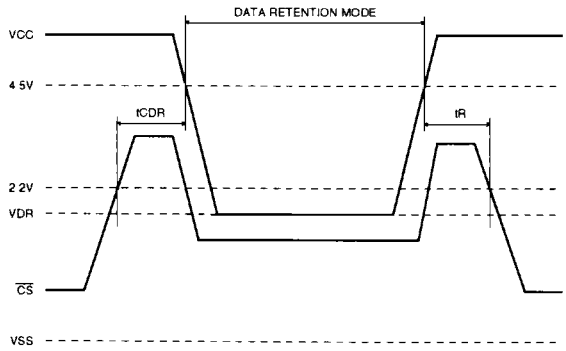
DATA RETENTIOSN CHARACTERISTICS NOTE 1

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITION	POWER	MIN.	TYP.[2]	MAX.	UNIT
V_{DR}	V_{CC} for retention of data	$\overline{CS} \geq V_{CC}$-0.2V, $V_{SS} \leq V_{IN} \leq V_{CC}$		2.0	-	-	V
I_{CCDR}	Data Retention Current	V_{CC}= 3.0V, $\overline{CS} \geq V_{CC}$-0.2V, $V_{SS} \leq V_{IN} \leq V_{CC}$	L	-	5	100	µA
t_{CDR}	Chip Disable to Data Retention Time	See Data Retention Timing Diagram		0	-	-	ns
t_R	Operating Recovery Time			t_{RC}[3]	-	-	ns

NOTES :
1. These characteristics are only applied to L-part.
2. Typical values are at the condition of T_A= 25°C.
3. t_{RC} is Read Cycle Time.

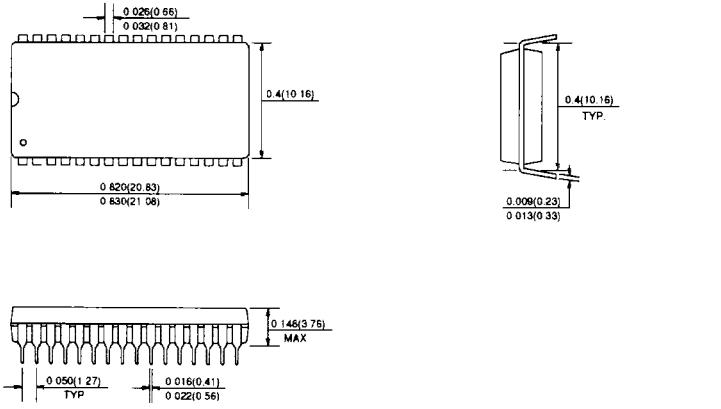
DATA RETENTION TIMING DIAGRAM



PACKAGE INFORMATION

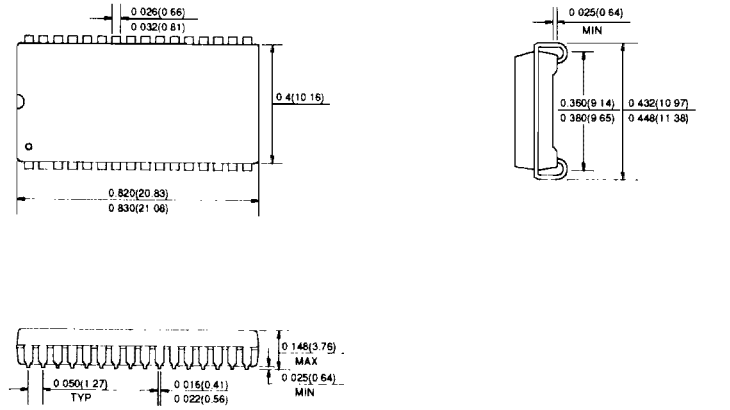
400 mil 32 pin Dual In Line Package (P)

UNIT INCH(mm)



400 mil 32 pin Small Outline Package (J)

UNIT INCH(mm)



ORDERING INFORMATION

PART NO	SPEED	POWER	PACKAGE
HY638100PC	15/17/20/25		PDIP
HY628100LPC	15/17/20/25	L-part	PDIP
HY638100JC	15/17/20/25		SOJ
HY638100LJC	15/17/20/25	L-part	SOJ