

# Complementary Plastic Power Transistors

## NPN/PNP Silicon DPAK For Surface Mount Applications



ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)

### MJD200 (NPN), MJD210 (PNP)

Designed for low voltage, low-power, high-gain audio amplifier applications.

#### Features

- High DC Current Gain
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Low Collector–Emitter Saturation Voltage
- High Current–Gain – Bandwidth Product
- Annular Construction for Low Leakage
- Epoxy Meets UL 94 V–0 @ 0.125 in
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q101 Qualified and PPAP Capable
- These Devices are Pb–Free and are RoHS Compliant

#### MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector–Base Voltage	$V_{CB}$	40	Vdc
Collector–Emitter Voltage	$V_{CEO}$	25	Vdc
Emitter–Base Voltage	$V_{EB}$	8.0	Vdc
Collector Current – Continuous	$I_C$	5.0	Adc
Collector Current – Peak	$I_{CM}$	10	Adc
Base Current	$I_B$	1.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	12.5 0.1	W W/ $^\circ\text{C}$
Total Power Dissipation (Note 1) @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.4 0.011	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150	$^\circ\text{C}$
ESD – Human Body Model	HBM	3B	V
ESD – Machine Model	MM	C	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

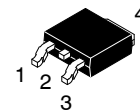
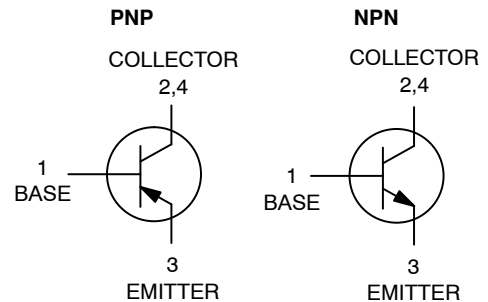
1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	10	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction–to–Ambient (Note 2)	$R_{\theta JA}$	89.3	$^\circ\text{C}/\text{W}$

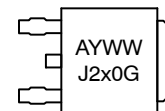
2. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

### SILICON POWER TRANSISTORS 5 AMPERES 25 VOLTS, 12.5 WATTS



**DPAK  
CASE 369C  
STYLE 1**

#### MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- WW = Work Week  
x = 1 or 0
- G = Pb–Free Package

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

# MJD200 (NPN), MJD210 (PNP)

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector-Emitter Sustaining Voltage (Note 3) ( $I_C = 10\text{ mAdc}$ , $I_B = 0$ )	$V_{CE(sus)}$	25	-	Vdc
Collector Cutoff Current ( $V_{CB} = 40\text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 40\text{ Vdc}$ , $I_E = 0$ , $T_J = 125^\circ\text{C}$ )	$I_{CBO}$	-	100	nAdc $\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 8\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	-	100	nAdc
<b>ON CHARACTERISTICS</b>				
C Current Gain (Note 3), ( $I_C = 500\text{ mAdc}$ , $V_{CE} = 1\text{ Vdc}$ ) ( $I_C = 2\text{ Adc}$ , $V_{CE} = 1\text{ Vdc}$ ) ( $I_C = 5\text{ Adc}$ , $V_{CE} = 2\text{ Vdc}$ )	$h_{FE}$	70 45 10	- 180 -	-
Collector-Emitter Saturation Voltage (Note 3) ( $I_C = 500\text{ mAdc}$ , $I_B = 50\text{ mAdc}$ ) ( $I_C = 2\text{ Adc}$ , $I_B = 200\text{ mAdc}$ ) ( $I_C = 5\text{ Adc}$ , $I_B = 1\text{ Adc}$ )	$V_{CE(sat)}$	- - -	0.3 0.75 1.8	Vdc
Base-Emitter Saturation Voltage (Note 3) ( $I_C = 5\text{ Adc}$ , $I_B = 1\text{ Adc}$ )	$V_{BE(sat)}$	-	2.5	Vdc
Base-Emitter On Voltage (Note 3) ( $I_C = 2\text{ Adc}$ , $V_{CE} = 1\text{ Vdc}$ )	$V_{BE(on)}$	-	1.6	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Current-Gain - Bandwidth Product (Note 4) ( $I_C = 100\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 10\text{ MHz}$ )	$f_T$	65	-	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$ ) MJD200 MJD210, NJVMJD210T4G	$C_{ob}$	- -	80 120	pF

3. Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle  $\approx 2\%$ .

4.  $f_T = |h_{fe}| \cdot f_{test}$ .

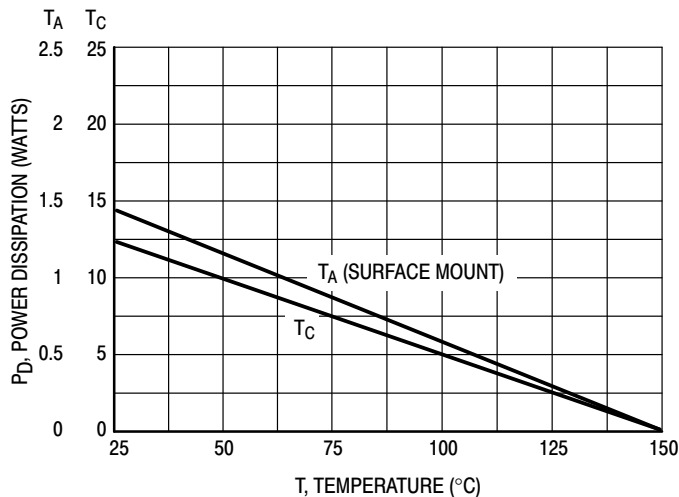


Figure 1. Power Derating

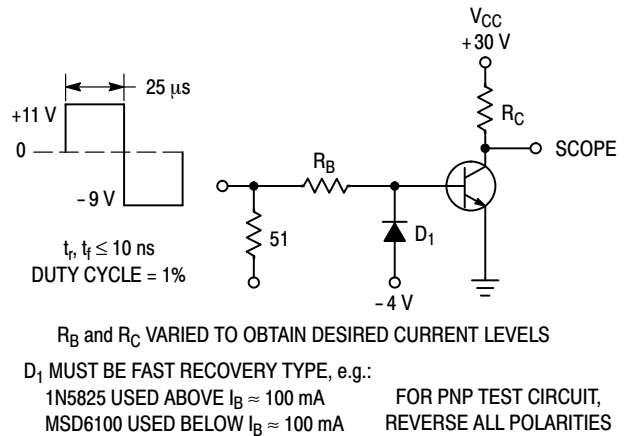


Figure 2. Switching Time Test Circuit

# MJD200 (NPN), MJD210 (PNP)

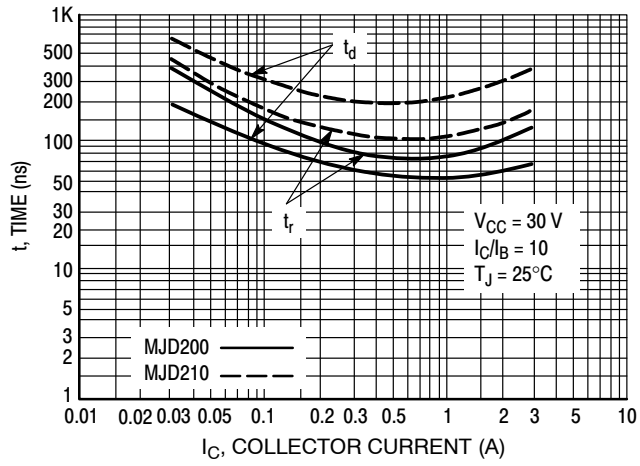


Figure 3. Turn-On Time

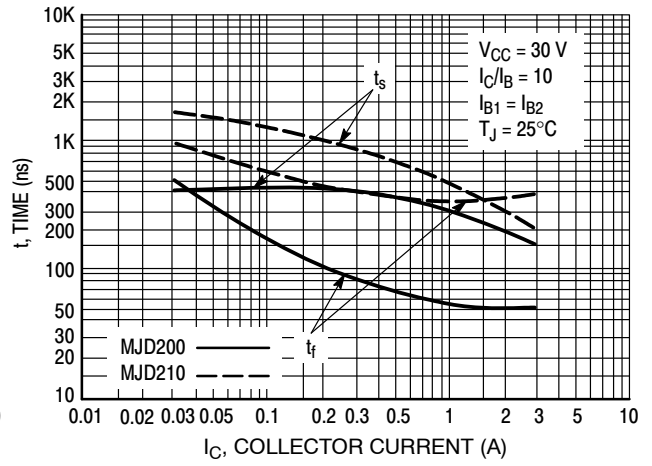


Figure 4. Turn-Off Time

# MJD200 (NPN), MJD210 (PNP)

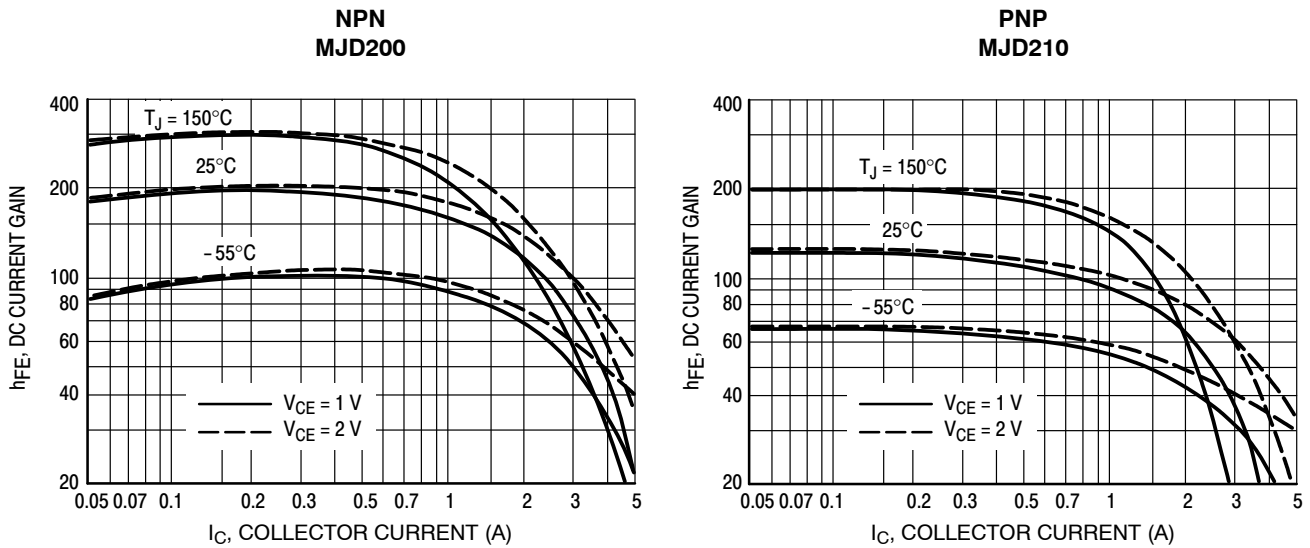


Figure 5. DC Current Gain

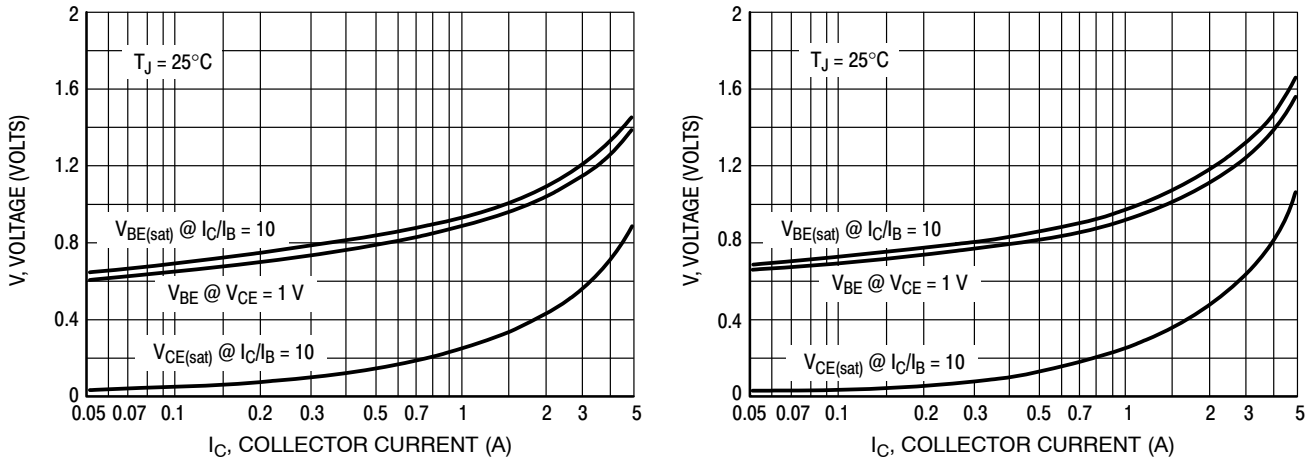


Figure 6. "On" Voltage

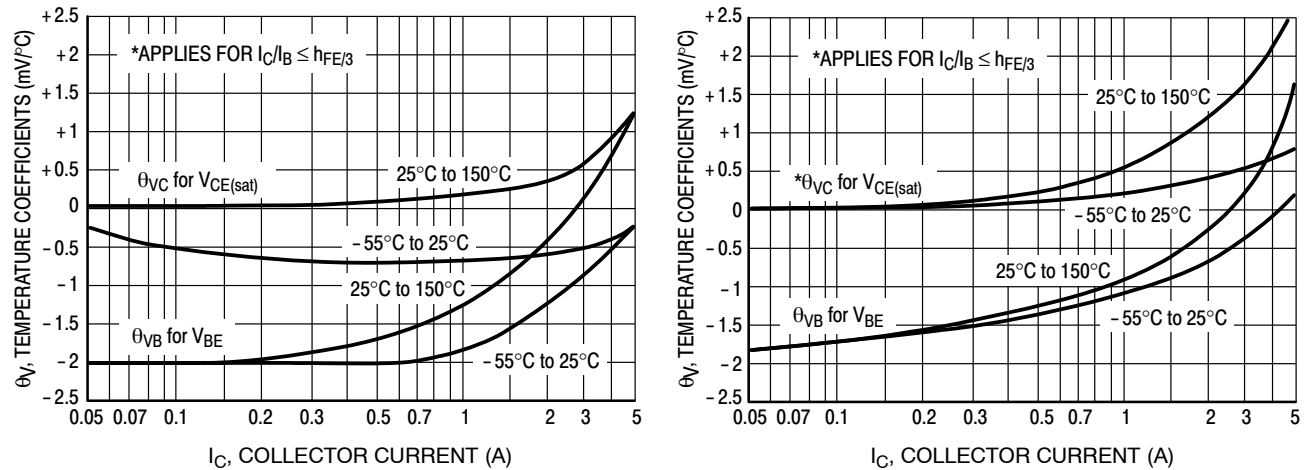


Figure 7. Temperature Coefficients

# MJD200 (NPN), MJD210 (PNP)

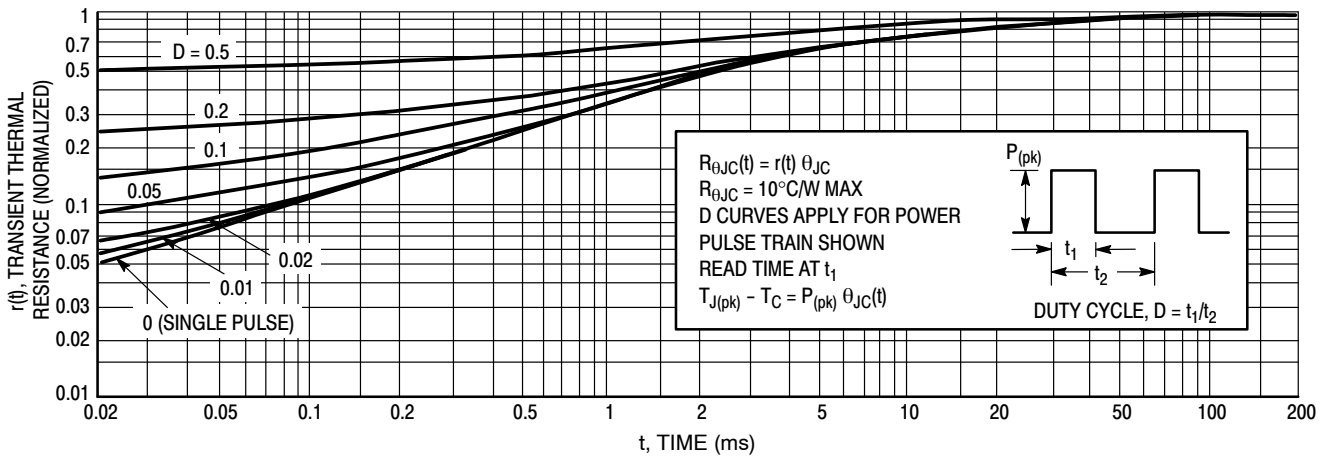


Figure 8. Thermal Response

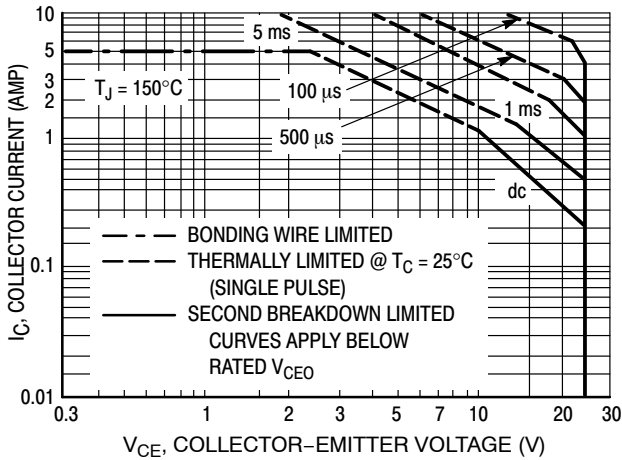


Figure 9. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 9 is based on  $T_{J(pk)} = 150^{\circ}\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^{\circ}\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 8. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

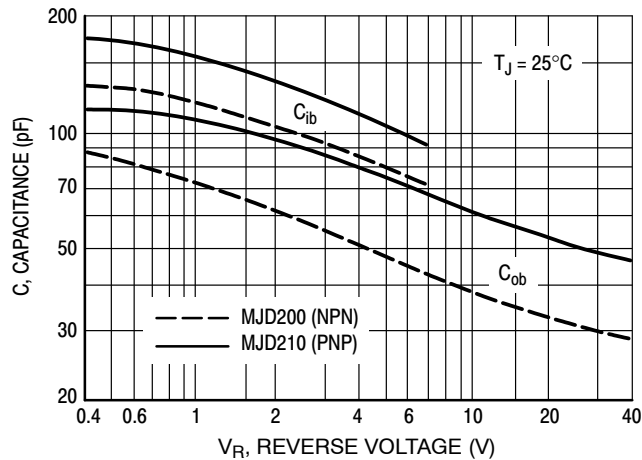


Figure 10. Capacitance

## MJD200 (NPN), MJD210 (PNP)

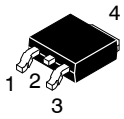
### ORDERING INFORMATION

Device	Package Type	Shipping†
MJD200G	DPAK (Pb-Free)	75 Units / Rail
MJD200RLG	DPAK (Pb-Free)	1,800 / Tape & Reel
MJD200T4G	DPAK (Pb-Free)	2,500 / Tape & Reel
MJD210G	DPAK (Pb-Free)	75 Units / Rail
MJD210RLG	DPAK (Pb-Free)	1,800 / Tape & Reel
MJD210T4G	DPAK (Pb-Free)	2,500 / Tape & Reel
NJVMJD210T4G*	DPAK (Pb-Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable

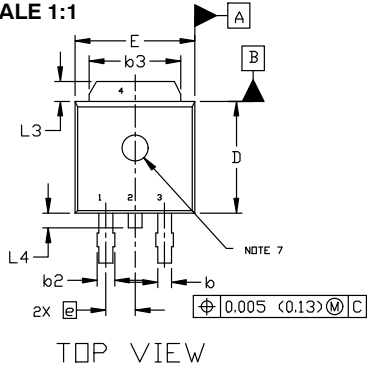
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



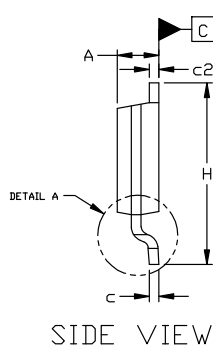
## DPAK (SINGLE GAUGE) CASE 369C ISSUE G

DATE 31 MAY 2023

SCALE 1:1



TOP VIEW

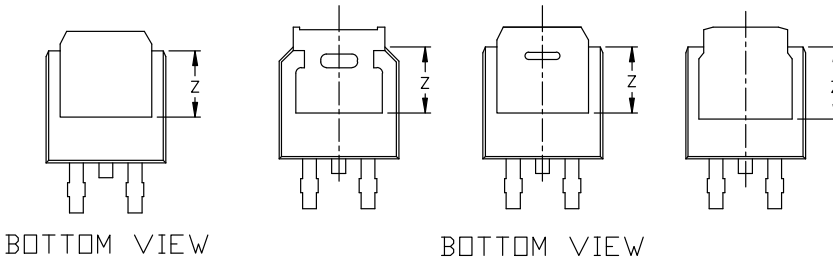


SIDE VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

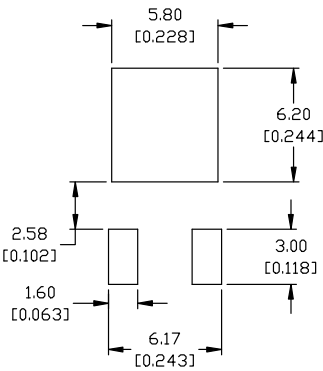
DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114	REF	2.90	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	----	0.040	---	1.01
Z	0.155	----	3.93	---



BOTTOM VIEW

BOTTOM VIEW

ALTERNATE CONSTRUCTIONS

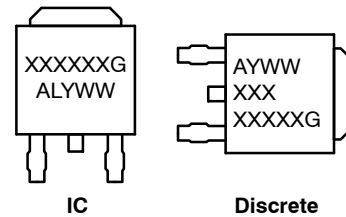


### RECOMMENDED MOUNTING FOOTPRINT\*

\*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

- |  |  |   |   |  |
|--|--|---|---|--|
| <b>STYLE 1:</b><br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 2:</b><br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN          | <b>STYLE 3:</b><br>PIN 1. ANODE<br>2. CATHODE<br>3. ANODE<br>4. CATHODE | <b>STYLE 4:</b><br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE<br>4. ANODE              | <b>STYLE 5:</b><br>PIN 1. GATE<br>2. ANODE<br>3. CATHODE<br>4. ANODE     |
| <b>STYLE 6:</b><br>PIN 1. MT1<br>2. MT2<br>3. GATE<br>4. MT2                 | <b>STYLE 7:</b><br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 8:</b><br>PIN 1. N/C<br>2. CATHODE<br>3. ANODE<br>4. CATHODE   | <b>STYLE 9:</b><br>PIN 1. ANODE<br>2. CATHODE<br>3. RESISTOR ADJUST<br>4. CATHODE | <b>STYLE 10:</b><br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE<br>4. ANODE |

### GENERIC MARKING DIAGRAM\*



- XXXXXX = Device Code  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 WW = Work Week  
 G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	DPAK (SINGLE GAUGE)	PAGE 1 OF 1

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