DENSE-PAC
MICROSYSTEMS

4 Megabit High Speed CMOS SRAM

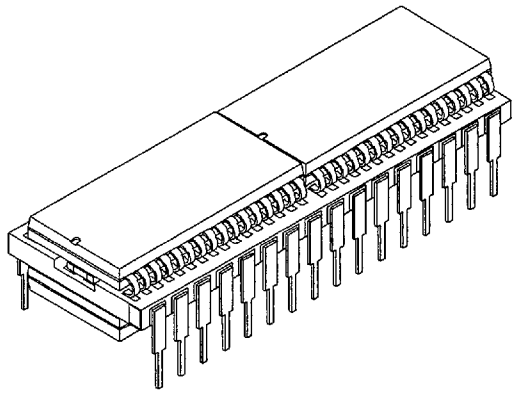
DPS512S8AP

DESCRIPTION:

The DPS512S8AP is a high speed 512K x 8 high-density, low-power static RAM module comprised of four high speed ceramic 128K x 8 monolithic SRAM's, an advanced high-speed CMOS decoder and decoupling capacitors surface mounted on a co-fired ceramic substrate having side-brazed leads.

The DPS512S8AP is available in a 600-mil-wide, 32-pin dual-in-line package that conforms to the same JEDEC standard pin configuration as the future four megabit monolithics.

The DPS512S8AP operates from a single +5V supply and all input and output pins are completely TTL-compatible. The low power of the DPS512S8AP make it ideal for battery-backed applications.



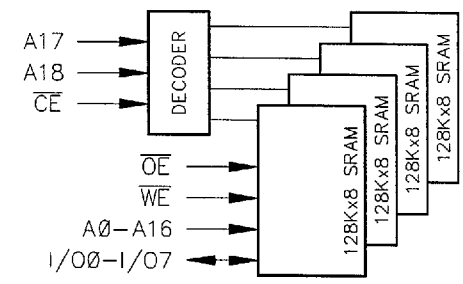
FEATURES:

- Organized Available: 524, 288 by 8 bit configuration
- Access Times: 25*, 35, 45, 55, 70ns
- Low Power Dissipation:
  - 2.0 mW (typ.) Standby
  - 450 mW (typ.) Operating
- 2 - Volt Data Retention
- Fully Static Operation - No clock or refresh required
- All inputs and outputs are TTL-Compatible
- 600 mil, 32 - Pin JEDEC standard DIP pinout

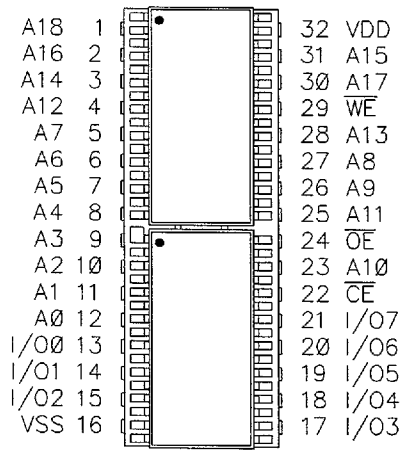
* Available in Commercial only.

PIN NAMES	
A0 - A18	Address Inputs
I/O0 - I/O7	Data In/Out
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground

FUNCTIONAL BLOCK DIAGRAM



PIN-OUT DIAGRAM



RECOMMENDED OPERATING RANGE[1]						
Symbol	Characteristic		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage		2.2		$V_{DD}+0.3$	V
V_{IL}	Input LOW Voltage		-0.5[2]		0.8	V
T_A	Operating Temperature	C	0	+25	+70	°C
		I	-40	+25	+85	

TRUTH TABLE					
Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current
Not Selected	H	X	X	HIGH-Z	Standby
D_{OUT} Disable	L	H	H	HIGH-Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

H = HIGH L = LOW X = Don't Care

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	HIGH Voltage	I_{OH} = -4.0mA	2.4	-	V
V_{OL}	LOW Voltage	I_{OL} = 8.0mA		0.4	V

ABSOLUTE MAXIMUM RATINGS[3]			
Symbol	Parameter	Max.	Unit
T_{STC}	Storage Temperature	-40 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
V_{DD}	Supply Voltage [1]	-0.5 to + 7.0	V
$V_{I/O}$	Input/Output Voltage [1]	-0.5 to V_{DD} +0.5	V

CAPACITANCE[4]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	50	pF	V_{IN} = 0V
C_{CE}	Chip Enable	20		
C_{WE}	Write Enable	45		
C_{OE}	Output Enable	45		
$C_{I/O}$	Data Input/Output	50		

DC OPERATING CHARACTERISTICS: Over operating ranges							
Symbol	Characteristics	Test Conditions	COMMERCIAL		INDUSTRIAL		Unit
			Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-20	+20	-20	+20	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}	-40	+40	-40	+40	µA
I_{CC2}	Operating Supply Current	Cycle = min., Duty = 100%, I_{OUT} = 0mA		230		245	mA
I_{SB1}	Full Standby Supply Current (CMOS)	$V_{IN} \geq V_{DD}$ -0.2V or $V_{IN} \leq V_{SS}$ +0.2V		20		20	mA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}		80		100	mA
V_{OL}	Output Low Voltage	I_{OUT} = 8.0mA		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -4.0mA	2.4		2.4		V

DATA RETENTION CHARACTERISTICS								
Symbol	Parameter	Test Conditions	TYP.	COMMERCIAL		INDUSTRIAL		Unit
				Min.	Max.	Min.	Max.	
V_{DR}	Data Retention Voltage	$\overline{CE} \geq V_{DR}$ -0.2V		2.0	5.5	2.0	5.5	V
I_{CCDR2}	Data Retention Supply Current	V_{DR} = 2.0V	0.14		1.00		1.60	mA
I_{CCDR3}	Data Retention Supply Current	V_{DR} = 3.0V	0.28		1.60		2.40	mA
t_{CDR}	Chip Disable to Data Retention Time			0		0		ns
t_R	Recovery Time	t_{RC} = Read Cycle Timing		5		5		ms

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns *
Input and Output Timing Reference Levels	1.5V

* Transition measured between 0.8V and 2.2V.

Output Load		
Load	C_L	Parameters Measured
1	30pF	except t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{WLZ}
2	5pF	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{WLZ}

DATA RETENTION WAVEFORM

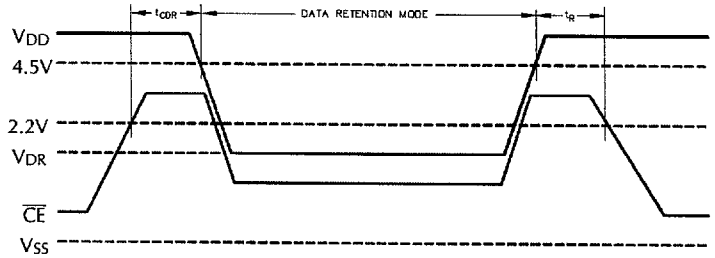
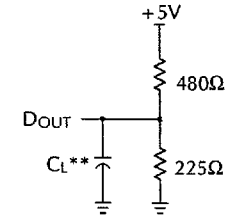


Figure 1. Output Load

** Including Probe and Jig Capacitance.

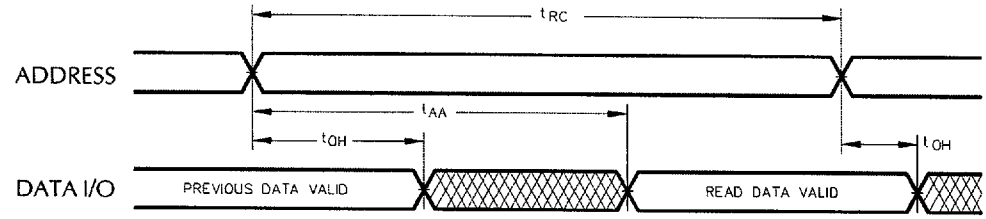


AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges													
No.	Symbol	Parameter	25ns †		35ns		45ns		55ns		70ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	25		35		45		55		70		ns
2	t_{AA}	Address Access Time		25		35		45		55		70	ns
3	t_{CO}	Chip Enable to Output Valid		25		35		45		55		70	ns
4	t_{OV}	Output Enable to Output Valid		10		25		35		40		45	ns
5	t_{CLZ}	Chip Enable to Output in LOW-Z [4, 6]	5		5		5		5		5		ns
6	t_{OLZ}	Output Enable to Output in LOW-Z [4, 6]	0		0		0		0		0		ns
7	t_{CHZ}	Chip Enable to Output in HIGH-Z [4, 6]		12		25		25		30		35	ns
8	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 6]		10		15		20		25		30	ns
9	t_{OH}	Output Hold from Address Change	3		3		5		5		10		ns

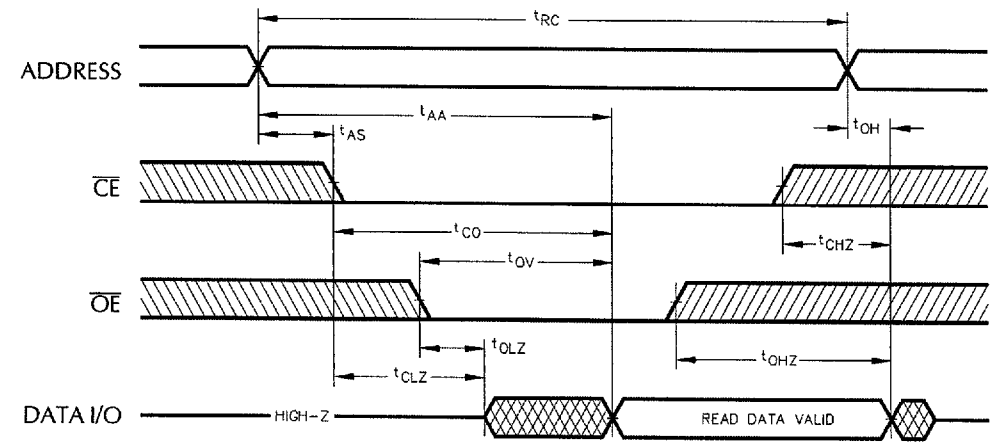
AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges [6, 7]													
No.	Symbol	Parameter	25ns †		35ns		45ns		55ns		70ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t_{WC}	Write Cycle Time	25		35		45		55		70		ns
11	t_{AW}	Address Valid to End of Write	20		30		40		50		65		ns
12	t_{CW}	Chip Enable to End of Write	20		30		40		50		65		ns
13	t_{AS}	Address Set-up Time ***	0		0		0		0		0		ns
14	t_{WP}	Write Pulse Width	20		25		35		40		55		ns
15	t_{AH}	Address Hold Time	5		5		5		5		5		ns
16	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 6]		10		15		20		25		30	ns
17	t_{DW}	Data to Write Time Overlap	15		15		20		25		35		ns
18	t_{DH}	Data Hold Time from Write Time	0		0		0		0		0		ns
19	t_{OW}	Output Active from End of Write	0		3		5		5		5		ns

*** Valid for both Read and Write Cycles.
† Available in commercial only.

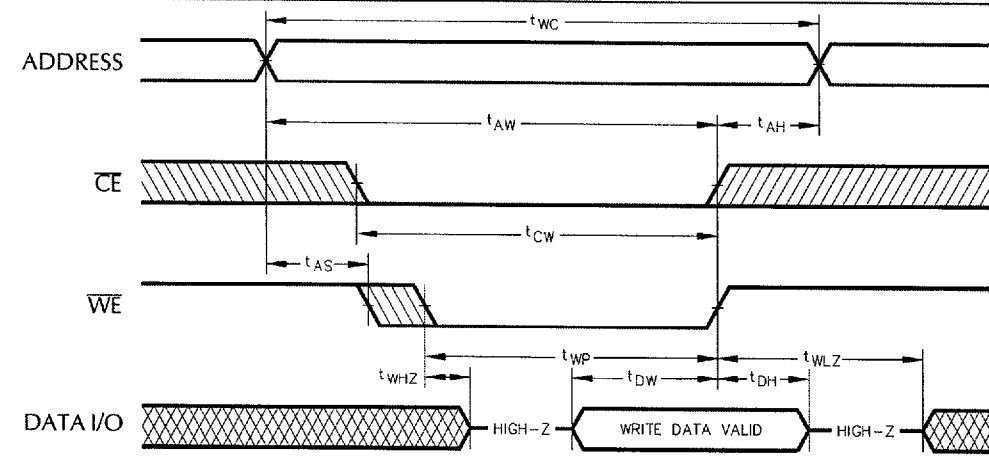
READ CYCLE 1: Address Controlled. $\overline{WE}$ is HIGH. $\overline{CE}$ and $\overline{OE}$ are LOW.



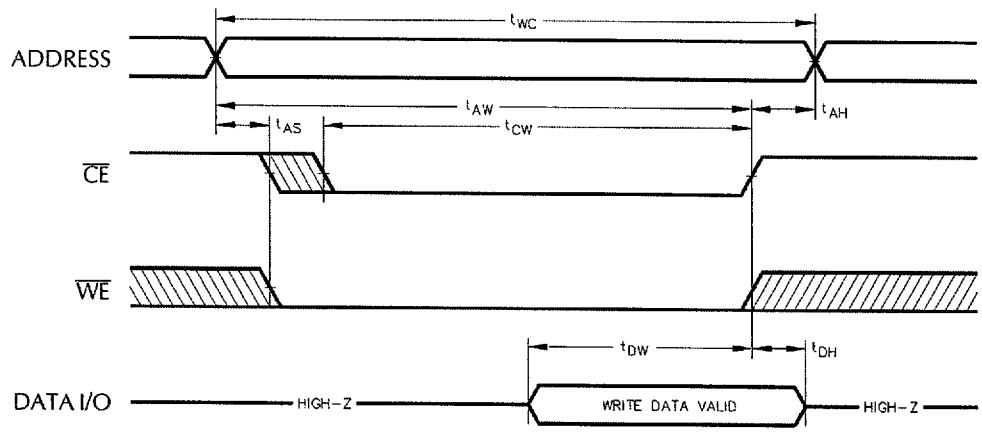
READ CYCLE 2: $\overline{CE}$ Controlled. $\overline{WE}$ is HIGH.



WRITE CYCLE 1: $\overline{WE}$ Controlled. $\overline{OE}$ is LOW.



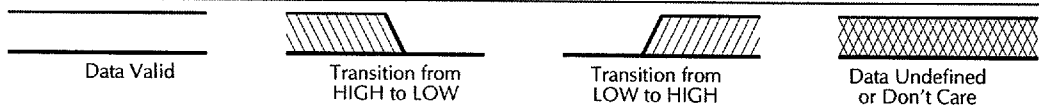
WRITE CYCLE 2: $\overline{CE}$ Controlled. $\overline{OE}$ is HIGH.



NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state, and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.

WAVEFORM KEY



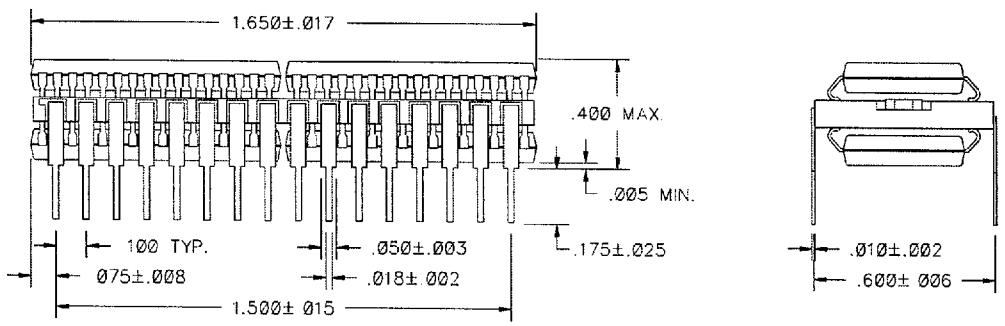
ORDERING INFORMATION

DP S 512 S 8 A P – XX X

PREFIX		
TYPE		
MEMORY DEPTH		
DESIG.		
MEMORY WIDTH		
DESIG.		
PACKAGE		
SPEED		
GRADE		

- GRADE: I INDUSTRIAL –40°C to +85°C; C COMMERCIAL 0°C to +70°C
- SPEED: 25 25ns (COMMERCIAL ONLY); 35 35ns; 45 45ns; 55 55ns; 70 70ns
- PACKAGE: P 32-PIN CERDIP WITH PLASTIC DEVICES
- DESIG.: A HIGH SPEED
- MEMORY WIDTH: 8
- DESIG.: S MEMORY MODULE WITH SUPPORT LOGIC
- MEMORY DEPTH: 512
- TYPE: S CMOS SRAM
- PREFIX: DP

MECHANICAL DRAWING



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