

# 54F/74F845

## 8-Bit Transparent Latch

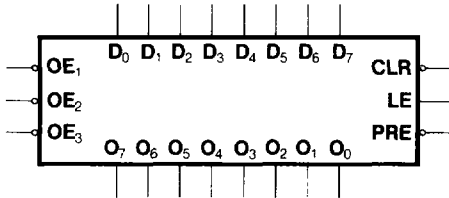
### Description

The 'F845 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data buses or buses carrying parity.

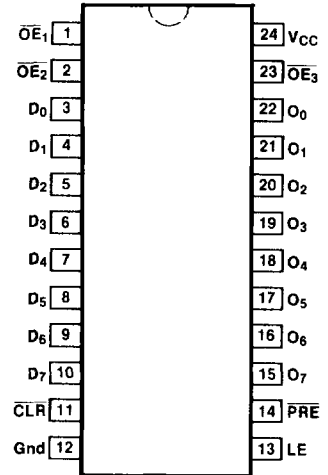
The 'F845 is functionally compatible with AMD's AM29845.

**Ordering Code:** See Section 5

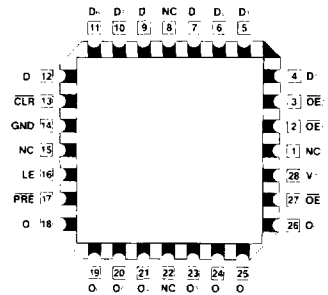
### Logic Symbol



### Connection Diagrams



**Pin Assignment for DIP and SOIC**



**Pin Assignment for LCC and PCC**

**Input Loading/Fan-Out:** See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D <sub>0</sub> -D <sub>7</sub>	Data Inputs	0.5/0.375
O <sub>0</sub> -O <sub>7</sub>	Data Outputs	75/15 (12.5)
OE <sub>1</sub> -OE <sub>3</sub>	Output Enables	0.5/0.375
LE	Latch Enable	0.5/0.375
CLR	Clear	0.5/0.375
PRE	Preset	0.5/0.375

### Functional Description

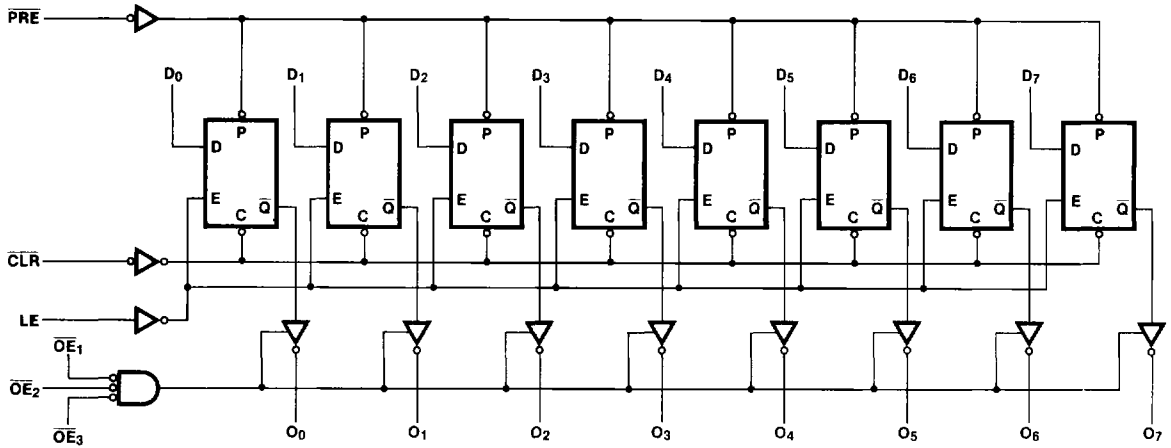
The 'F845 consists of eight D-type latches with 3-state outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation as the output transition follows the data in transition. On the LE HIGH-to-LOW transition the data that meets the setup times is latched. Data appears on the bus when the Output Enable ( $\overline{OE}$ ) is LOW. When  $\overline{OE}$  is HIGH, the bus output is in the high impedance state.

### Function Table

Inputs					Internal	Output	Function
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D	Q	O	
H	H	H	X	X	X	Z	High Z
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched
H	L	H	L	X	H	Z	Latched

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 NC = No Change

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F74F			Units	Conditions
		Min	Typ	Max		
$I_{CC}$	Power Supply Current		50	75	mA	$V_{CC} = \text{Max}$

**AC Characteristics:** See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$	$T_A, V_{CC} =$ Mil $C_L = 50\text{ pF}$	$T_A, V_{CC} =$ Com $C_L = 50\text{ pF}$		
		Min Typ Max	Min Max	Min Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $D_n$ to $O_n$	8.0 6.0			ns	3-1 3-4
$t_{PLH}$ $t_{PHL}$	Propagation Delay LE to $O_n$	13.0 8.0			ns	3-1 3-7
$t_{PLH}$	Propagation Delay $\overline{\text{PRE}}$ to O	9.0			ns	3-1 3-7
$t_{PHL}$	Propagation Delay $\overline{\text{CLR}}$ to O	18.0			ns	3-1 3-9
$t_{PZH}$ $t_{PZL}$	Output Enable Time $\overline{\text{OE}}$ to $O_n$	11.0 8.0			ns	3-1 3-12
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\overline{\text{OE}}$ to $O_n$	7.0 5.0				

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**AC Operating Requirements:** See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$	$T_A, V_{CC} =$ Mil	$T_A, V_{CC} =$ Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, High or LOW $D_n$ to LE	3.0 3.0			ns	3-15
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $D_n$ to LE	3.0 3.0				
$t_w(H)$	LE Pulse Width, HIGH	4.0			ns	3-7
$t_w(L)$	$\overline{\text{PRE}}$ Pulse Width, LOW	5.0			ns	3-9
$t_w(L)$	$\overline{\text{CLR}}$ Pulse Width, LOW	6.0			ns	3-9
$t_{rec}$	$\overline{\text{PRE}}$ Recovery Time	12.0			ns	3-11
$t_{rec}$	$\overline{\text{CLR}}$ Recovery Time	12.0			ns	3-11