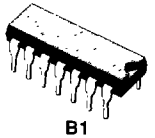
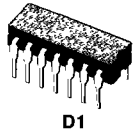
4-STAGE PRESETTABLE RIPPLE COUNTERS

- LOW POWER CONSUMPITION: TYPICALLY 80 mW
- ASYNCHRONOUS PRESETTABLE
- EASY MULTISTAGE CASCADING
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- HIGH COUNTING RATES: TYPICALLY 70 MHz
- ASYNCHRONOUS MASTER RESET
- CHOICE OF COUNTING MODES: BCD, BI-QUINARY, BINARY
- FULLY TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

T74LSXXX D1 T74LSXXX C1
T74LSXXX B1 T74LSXXX M1

DESCRIPTION

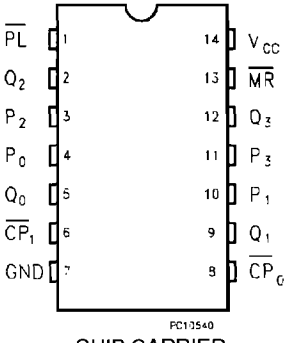
The T74LS196 decade counter is partioned into divide-by-two and divide-by five section which can be combined to count either in BCD (8, 4, 2, 1) sequence or in a bi-quinary mode producing a 50 % duty cycle output. The T74LS197 contains divide-by-two and divide-by-eight sections which can be combined to form a modulo-16 binary counter. Low Power Schottky technology is used to achive typical count rates of 70 MHz and power dissipation of only 80 mW. Both circuit types have Master Reset ($\overline{MR}$) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input ($\overline{PL}$) overrides clocked operations and asynchronously loads the data on the Parallel Data Inputs (P_n) into the flip-flops. This preset feature makes the circuits usable as programmable counters. The circuits can also be used as 4-bit latches, loading data from the Parallel Data inputs when $\overline{PL}$ is LOW and storing the data when $\overline{PL}$ is HIGH.

PIN NAMES

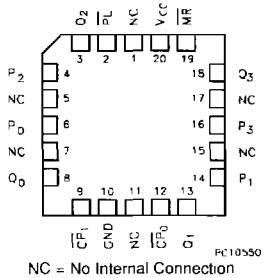
$\overline{CP_0}$	Clock (Active LOW Going Edge) Input to Divide-by-Two Section
$\overline{CP_1}$	Clock (Active LOW Going Edge) Input to Divide-by-Five Section (LS196)
$\overline{CP_1}$	Clock (Active LOW Going Edge) Input to Divide-by-Eight Section (LS197)
$\overline{MR}$	Master Reset (Active LOW) Input
$\overline{PL}$	Parallel Load (Active LOW) Input
P_0-P_3	Data Inputs
Q_0-Q_3	Outputs

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	- 0.5 to 7	V
V_I	Input Voltage. Applied to Input	- 0.5 to 15	V
V_O	Output Voltage, Applied to Output	- 0.5 to 10	V
I_I	Input Current, Into Inputs	- 30 to 5	mA
I_O	Output Current. Into Outputs	60	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS196/197XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

FUNCTIONAL DESCRIPTION

The LS196 and LS197 are asynchronous presettable decade and binary ripple counters. The LS196 Decade Counter is partitioned into divide-by-two and divide-by-five sections while the LS197 is partitioned into divide-by-two and divide-by-eight sections, with all section having a separate Clock input. In the counting modes, the state changes are initiated by the HIGH to LOW transition of the clock signals. State changes of the Q outputs, however, do not occur simultaneously bacause of the internal ripple delays. When using external logic to decode the Q outputs, designers should bear in mind that the unequal delays can lead to decoding spikes and thus a decoded signal should not be used as a clock or strobe. The $\overline{CP}_0$ input serves the Q_0 flip-flop in both circuit types while the $\overline{CP}_1$ serves the divide-by-five or divide-by-eight section. The Q_0 output is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input. With the input frequency connected to $\overline{CP}_0$ and Q_0 driving $\overline{CP}_1$, the LS197 form a strightforward module-16 counter, with Q0 the least significant output and Q_3 the most significant output.

The LS196 Decade Counter can be connecetd up to operate in two different count sequences, as indicated in the Table A. With the input frequency connected to $\overline{CP}_0$ and with Q_0 driving $\overline{CP}_1$, the circuit counts in the BCD (8, 4, 2, 1) sequence.

With the input frequency connected to $\overline{CP}_1$ and Q_3 driving $\overline{CP}_0$, Q_0 becomes the low frequency output and as a 50% duty cycle waveform. Note that the maximum counting rate is reduced in the later (biquinary) configuration because of the interstage gating delay within the divide-by-five section. The LS196 and LS197 have an asynchronous active LOW Master Reset input (MR) which overrides all other inputs and forces all outputs LOW. The counters are also asynchronously presettable. A LOW on the Parallel Load input (PL) overrides the clock inputs and loads the data from Parallel Data (P_0-P_3) inputs into flip-flops. While PL is LOW. the counters act as trasparent latches and any change in the P_n inputs will be reflected in the outputs.

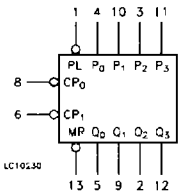
TRUTH TABLE

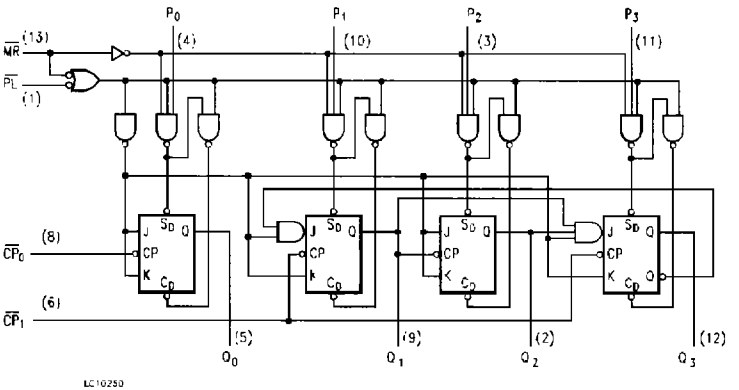
INPUTS			RESPONSE
$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	
L	X	X	Reset (Clear)
H	L	X	Parallel Load
H	H	⌐	Count

H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care. ⌐ = HIGH to LOW Clock Transition

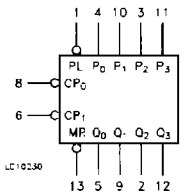
LOGIC DIAGRAMS

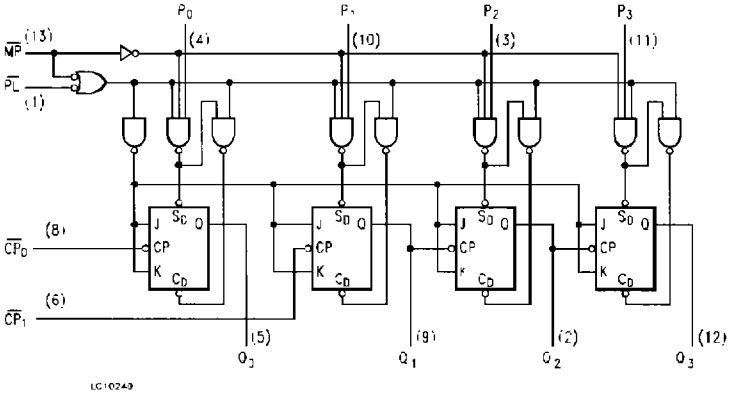
LS196





LS197





V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

TABLE A: LS196 COUNT SEQUENCES

DECADE (NOTE 1)					BI-QUINARY (NOTE 2)				
COUNT	Q_3	Q_2	Q_1	Q_0	COUNT	Q_0	Q_3	Q_2	Q_1
0	L	L	L	L	0	L	L	L	L
1	L	L	L	H	1	L	L	L	H
2	L	L	H	L	2	L	L	H	L
3	L	L	H	H	3	L	L	H	H
4	L	H	L	L	4	L	H	L	L
5	L	H	L	H	5	H	L	L	L
6	L	H	H	L	6	H	L	L	H
7	L	H	H	H	7	H	L	H	L
8	H	L	L	L	8	H	L	H	H
9	H	L	L	H	9	H	H	L	L

Notes: 1. Signal Applied to $\overline{CP}_0$, Q_0 connected to $\overline{CP}_1$
2. Signal Applied to $\overline{CP}_1$, Q_3 connecetd to $\overline{CP}_0$

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)	Unit
		Min.	Typ. (*)	Max.		
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs	V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs	V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA	V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table	V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
I_{IH}	Input HIGH Current $\overline{PL}$, P_0, P_1, P_2, P_3 $\overline{MR}$, $\overline{CP}_0$, $\overline{CP}_1$ (LS197) $\overline{CP}_1$ (LS196)			 20 40 80	V_{CC} = MAX, V_{IN} = 2.7 V	µA
	$\overline{PL}$, P_0, P_1, P_2, P_3 $\overline{MR}$, $\overline{CP}_0$, $\overline{CP}_1$ (LS197) $\overline{CP}_1$ (LS196)			0.1 0.2 0.4	V_{CC} = MAX, V_{IN} = 5.5 V	µA
I_{IL}	Input LOW Current $\overline{PL}$, P_0, P_1, P_2, P_3 $\overline{MR}$ $\overline{CP}_0$ $\overline{CP}_1$ (LS196) $\overline{CP}_1$ (LS197)			 - 0.36 - 0.72 - 2.4 - 2.8 - 1.3	V_{CC} = MAX, V_{IN} = 0.4 V	mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX V_{OUT} = 0 V	mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Note more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: T_A = 25 °C (L196)

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
f_{MAX}	Input Count Frequency	30	40		Figures 1	V_{CC} = 5.0 V C_L = 15 pF	MHz
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP_0}$ Input to Q_0 Outputs		8 13	15 20	Figures 1		ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP_1}$ Input to Q_1 Outputs		16 22	24 33			ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP_1}$ Input to Q_2 Outputs		38 41	57 62			ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP_1}$ Input to Q_3 Outputs		12 30	18 45			ns
t_{PLH} t_{PHL}	Propagation Delay, P_0, P_1, P_2, P_3 Inputs to Q_0, Q_1, Q_2, Q_3 Outputs		20 29	30 44	Figures 2		ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{PL}$ Inputs to Any Outputs		27 30	41 45	Figures 3		ns
t_{PHL}	Propagation Delay, $\overline{MR}$ Inputs to Any Outputs		34	51	Figures 4		ns

AC CHARACTERISTICS: T_A = 25 °C (LS197)

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
f_{MAX}	Input Count Frequency	30	40		Figures 1	V_{CC} = 5.0 V C_L = 15 pF	MHz
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP_0}$ Input to Q_0 Outputs		8 14	15 21	Figures 1		ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP_1}$ Input to Q_1 Outputs		12 23	19 35			ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP_1}$ Input to Q_2 Outputs		34 42	51 63			ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP_1}$ Input to Q_3 Outputs		55 63	78 95			ns
t_{PLH} t_{PHL}	Propagation Delay, P_0, P_1, P_2, P_3 Inputs to Q_0, Q_1, Q_2, Q_3 Outputs		18 29	27 44	Figures 2		ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{PL}$ Inputs to Any Outputs		26 30	39 45	Figures 3		ns
t_{PHL}	Propagation Delay, $\overline{MR}$ Inputs to Any Outputs		34	51	Figures 4		ns

AC SET-UP REQUIREMENTS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_W	$\overline{CP_0}$ Pulse Width	20			Figure 1	V_{CC} = 5.0 V	ns
t_W	$\overline{CP_1}$ Pulse Width	30					ns
t_W	$\overline{PL}$ Pulse Width	20			Figure 3		ns
t_W	$\overline{MR}$ Pulse Width	15			Figure 4		ns
t_sL	Set-Up Time LOW	15			Figure 6		ns
t_hL	Hold Time LOW	20					ns
t_sH	Set-Up Time HIGH	10					ns
t_hH	Hold Time HIGH	20					ns
t_{rec}	Recovery Time	30			Figure 5		ns

DEFINITION OF TERMS:

SET-UP TIME (t_s): is defined as the minimum time required for the corret logic level to be present at the logic input prior the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h): is defined as the minimum time following the clock transition from LOW to HIGH at which the logiclevel must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be relased prior to the clock transitio from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) : is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORM

Fig 1.

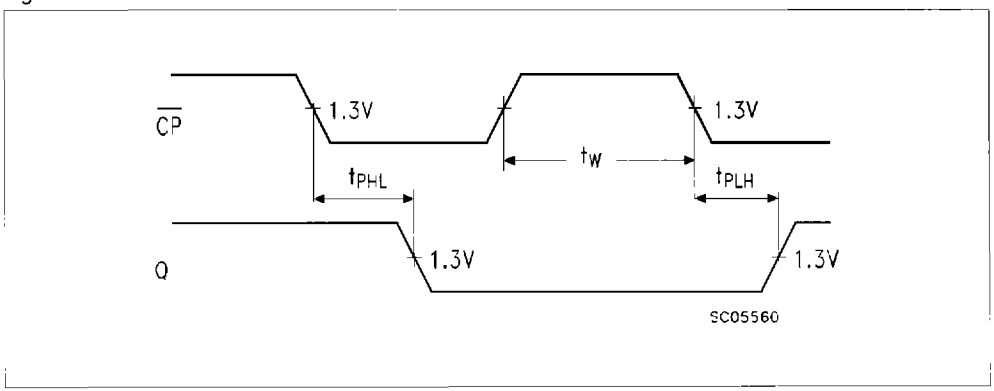


Fig 2.

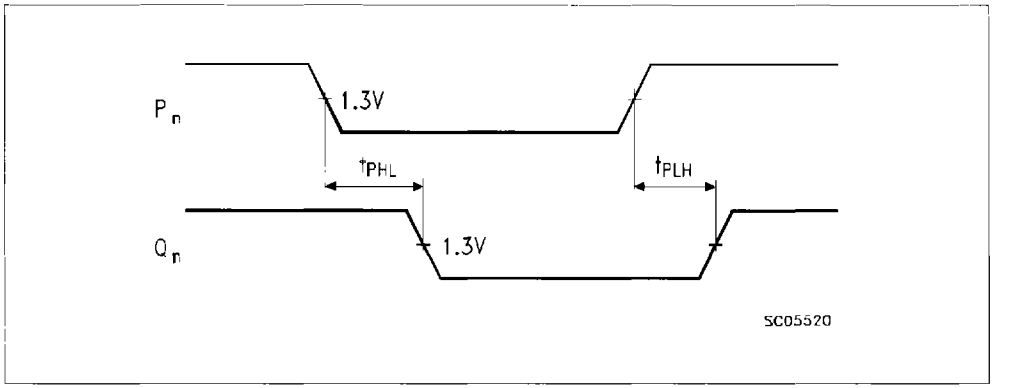


Fig 3.

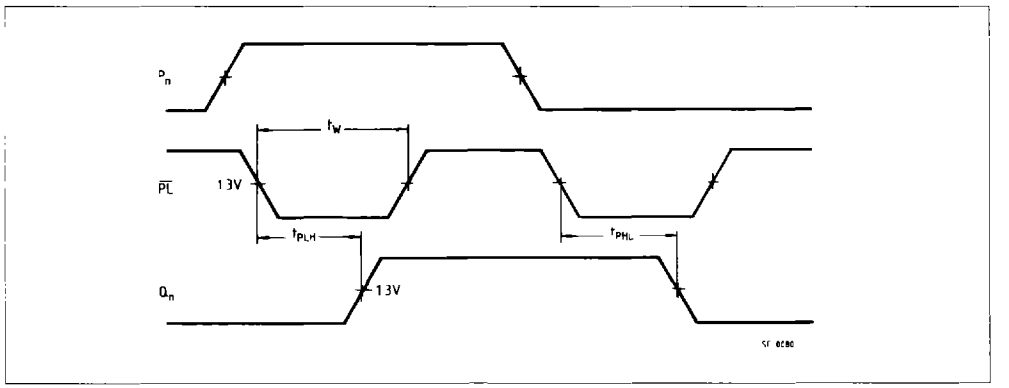


Fig 4.

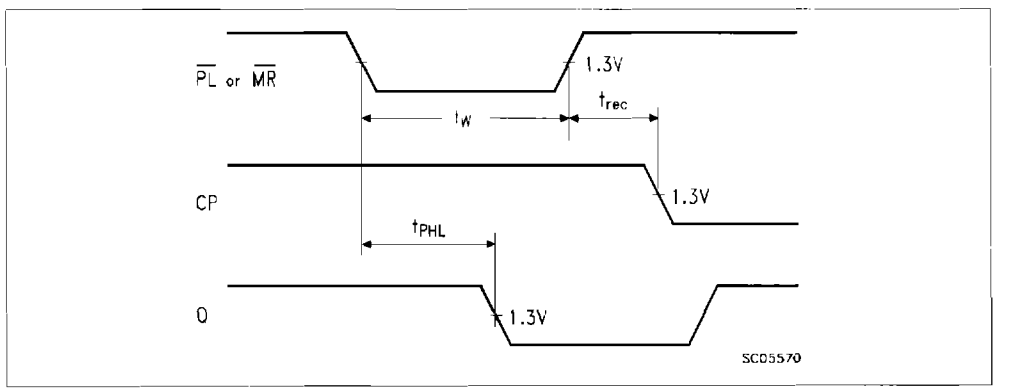
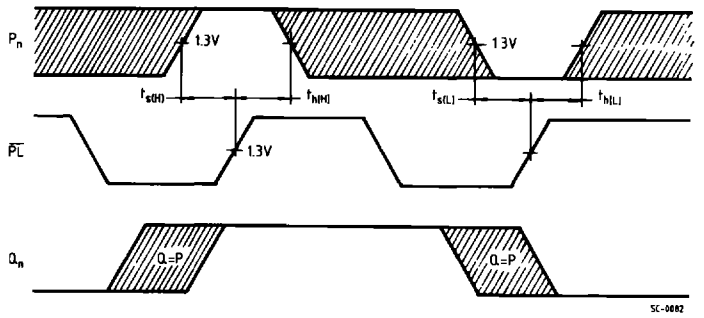


Fig 5.



The shaded areas indicate when the input is permitted to change for predictable output performance