

# 54F/74F550 • 54F/74F551

## Octal Registered Transceiver with Status Flags

### General Description

The 'F550 and 'F551 octal transceivers each contain two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own clock pulse and clock enable inputs, as well as a flag flip-flop that is set automatically as the register is loaded. Each flag flip-flop is provided with a clear input, and each register has a separate output enable control for its TRI-STATE® buffers. The separate clocks, flags and enables provide considerable flexibility as I/O ports for demand-response data transfer. The 'F550 is non-inverting; the 'F551 inverts data in both directions.

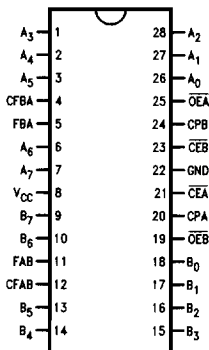
### Features

- 8-bit bidirectional I/O port with handshake
- Back-to-back registers for storage
- Register status flag flip-flops
- Separate edge-detecting clears for flags
- Inverting and non-inverting versions
- B outputs sink 64 mA (48 mA Mil)

**Ordering Code:** See Section 5

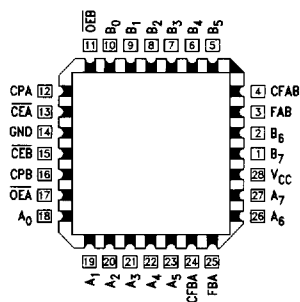
### Connection Diagrams

Pin Assignment for  
DIP, SOIC and Flatpak  
'F550



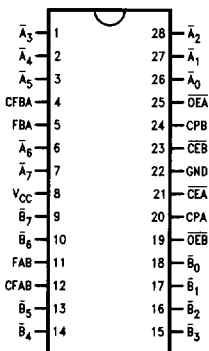
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Pin Assignment  
for LCC  
'F550



TL/F/9559-2

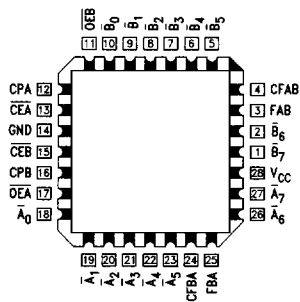
'F551



IEEE/IEC

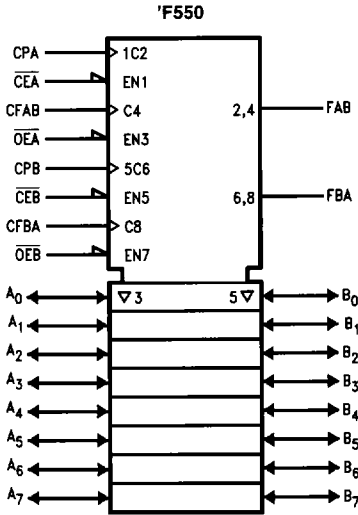
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'F551

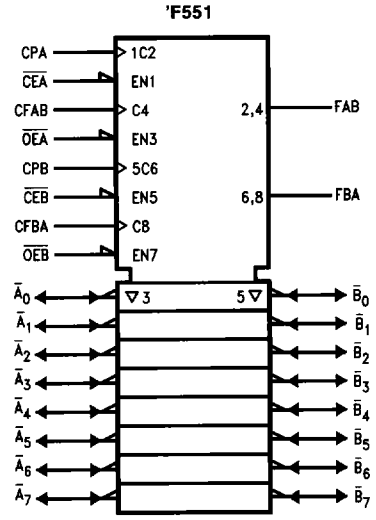


TL/F/9559-9

Connection Diagrams (Continued)

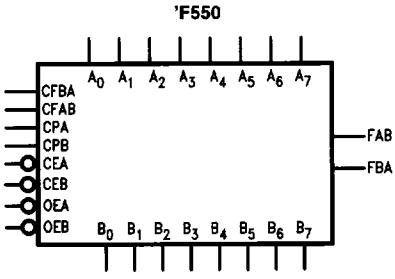


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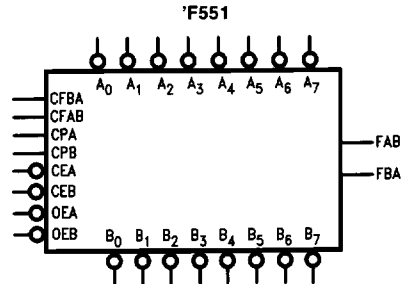


TL/F/9559-11

Logic Symbols



TL/F/9559-3



TL/F/9559-7

Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I <sub>H</sub> /I <sub>L</sub> Output I <sub>OH</sub> /I <sub>OL</sub>
CPA	A-to-B Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/ -0.6 mA
CPB	B-to-A Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/ -0.6 mA
CEA	A-to-B Clock Enable Input (Active LOW)	1.0/1.0	20 μA/ -0.6 mA
CEB	B-to-A Clock Enable Input (Active LOW)	1.0/1.0	20 μA/ -0.6 mA
OEA	A Output Enable Input (Active LOW)	1.0/1.0	20 μA/ -0.6 mA
OEB	B Output Enable Input (Active LOW)	1.0/1.0	20 μA/ -0.6 mA
CFAB	A-to-B Flag Clear Input (Active Rising Edge)	1.0/1.0	20 μA/ -0.6 mA
CFBA	B-to-A Flag Clear Input (Active Rising Edge)	1.0/1.0	20 μA/ -0.6 mA
A <sub>0</sub> -A <sub>7</sub>	A-to-B Data Inputs or TRI-STATE B-to-A Outputs	3.5/1.083	70 μA/ -0.65 mA
B <sub>0</sub> -B <sub>7</sub>	B-to-A Data Inputs or TRI-STATE A-to-B Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)
		3.5/1.083	70 μA/ -0.65 mA
		600/106.6 (80)	-12 mA/64 mA (48 mA)
FAB	A-to-B Status Flag Output (Active HIGH)	50/33.3	-1 mA/20 mA
FBA	B-to-A Status Flag Output (Active HIGH)	50/33.3	-1 mA/20 mA

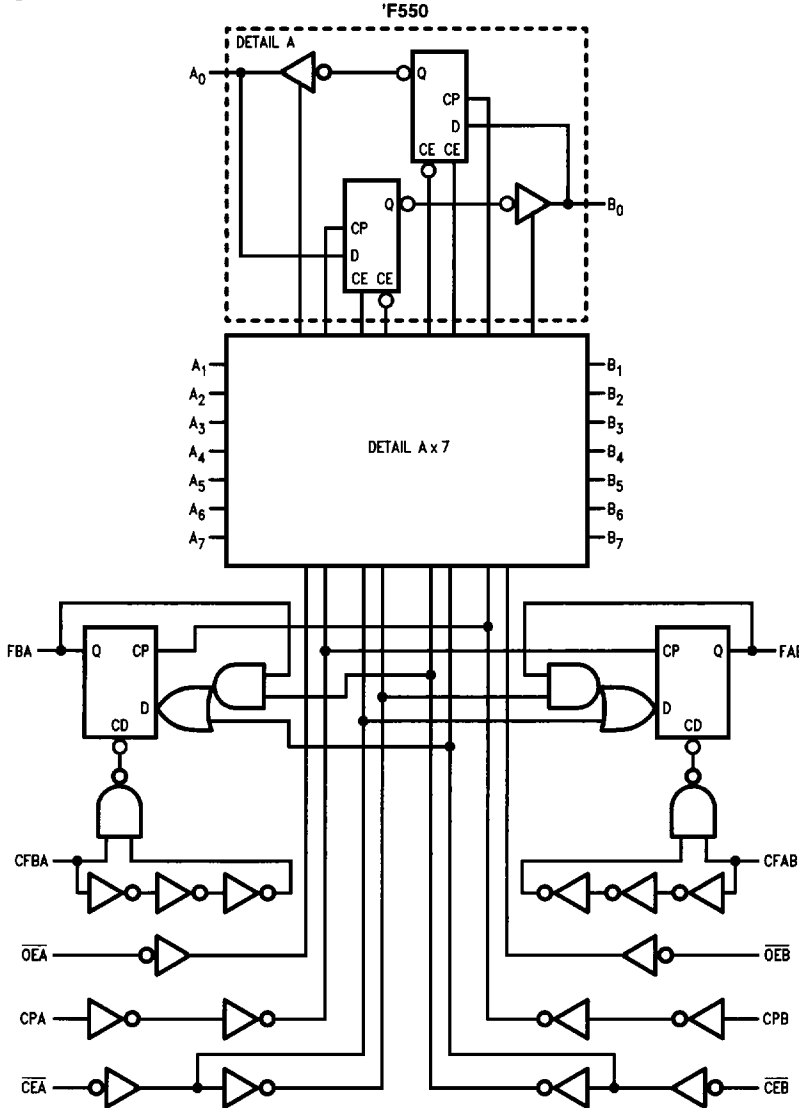
## Functional Description

Data applied to the A inputs is entered and stored on the rising edge of the A Clock Pulse (CPA), provided that the A Clock Enable ( $\overline{CEA}$ ) is LOW; simultaneously, the status flip-flop is set and the A-to-B flag (FAB) output goes HIGH. Data thus entered from the A inputs is present at the inputs to the B output buffers, but only appears on the B I/O pins when the B Output Enable ( $\overline{OEB}$ ) signal is made LOW. After the B output data is assimilated, the receiving system clears the A-to-B flag flip-flop by applying a LOW-to-HIGH tran-

sition to the CFAB input. Optionally, the  $\overline{OEB}$  and CFAB pins can be tied together and operated by one function from the receiving system.

Data flow from B-to-A proceeds in the same manner described for A-to-B flow. Inputs  $\overline{CEB}$  and CPB enter the B input data and set the B-to-A flag (FBA) output HIGH. A LOW signal on  $\overline{OEA}$  enables the A output buffers and a LOW-to-HIGH transition on CFBA clears the FBA flag.

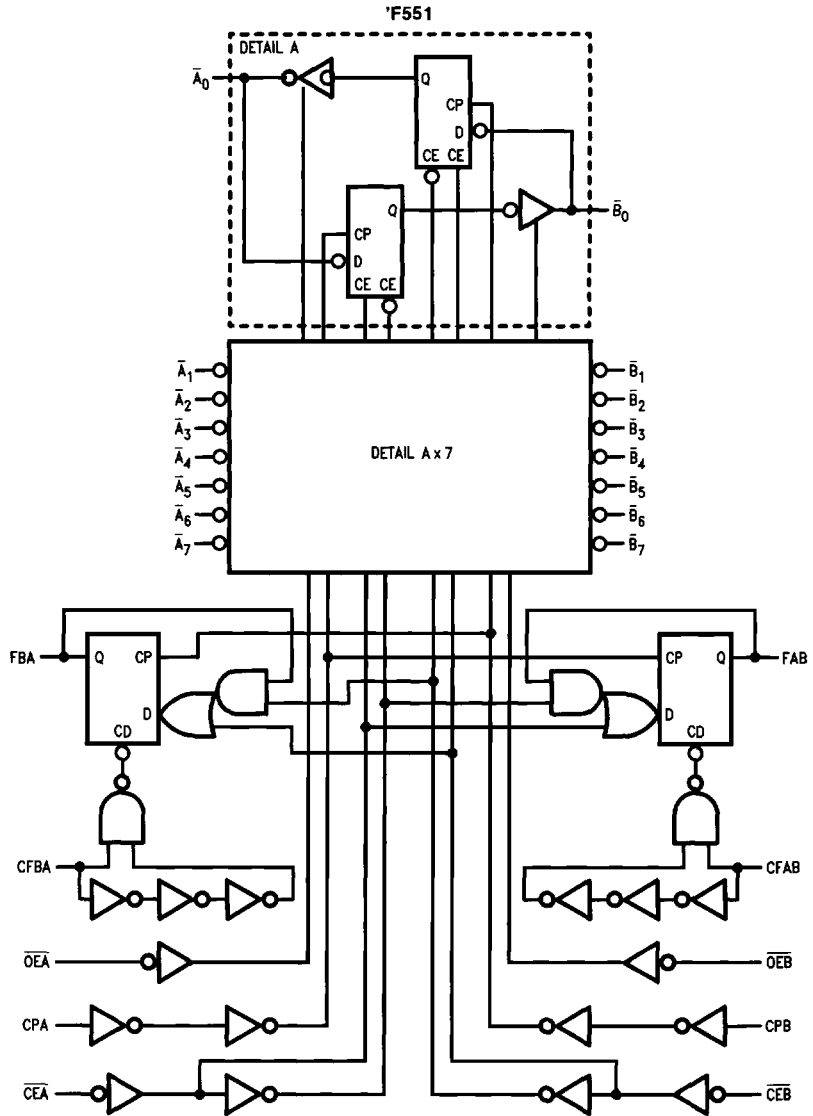
## Logic Diagrams



TL/F/9559-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Logic Diagrams (Continued)



TL/F/9559-12

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V <sub>CC</sub>	Conditions
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage					V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage					V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min		I <sub>OH</sub> = -1 mA (A <sub>0</sub> -A <sub>7</sub> )
		54F 10% V <sub>CC</sub>	2.4					I <sub>OH</sub> = -3 mA (A <sub>0</sub> -A <sub>7</sub> )
		54F 10% V <sub>CC</sub>	2.0					I <sub>OH</sub> = -12 mA (B <sub>0</sub> -B <sub>7</sub> )
		74F 10% V <sub>CC</sub>	2.5					I <sub>OH</sub> = -1 mA (A <sub>0</sub> -A <sub>7</sub> )
		74F 10% V <sub>CC</sub>	2.4					I <sub>OH</sub> = -3 mA (A <sub>0</sub> -A <sub>7</sub> )
		74F 10% V <sub>CC</sub>	2.0					I <sub>OH</sub> = -15 mA (B <sub>0</sub> -B <sub>7</sub> )
		74F 5% V <sub>CC</sub>	2.7					I <sub>OH</sub> = -1 mA (A <sub>0</sub> -A <sub>7</sub> )
V <sub>OL</sub>	Output Low Voltage	54F 10% V <sub>CC</sub>	0.5		V	Min		I <sub>OL</sub> = 20 mA (A <sub>0</sub> -A <sub>7</sub> )
		54F 10% V <sub>CC</sub>	0.55					I <sub>OL</sub> = 48 mA (B <sub>0</sub> -B <sub>7</sub> )
		74F 10% V <sub>CC</sub>	0.5					I <sub>OL</sub> = 24 mA (A <sub>0</sub> -A <sub>7</sub> )
		74F 10% V <sub>CC</sub>	0.55					I <sub>OL</sub> = 64 mA (B <sub>0</sub> -B <sub>7</sub> )
I <sub>IH</sub>	Input HIGH Current	54F	20.0		μA	Max		V <sub>IN</sub> = 2.7V (Non I/O Inputs)
		74F	5.0					
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F	100		μA	Max		V <sub>IN</sub> = 7.0V (Non I/O Inputs)
		74F	7.0					
I <sub>BVIT</sub>	Input HIGH Current Breakdown (I/O)	54F	1.0		mA	Max		V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )
		74F	0.5					
I <sub>CEx</sub>	Output HIGH Leakage Current	54F	250		μA	Max		V <sub>OUT</sub> = V <sub>CC</sub>
		74F	50					
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0		I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F	3.75		μA	0.0		V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current		-0.6		mA	Max		V <sub>IN</sub> = 0.5V (Non I/O Inputs)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current		70		μA	Max		V <sub>OUT</sub> = 2.7V (A <sub>0</sub> -A <sub>7</sub> , B <sub>0</sub> -B <sub>7</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current		-650		μA	Max		V <sub>OUT</sub> = 0.5V (A <sub>0</sub> -A <sub>7</sub> , B <sub>0</sub> -B <sub>7</sub> )

## DC Electrical Characteristics (Continued)

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
I <sub>OS</sub>	Output Short-Circuit Current	-60 -100		-150 -225	mA mA	Max Max	V <sub>OUT</sub> = 0V (A <sub>0</sub> -A <sub>7</sub> ) V <sub>OUT</sub> = 0V (B <sub>0</sub> -B <sub>7</sub> )
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current		84	140	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		105	140	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		102	140	mA	Max	V <sub>O</sub> = HIGH Z

## AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CPA or CPB to B <sub>n</sub> or A <sub>n</sub>	3.0 4.0	5.5 7.0	7.5 9.0			2.5 3.5	8.5 10.0	ns	2-3
t <sub>PLH</sub>	Propagation Delay CPA or CPB to FBA or FAB	3.5	6.0	8.0			3.0	9.0	ns	2-3
t <sub>PHL</sub>	Propagation Delay CFAB or CFBA to FAB or FBA	5.0	9.0	11.5			4.5	13.0	ns	2-3
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time OE <sub>A</sub> or OE <sub>B</sub> to A <sub>n</sub> or B <sub>n</sub>	2.5 3.5	5.5 7.0	7.5 9.5			2.0 3.0	8.5 10.5	ns	2-5
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time OE <sub>A</sub> or OE <sub>B</sub> to A <sub>n</sub> or B <sub>n</sub>	3.0 2.5	6.5 5.5	9.0 7.5			2.5 2.0	10.0 8.5		

## AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> , V <sub>CC</sub> = Mil		T <sub>A</sub> , V <sub>CC</sub> = Com			
		Min	Max	Min	Max	Min	Max		
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time, HIGH or LOW A <sub>n</sub> , B <sub>n</sub> to CPA, CPB	4.0 4.0				4.5 4.5		ns	2-6
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, HIGH or LOW A <sub>n</sub> , B <sub>n</sub> to CPA, CPB	2.0 2.0				2.5 2.5			
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time, HIGH or LOW CE <sub>A</sub> , CE <sub>B</sub> to CPA, CPB	1.0 4.0				1.5 4.5		ns	2-6
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, HIGH or LOW CE <sub>A</sub> , CE <sub>B</sub> to CPA, CPB	2.0 2.0				2.5 2.5			
t <sub>w</sub> (H) t <sub>w</sub> (L)	Pulse Width, HIGH or LOW CPA or CPB	3.0 3.0				3.5 3.5		ns	2-4
t <sub>w</sub> (H)	Pulse Width, HIGH CFAB or CFBA	3.0				3.5		ns	2-4
t <sub>rec</sub>	Recovery Time CFAB, CFBA to CPA, CPB	9.0				10.0		ns	2-6