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Status	Product Specification
ACL Products	

74AC/ACT11652

Octal transceiver/register with dual enable (3-State)

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11652 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11652 device is an octal transceiver/register featuring non-inverting 3-State bus compatible outputs in both send and receive directions, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data di-

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to B_n, or B_n to A_n	C_L = 50pF		5.6	6.9	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz; C_L = 50pF	Enabled	60	59	pF
			Disabled	14	14	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{IO}	I/O capacitance	V_O = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency, CP_x to A or B	C_L = 50pF		125	125	MHz

Note:

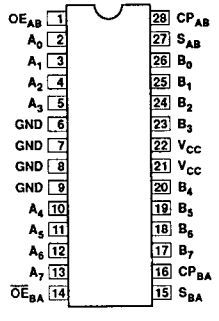
1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_i = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

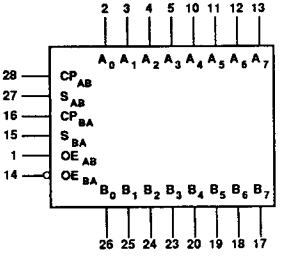
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11652N 74ACT11652N
28-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11652D 74ACT11652D

PIN CONFIGURATION

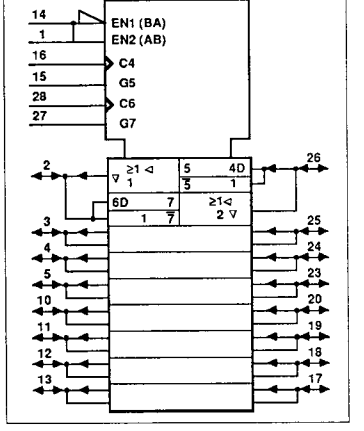
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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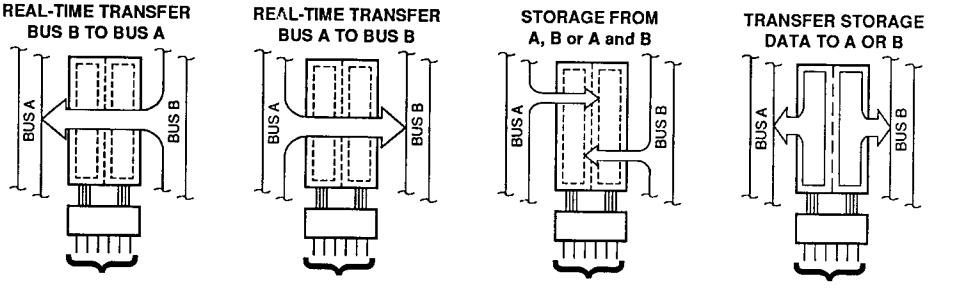
rectly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a High logic level. Output Enable (OE_{AB}, $\overline{OE}_{BA}$) and Select pins (S_{AB}, S_{BA}) are provided for bus management. In the transceiver mode, data present at the High-impedance port may be stored in either the A or B register or both.

Figure 1 demonstrates the four fundamental bus-management functions that can be performed. The select pins (S_{AB}, S_{BA}) determine whether data is stored or transferred through the device in real-time. The Output Enable pins (OE_{AB}, $\overline{OE}_{BA}$) determine the direction of the data flow.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OE_{AB}	A-to-B output enable input
14	$\overline{OE}_{BA}$	B-to-A output enable input (active Low)
28	CP_{AB}	A-to-B clock input
16	CP_{BA}	B-to-A clock input
27	S_{AB}	A-to-B select input
15	S_{BA}	B-to-A select input
2, 3, 4, 5, 10, 11, 12, 13	A_0 - A_7	A side inputs/outputs (3-state)
26, 25, 24, 23, 20, 19, 18, 17	B_0 - B_7	B side inputs/outputs (3-state)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage



OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	L	X	X	X	L

OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
H	H	X	X	L	X

OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
H	L	H or L	H or L	H	H

Figure 1

Octal transceiver/register with dual enable (3-State)

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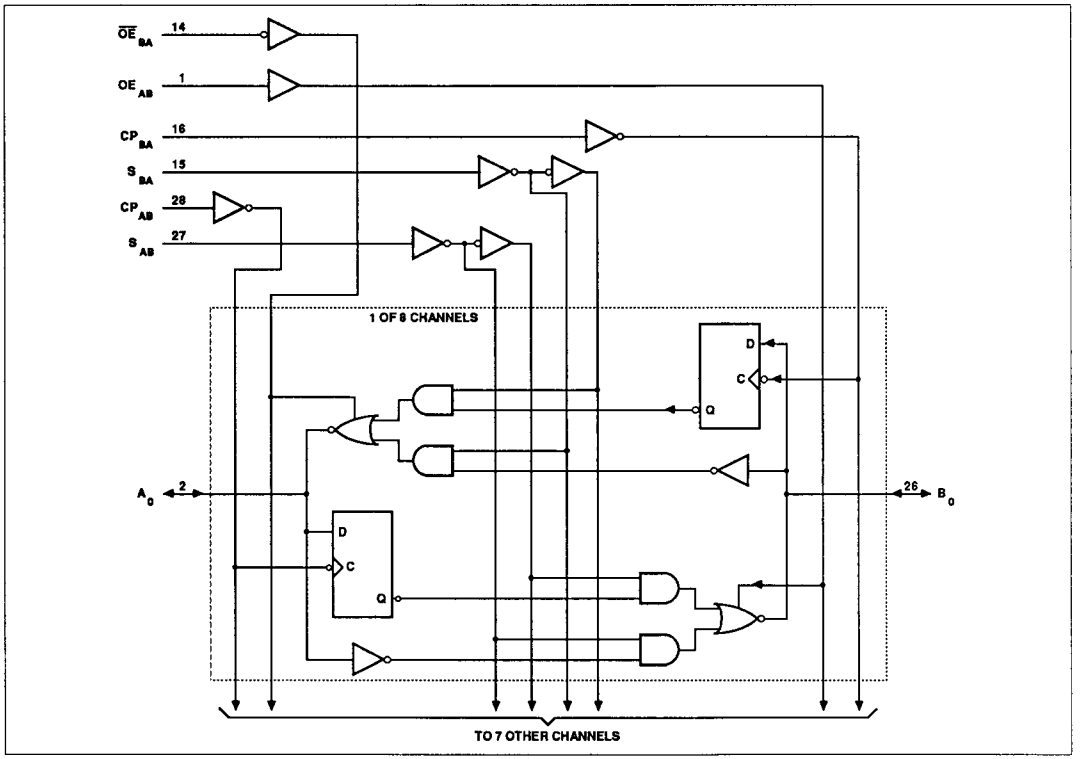
FUNCTION TABLE

OPERATING MODE	INPUTS						DATA I/O*	
	OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	$\overline{A}_0 - \overline{A}_7$	$\overline{B}_0 - \overline{B}_7$
Isolation Store A and B data	L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input
Store A, Hold B	X	H	↑	H or L	X	X	Input	unspecified*
Store A in both registers	H	H	↑	↑	L	X	Input	Output
Hold A, Store B	L	X	H or L	↑	X	X	unspecified*	Input
Store B in both registers	L	L	↑	↑	X	L	Output	Input
Real time B data to A bus Stored B data to A bus	L L	L L	X X	X H or L	X X	L H	Output	Input
Real time A data to B bus Stored A data to B bus	H H	H H	X H or L	X X	L H	X X	Input	Output
Stored A data to B bus Stored B data to A bus	H	L	H or L	H or L	H	H	Output	Output

* The data output functions may be enabled or disabled by various signals at the OE_{AB} and the $\overline{OE}_{BA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

un = unspecified
H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11652			74ACT11652			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±400	mA
	DC ground current		±400	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11652				74ACT11652				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	$V_I = V_{CC}$ or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	$V_I = V_{IL}$ or V_{IH}, $V_O = V_{CC}$ or GND		5.5		±0.5		5.0		±0.5		5.0	μA
I_{CC}	Quiescent supply current	$V_I = V_{CC}$ or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

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AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11652					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	65	80		65		MHz
t_{PLH} t_{PHL}	Propagation delay CP_{AB} or CP_{BA} to A_n or B_n	1	4.3 5.3	11.2 13.1	14.3 16.2	4.3 5.3	16.2 17.8	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	3	2.9 3.9	8.5 10.3	11.1 12.9	2.9 3.9	12.9 14.2	ns
t_{PLH} t_{PHL}	Propagation delay (A_n or B_n High) S_{BA} or S_{AB} to A_n or B_n	2	3.4 4.7	9.4 11.5	12.0 14.3	3.4 4.7	13.7 15.6	ns
t_{PLH} t_{PHL}	Propagation delay (A_n or B_n Low) S_{BA} or S_{AB} to A_n or B_n	3	3.9 4.8	10.5 12.1	13.3 16.3	3.9 4.8	14.9 17.7	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_{BA}$ to A_n	5	4.3 5.2	11.1 14.4	14.5 19.8	4.3 5.2	16.5 22.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to A_n	5	3.7 3.5	6.4 6.0	8.1 7.8	3.7 3.5	8.5 8.2	ns
t_{PZH} t_{PZL}	Output Enable time OE_{AB} to B_n	5	4.7 5.6	11.6 14.8	15.0 19.9	4.7 5.6	16.9 21.9	ns
t_{PHZ} t_{PLZ}	Output disable time OE_{AB} to B_n	5	4.0 3.5	6.6 6.1	8.2 7.7	4.0 3.5	8.6 8.0	ns
t_s	Setup time (High or Low) A_n or B_n to CP_{AB} or CP_{BA}	4	6.0			6.0		ns
t_h	Hold time (High or Low) A_n or B_n to CP_{AB} or CP_{BA}	4	1.0			1.0		ns
t_w	Pulse width (High or Low) CP_{AB} or CP_{BA}	1	7.7			7.7		ns

Octal transceiver/register with dual enable (3-State)

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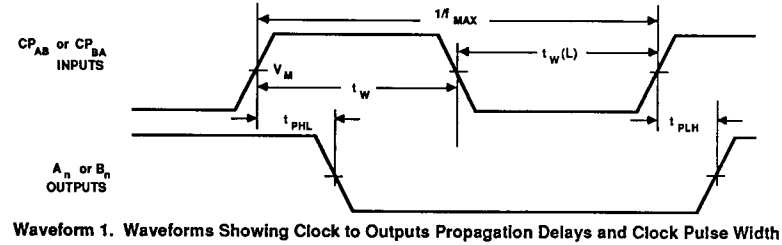
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11652					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP_{AB} or CP_{BA} to A_n or B_n	1	3.6 4.4	6.7 7.8	9.5 10.8	3.6 4.4	10.7 12.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	3	2.4 3.1	5.2 6.0	7.6 8.7	2.4 3.1	8.6 9.6	ns
t_{PLH} t_{PHL}	Propagation delay (A_n or B_n High) S_{BA} or S_{AB} to A_n or B_n	2	2.9 3.8	5.6 6.9	8.1 9.6	2.9 3.8	9.1 10.7	ns
t_{PLH} t_{PHL}	Propagation delay (A_n or B_n Low) S_{BA} or S_{AB} to A_n or B_n	3	3.3 4.0	6.2 7.1	8.8 9.9	3.3 4.0	9.9 10.9	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_{BA}$ to A_n	5	3.3 4.2	6.6 7.4	9.6 10.9	3.3 4.2	10.9 12.2	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to A_n	5	3.6 3.3	5.5 5.0	7.2 6.7	3.6 3.3	7.6 7.1	ns
t_{PZH} t_{PZL}	Output Enable time OE_{AB} to B_n	5	4.1 4.6	7.2 7.9	10.1 11.1	4.1 4.6	11.3 12.3	ns
t_{PHZ} t_{PLZ}	Output disable time OE_{AB} to B_n	5	3.9 3.4	5.6 5.2	7.3 6.8	3.9 3.4	7.6 7.2	ns
t_s	Setup time (High or Low) A_n or B_n to CP_{AB} or CP_{BA}	4	4.5			4.5		ns
t_h	Hold time (High or Low) A_n or B_n to CP_{AB} or CP_{BA}	4	1.0			1.0		ns
t_w	Pulse width (High or Low) CP_{AB} or CP_{BA}	1	5.0			5.0		ns

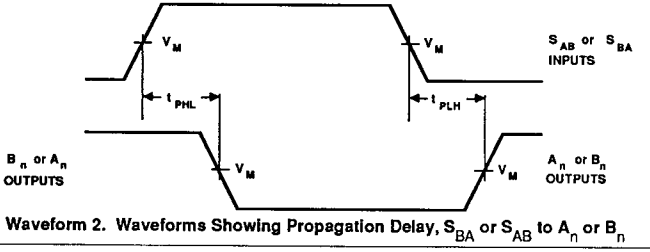
AC ELECTRICAL CHARACTERISTICS AT 5.5V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11652					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP_{AB} or CP_{BA} to A_n or B_n	1	5.4 6.1	8.4 9.4	11.8 13.1	5.4 6.1	13.1 14.4	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	3	3.8 3.4	7.0 6.7	9.9 10.7	3.8 3.4	11.1 11.6	ns
t_{PLH} t_{PHL}	Propagation delay (A_n or B_n High) S_{BA} or S_{AB} to A_n or B_n	2	2.8 5.5	6.2 8.7	10.1 12.1	2.8 5.5	11.0 13.3	ns
t_{PLH} t_{PHL}	Propagation delay (A_n or B_n Low) S_{BA} or S_{AB} to A_n or B_n	3	4.9 3.9	7.8 7.5	11.0 11.6	4.9 3.9	12.2 12.6	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_{BA}$ to A_n	5	3.3 4.1	7.2 7.8	11.4 12.6	3.3 4.1	12.6 13.8	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to A_n	5	5.2 4.8	7.2 6.7	9.3 8.6	5.2 4.8	9.9 9.3	ns
t_{PZH} t_{PZL}	Output Enable time OE_{AB} to B_n	5	5.1 5.8	9.1 9.7	13.4 14.2	5.1 5.8	15.2 16.1	ns
t_{PHZ} t_{PLZ}	Output disable time OE_{AB} to B_n	5	3.4 3.1	6.8 6.0	9.7 8.8	3.4 3.1	10.3 9.3	ns
t_s	Setup time (High or Low) A_n or B_n to CP_{AB} or CP_{BA}	4	4.0			4.0		ns
t_h	Hold time (High or Low) A_n or B_n to CP_{AB} or CP_{BA}	4	2.5			2.5		ns
t_w	Pulse width (High or Low) CP_{AB} or CP_{BA}	1	5.0			5.0		ns

AC WAVEFORMS

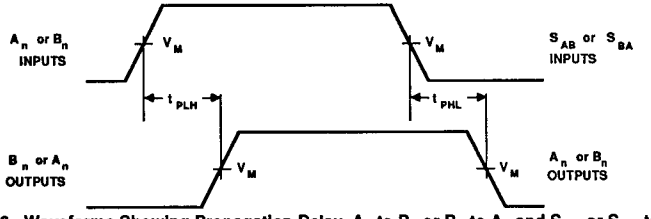


Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays and Clock Pulse Width

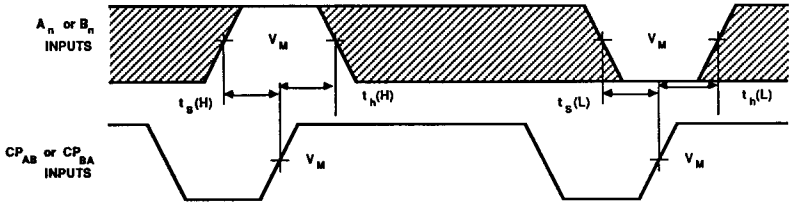


Waveform 2. Waveforms Showing Propagation Delay, S_{BA} or S_{AB} to A_n or B_n

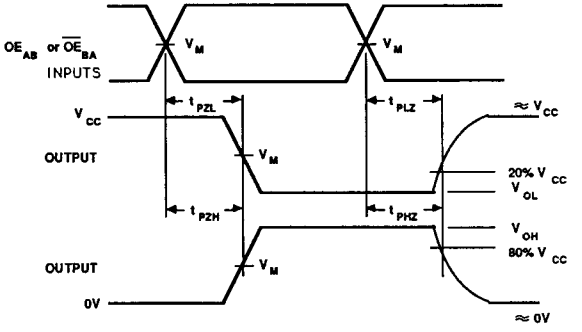
AC WAVEFORMS (Continued)



Waveform 3. Waveforms Showing Propagation Delay, A_n to B_n or B_n to A_n and S_{BA} or S_{AB} to A_n or B_n



Waveform 4. Waveforms Showing the Data Setup and Hold Times



Waveform 5. Waveforms Showing 3-State Output Enable and Disable Times

Octal transceiver/register with dual enable (3-State)

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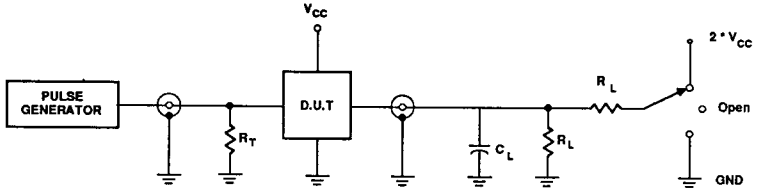
WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*V_{CC}
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns