

SRAM

16K x 4 SRAM

WITH SEPARATE INPUTS
AND OUTPUTS

FAST SRAM

FEATURES

- High speed: 8, 10, 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE1}$, $\overline{CE2}$ and \overline{OE} options
- All inputs and outputs are TTL compatible
- MT5C6406 – output tracks input during WRITE
- MT5C6407 – output High-Z during WRITE

OPTIONS

- Timing
 - 8ns access (preliminary)
 - 10ns access
 - 12ns access
 - 15ns access
 - 20ns access
 - 25ns access
 - 35ns access

MARKING

- Packages

Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ

Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.
- 2V data retention L
- Temperature

Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

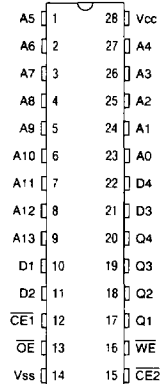
GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

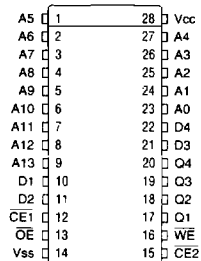
For flexibility in high-speed memory applications, Micron offers chip enable (\overline{CE}) on all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design. The x4 configuration features separate data input and output.

PIN ASSIGNMENT (Top View)

28-Pin DIP (A-9)



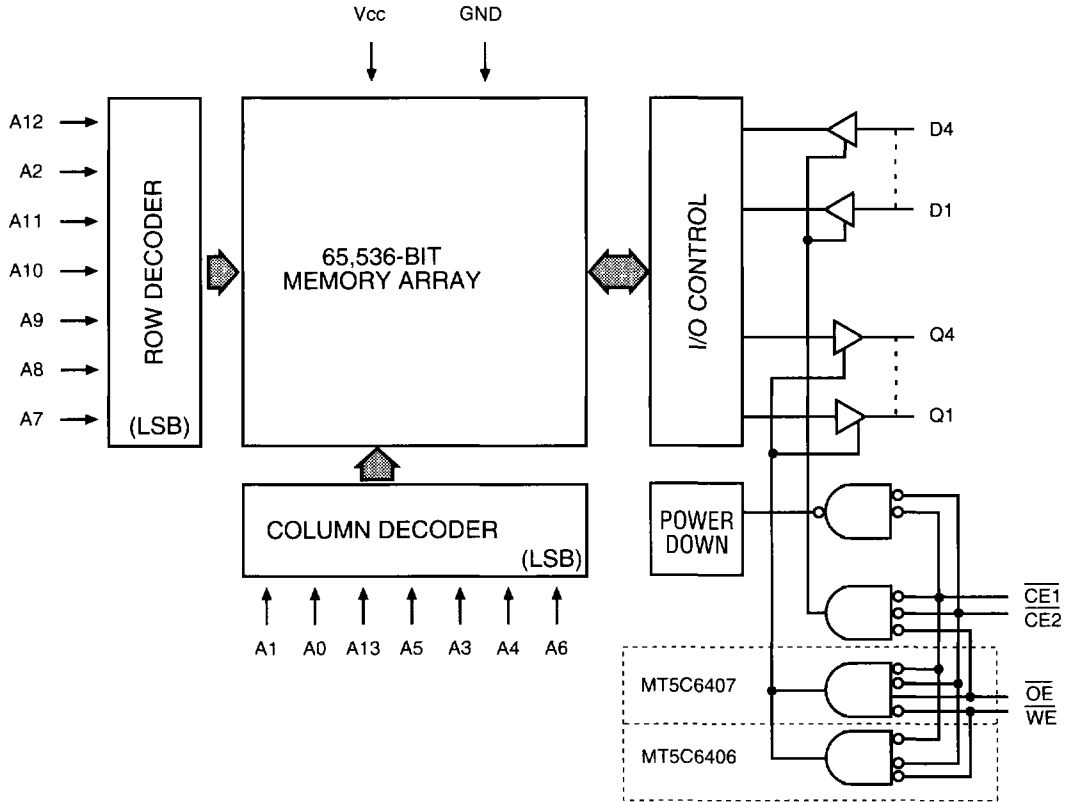
28-Pin SOJ (E-8)



Writing to these devices is accomplished when write enable (\overline{WE}) and \overline{CE} inputs are both LOW. Reading is accomplished when \overline{WE} remains HIGH and \overline{CE} goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	CE1	CE2	OE	WE	OUTPUT	POWER
STANDBY	H	X	X	X	HIGH-Z	STANDBY
STANDBY	X	H	X	X	HIGH-Z	STANDBY
READ	L	L	L	H	Q	ACTIVE
READ	L	L	H	H	HIGH-Z	ACTIVE
WRITE (1)	L	L	X	L	HIGH-Z	ACTIVE
WRITE (2)	L	L	L	L	D	ACTIVE
WRITE (2)	L	L	H	L	HIGH-Z	ACTIVE

NOTE: 1. MT5C6407 ONLY
2. MT5C6406 ONLY

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss -1V to +7V
 Storage Temperature (Plastic) -55°C to +150°C
 Power Dissipation 1W
 Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V _{IH}	2.2	V _{CC} +1	V	1
Input Low (Logic 0) Voltage		V _{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V _{IN} ≤ V _{CC}	I _{LI}	-5	5	μA	
Output Leakage Current	Output(s) Disable 0V ≤ V _{OUT} ≤ V _{CC}	I _{LO}	-5	5	μA	
Output High Voltage	I _{OH} = -4.0mA	V _{OH}	2.4		V	1
Output Low Voltage	I _{OL} = 8.0mA	V _{OL}		0.4	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX							UNITS	NOTES
				-8	-10	-12	-15	-20	-25	-35		
Power Supply Current: Operating	$\overline{CE} \leq V_{IL}; V_{CC} = \text{MAX}$ f = MAX = 1/1RC Outputs Open	I _{CC}	65	160	150	140	120	110	100	90	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \geq V_{IH}; V_{CC} = \text{MAX}$ f = MAX = 1/1RC Outputs Open	I _{SB1}	20	55	50	45	40	35	30	25	mA	14
	$\overline{CE} \geq V_{CC} - 0.2V; V_{CC} = \text{MAX}$ V _{IL} ≤ V _{SS} + 0.2V V _{IH} ≥ V _{CC} - 0.2V; f = 0	I _{SB2}	0.4	3	3	3	3	3	3	3	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T _A = 25°C, f = 1 MHz V _{CC} = 5V	C _I	5	pF	4
Output Capacitance		C _O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

FAST SRAM

DESCRIPTION	SYM	-8*		-10		-12		-15		-20		-25		-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle																	
READ cycle time	¹ RC	8		10		12		15		20		25		35		ns	
Address access time	¹ AA		8		10		12		15		20		25		35	ns	
Chip Enable access time	¹ ACE		7		9		10		12		15		20		30	ns	
Output hold from address change	¹ OH	3		3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	¹ LZCE	2		2		2		3		5		5		5		ns	
Chip disable to output in High-Z	¹ HZCE		4		5		6		7		8		8		8	ns	6, 7
Chip Enable to power-up time	¹ PU	0		0		0		0		0		0		0		ns	
Chip disable to power-down time	¹ PD		8		10		12		15		20		25		35	ns	
Output Enable access time	¹ AOE		3		4		5		6		7		8		15	ns	
Output Enable to output in Low-Z	¹ LZOE	0		0		0		0		0		0		0		ns	
Output disable to output in High-Z	¹ HZOE		4		4		5		6		7		8		8	ns	6
WRITE Cycle																	
WRITE cycle time	¹ WC	8		10		12		15		20		25		35		ns	
Chip Enable to end of write	¹ CW	8		9		10		12		15		20		25		ns	
Address valid to end of write	¹ AW	8		9		11		12		15		20		25		ns	
Address setup time	¹ AS	0		0		0		0		0		0		0		ns	
Address hold from end of write	¹ AH	0		0		0		0		0		0		0		ns	
WRITE pulse width	¹ WP	7		8		9		12		15		18		20		ns	
Data setup time	¹ DS	5		6		7		8		10		10		12		ns	
Data hold time	¹ DH	0		0		0		0		0		0		0		ns	
Write disable to output in Low-Z	¹ LZWE	2		2		2		2		2		2		2		ns	
Write Enable to output in High-Z	¹ HZWE		4		5		5		6		8		8		8	ns	6
Write Enable to output valid	¹ AWE		10		12		14		17		20		25		35	ns	
Data valid to output valid	¹ ADV		10		12		14		17		20		25		35	ns	

*These specifications are preliminary.

AC TEST CONDITIONS

Input pulse levels	V _{ss} to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

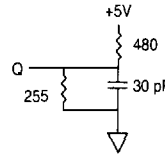


Fig. 1 OUTPUT LOAD EQUIVALENT

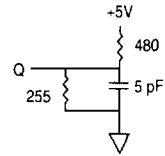


Fig. 2 OUTPUT LOAD EQUIVALENT

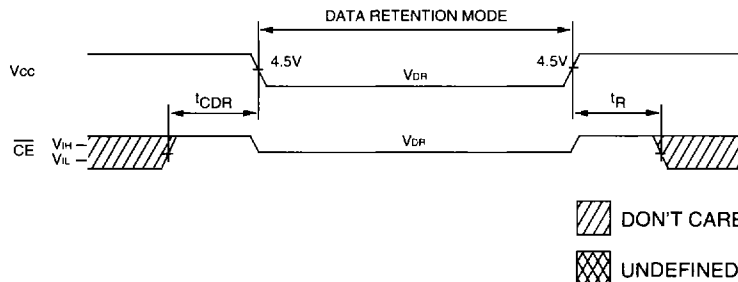
NOTES

1. All voltages referenced to V_{ss} (GND).
2. -3V for pulse width < 20ns.
3. I_{cc} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^tHZCE, ^tHZWE and ^tHZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^tHZCE is less than ^tLZCE and ^tHZWE is less than ^tLZWE.
8. \overline{WE} is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^tRC = Read Cycle Time.
12. Chip enable (\overline{CE}) and write enable (\overline{WE}) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications, refer to page 1-173.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

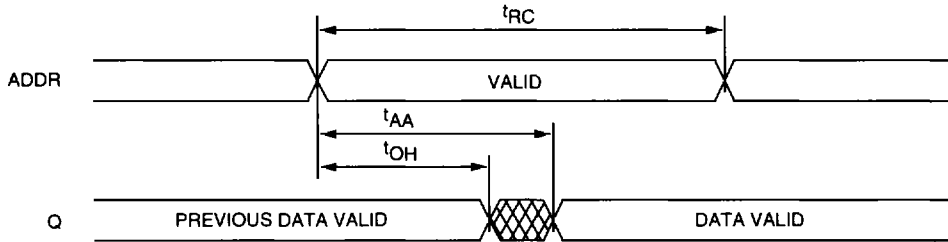
DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V _{cc} for Retention Data		V _{DR}	2		—	V	
Data Retention Current	$\overline{CE} \geq (V_{cc} - 0.2V)$ $V_{IN} \geq (V_{cc} - 0.2V)$ or $\leq 0.2V$	V _{cc} = 2V		95	250	μA	
		V _{cc} = 3V		125	400	μA	
Chip Deselect to Data Retention Time		^t CDR	0		—	ns	4
Operation Recovery Time		^t R	^t RC			ns	4, 11

LOW V_{cc} DATA RETENTION WAVEFORM

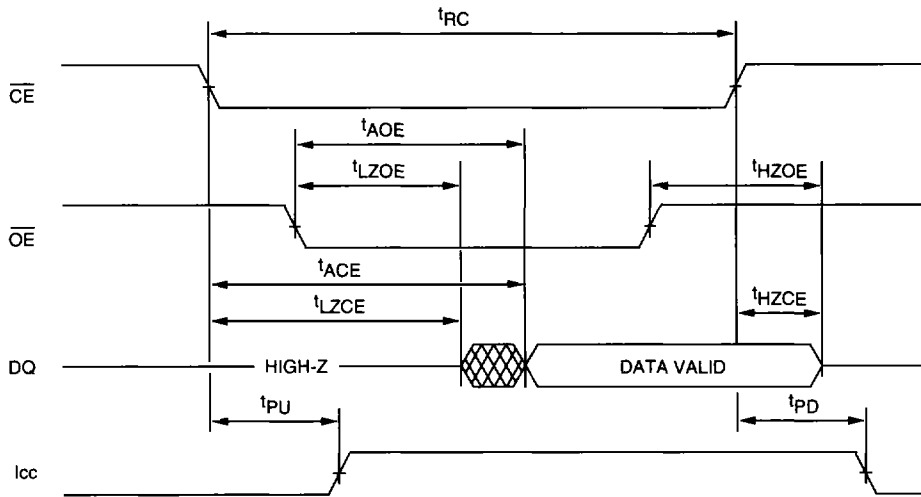


DON'T CARE
 UNDEFINED

READ CYCLE NO. 1 8, 9

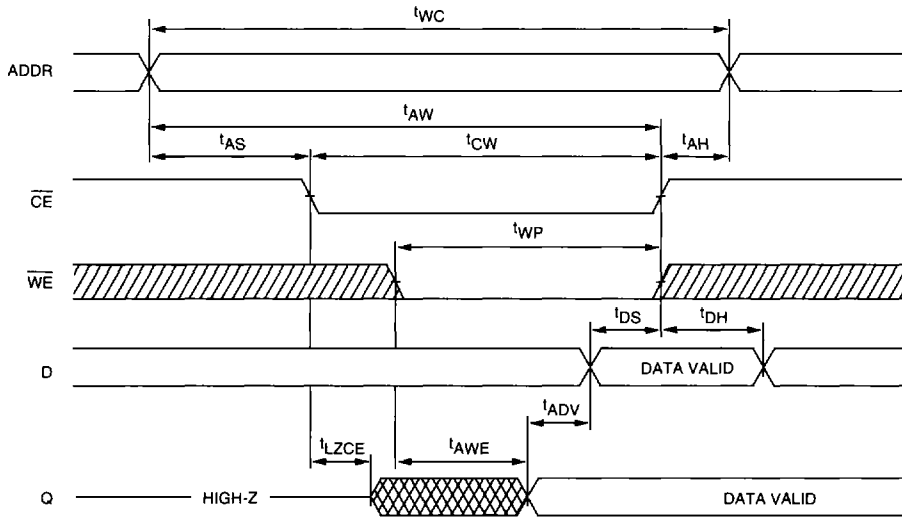


READ CYCLE NO. 2 7, 8, 10

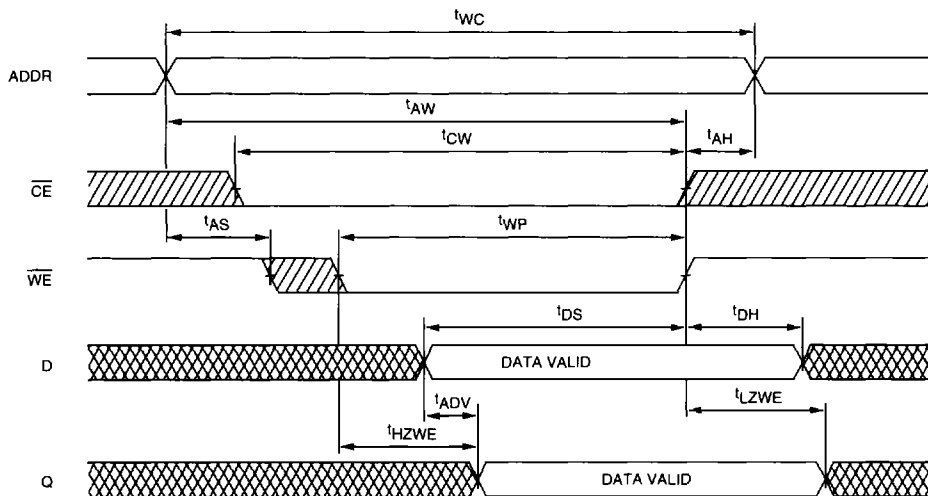




 DON'T CARE
 UNDEFINED

WRITE CYCLE NO. 1
(Chip Enable Controlled)



WRITE CYCLE NO. 2
(Write Enable Controlled) 7, 12



 DON'T CARE
 UNDEFINED