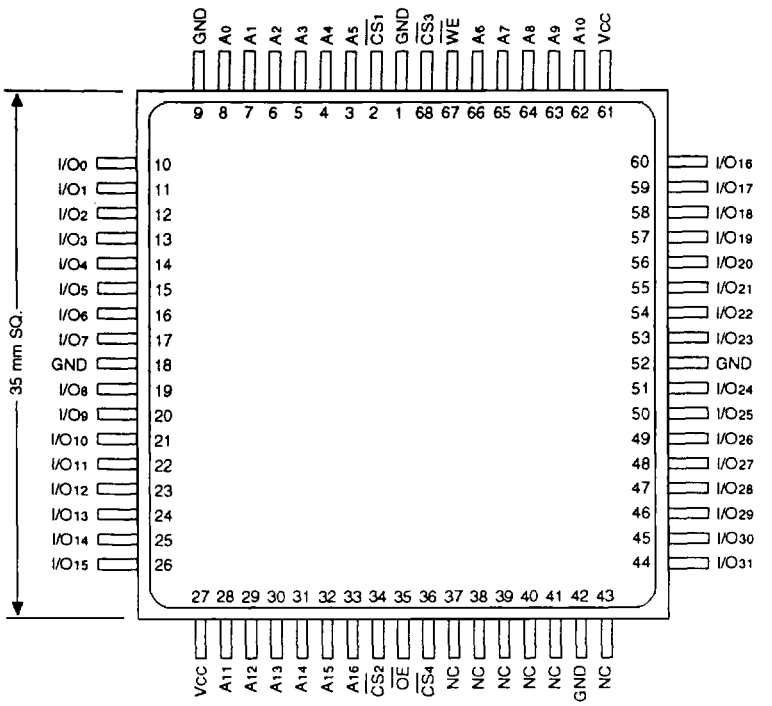


FIGURE 1 — Pin Configuration

I/O_{0-31}	Data Inputs/Outputs
A_{0-16}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
GND	Ground

Pin Description

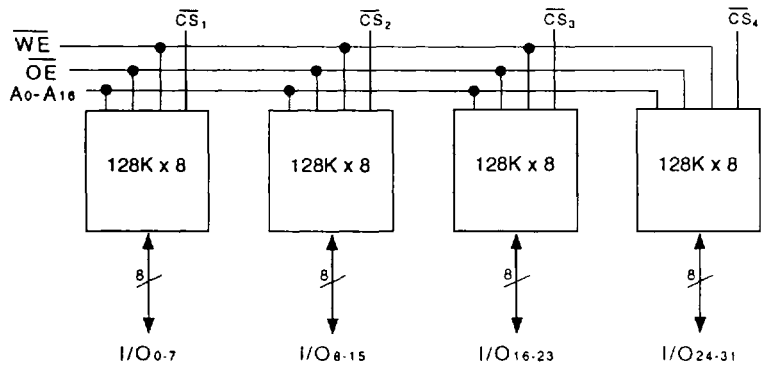


FIGURE 2 — Block Diagram

WS-128K32-XG4X

Advanced*
4 Megabit CMOS SRAM Module

FEATURES

- Access Times of 25nS to 120nS
- 68 lead, 35 mm Gull Wing Ceramic QFP
- User Configurable as 128Kx32, 256Kx16 or 512Kx8
- Battery Back-Up Operation
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- Low Power CMOS Fully Static Design
- 5 Volt Power Supply
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation

DESCRIPTION

The White Technology WS-128K32-XG4X is a 4-megabit CMOS SRAM module organized as 128K words by 32 bits; 256K x 16 or 512K x 8. The module is constructed on a ceramic substrate, hermetically sealed with a welded metal cover, on a 35mm square gull wing package, utilizing four 128K x 8 SRAM devices.

The WS-128K32-XG4X is available with access times of 25 to 120nS over the military temperature ranges.

* This data sheet describes a product under development and is subject to change without notice.

WHITE012

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Commercial	Military	Unit
Operating Temperature	T_A	0 to +70	-55 to +125	°C
Storage Temperature	T_{STG}	-40 to +85	-65 to +150	°C
Signal Voltage Relative to GND	V_G	-0.5 to +7.0	-0.5 to +7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}(1)	-0.5	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C

(1) V_{IL} (min.) = 3.0V for pulse width less than 20nS.

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby (deselect/power down)
L	L	H	Read	Data Out	Active
L	H	H	Read	High Z	Active (deselect)
L	X	L	Write	Data In	Active

CAPACITANCE

(@ T_A = 25°C)

Parameter	Symbol	Condition	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1.0MHz	30	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V, f = 1.0MHz	30	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Sym	Conditions	-25		-35		-45		-55		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = Max, V_{IN} = GND or V_{CC}		15		15		15		15	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		15		15		15		15	µA
Operating Supply Current x 32 Mode	I_{CC} x 32	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		400		400		350		350	mA
Operating Supply Current x 16 Mode	I_{CC} x 16	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		280		280		250		250	mA
Operating Supply Current x 8 Mode	I_{CC} x 8	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		150		150		130		130	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{CC}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		60		60		40		35	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA, V_{CC} = Min		0.4		0.4					V
		I_{OL} = 2.1mA, V_{CC} = Min						0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, V_{CC} = Min	2.4		2.4						V
		I_{OH} = -1.0mA, V_{CC} = Min					2.4		2.4		V

Parameter	Sym	Conditions	-70		-85		-100		-120		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = Max, V_{IN} = GND or V_{CC}		15		15		15		15	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		15		15		15		15	µA
Operating Supply Current x 32 Mode	I_{CC} x 32	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		300		300		250		250	mA
Operating Supply Current x 16 Mode	I_{CC} x 16	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		225		225		200		200	mA
Operating Supply Current x 8 Mode	I_{CC} x 8	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		120		80		70		70	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{CC}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		7		7		5		5	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA		0.4		0.4		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA	2.4		2.4		2.4		2.4		V

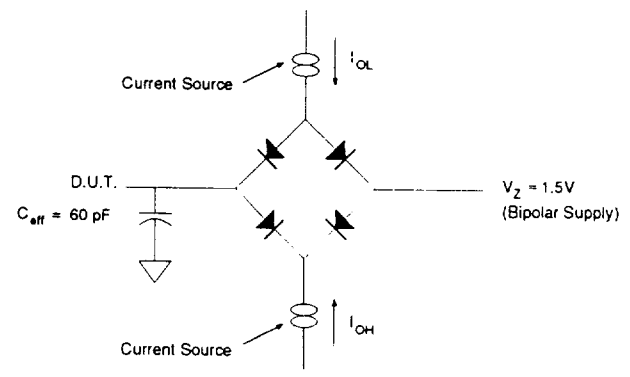


FIGURE 3 — AC Test Circuit

AC TEST CONDITIONS

Parameter	Typ.	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:

Vz is programmable from -2V to +7V

I_{OL} & I_{OH} programmable from 0 to 16mA

Tester Impedance Z_O = 75 Ω

Vz is typically the midpoint of V_{OH} and V_{OL} (i.e. (2.4 + 0.4)/2 = 1.4V)

I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.

ATE Tester Includes Jig Capacitance

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol	-25		-35		-45		-55		Units
Read Cycle		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		45		55		nS
Address Access Time	t_{AA}		25		35		45		55	nS
Data Hold from Address Change	t_{OH}	4		4		4		4		nS
Chip Select Access	t_{ACS}		25		35		45		55	nS
Output Enable to Output Valid	t_{OE}		15		20		25		30	nS
Chip Select to Output in Low Z	t_{CLZ}[1]	5		5		5		5		nS
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		0		nS
Chip Deselect to Output in High Z	t_{CHZ}[1]		12		15		20		25	nS
Output Disable to Output in High Z	t_{OHZ}[1]		12		15		20		25	nS

1. This parameter is guaranteed by design but not tested.

Parameter	Symbol	-70		-85		-100		-120		Units
Read Cycle		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		85		100		120		nS
Address Access Time	t_{AA}		70		85		100		120	nS
Data Hold from Address Change	t_{OH}	5		5		5		5		nS
Chip Select Access	t_{ACS}		70		85		100		120	nS
Output Enable to Output Valid	t_{OE}		35		40		45		50	nS
Chip Select to Output in Low Z	t_{CLZ}[1]	5		5		5		5		nS
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		0		nS
Chip Deselect to Output in High Z	t_{CHZ}[1]		30		35		40		50	nS
Output Disable to Output in High Z	t_{OHZ}[1]		30		35		40		50	nS

1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORMS

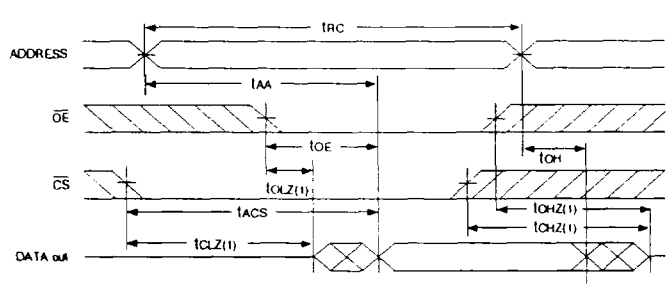


FIGURE 4 — Read Cycle Timing

1. Measured ± 200mV steady state; guaranteed by design but not tested.

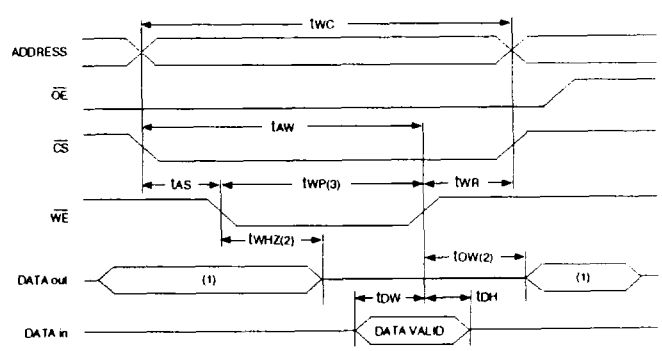


FIGURE 5 — Write Cycle Timing $\overline{WE}$ Controlled

1. I/O pins are in their output state, input signals must not be applied.
2. This parameter is guaranteed by design but not tested.
3. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter Write Cycle	Symbol	-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	25		35		45		55		nS
Chip Select to End of Write	t_{CW}	20		30		40		45		nS
Address Valid to End of Write	t_{AW}	20		30		40		45		nS
Data to Write-Time Overlap	t_{DW}	15		18		20		25		nS
Write Pulse Width	t_{WP}	20		25		35		40		nS
Address Setup Time	t_{AS}	0		0		0		0		nS
Write Recovery Time	t_{WR}	0		0		0		0		nS
Output Active from End of Write	t_{OW}[1]	5		5		5		5		nS
Write to Output in High Z	t_{WHZ}[1]		10		15		15		20	nS
Data Hold from Write Time	t_{DH}	3		3		3		5		nS

1. This parameter is guaranteed by design but not tested.

Parameter Write Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		85		100		120		nS
Chip Select to End of Write	t_{CW}	65		80		90		110		nS
Address Valid to End of Write	t_{AW}	65		80		90		110		nS
Data to Write-Time Overlap	t_{DW}	30		35		40		55		nS
Write Pulse Width	t_{WP}	45		50		55		65		nS
Address Setup Time	t_{AS}	5		5		5		5		nS
Write Recovery Time	t_{WR}	0		0		0		0		nS
Output Active from End of Write	t_{OW}[1]	5		5		5		5		nS
Write to Output in High Z	t_{WHZ}[1]		30		35		40		50	nS
Data Hold from Write Time	t_{DH}	5		5		5		5		nS

1. This parameter is guaranteed by design but not tested.

DATA RETENTION CHARACTERISTICS

(T_A = -55°C TO 125°C)

Parameter	Symbol	Conditions	-25			-35			-45			-55			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Data Retention Supply Voltage	V_{DR}	$\overline{CS} \geq V_{CC}$ -.2V	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		.3	6.0		.3	6.0		.5	6.0		.03	3.2	mA
	I_{CCDR2}	V_{CC} = 2V		.15	4		.15	4		.25	2.5		.02	2.0	mA

Parameter	Symbol	Conditions	-70			-85			-100			-120			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Data Retention Supply Voltage	V_{DR}	$\overline{CS} \geq V_{CC}$ -.2V	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		30	1500		30	1500		10	1100		10	1500	µA
	I_{CCDR2}	V_{CC} = 2V		20	1000		20	1000		7	750		7	1000	µA

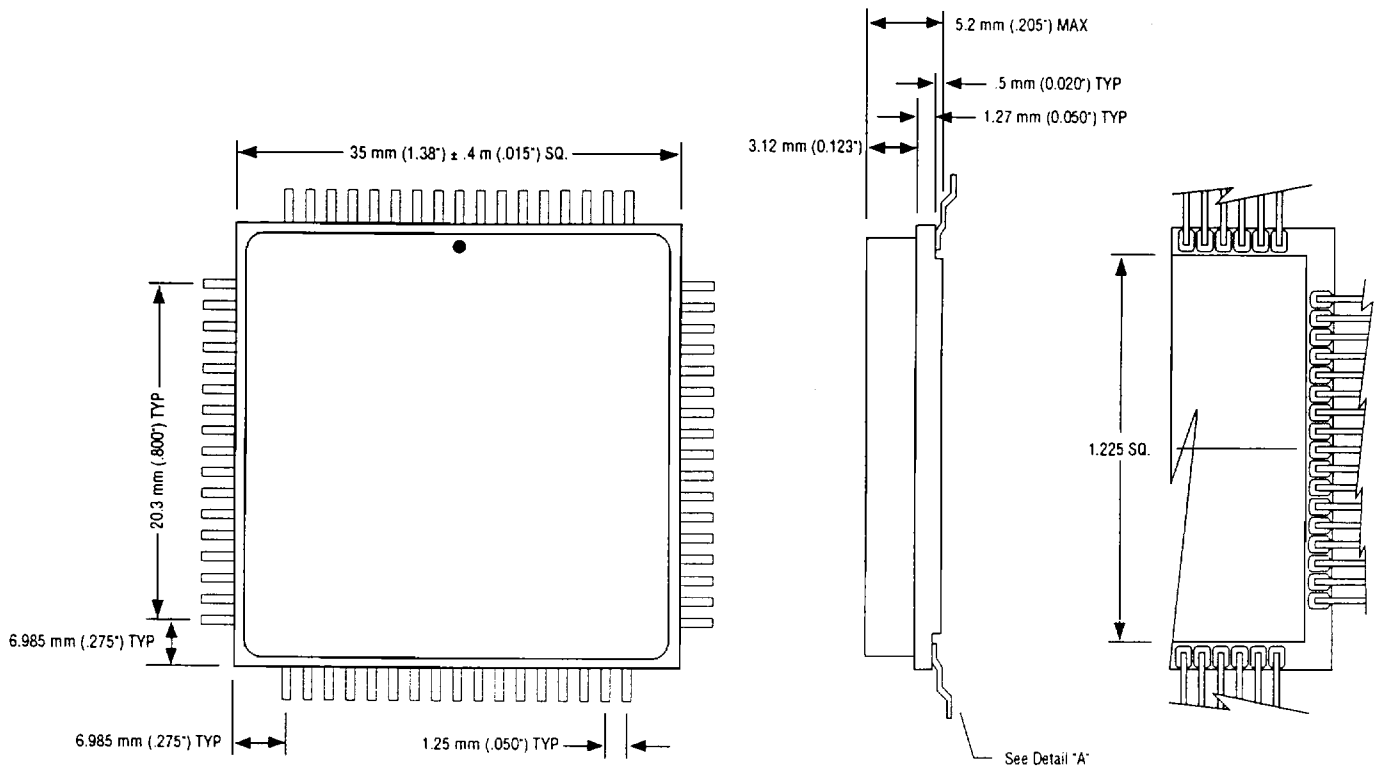
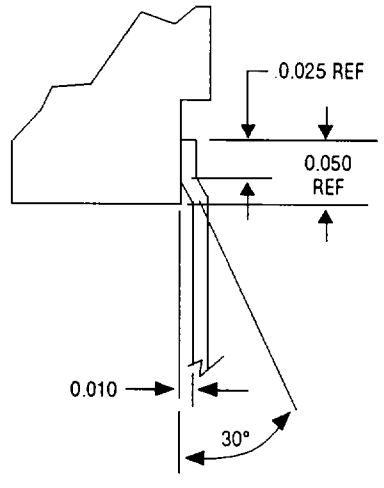


FIGURE 6 — Package Dimensions



ORDERING INFORMATION

W S - 128K 32 - XXX G4 X X

- **SPECIAL PROCESSING:**
  - E = Rad Tolerant Die
- **DEVICE GRADE:**
  - C = Commercial, 0 to 70°C
  - I = Industrial, -40°C to 85°C
  - M = Military, -55°C to 125°C
- **PACKAGE TYPE:**
  - G4 = Ceramic 35 mm Quad Flat Pack - Gull Wing
- **ACCESS TIME IN nS**
- **ORGANIZATION, 128Kx32**
  - User configurable as 256Kx16 or 512Kx8
- **SRAM**
- **WHITE TECHNOLOGY**

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