

OKI Semiconductor

MSM5116165A

1,048,576-Word × 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO

DESCRIPTION

The MSM5116165A is a 1,048,576-word × 16-bit dynamic RAM fabricated in OKI's CMOS silicon gate technology. The MSM5116165A achieves high integration, high-speed operation, and low-power consumption due to quadruple polysilicon double metal CMOS. The MSM5116165A is available in a 42-pin plastic SOJ or 50/44-pin plastic TSOP.

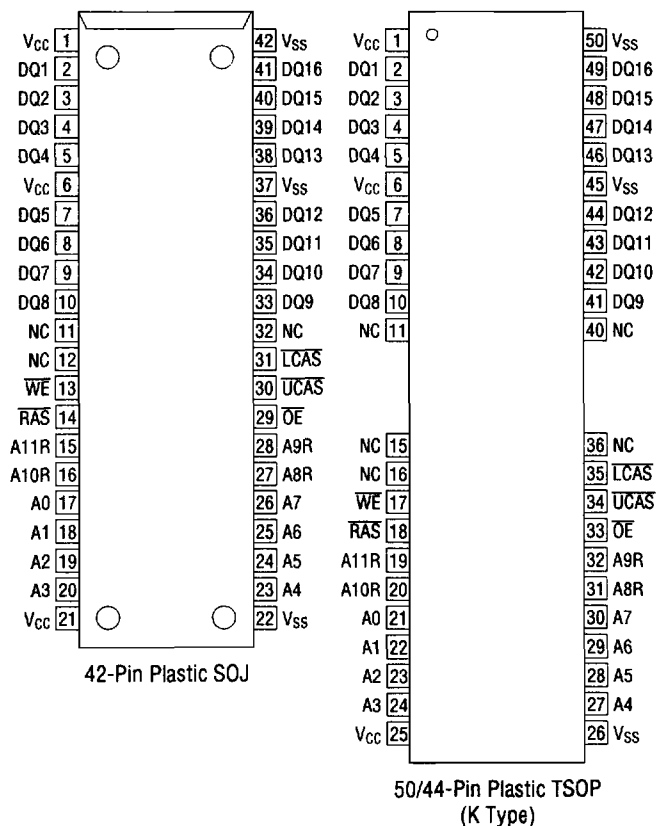
FEATURES

- 1,048,576-word × 16-bit configuration
- Single 5 V power supply, ±10% tolerance
- Input : TTL compatible, low input capacitance
- Output : TTL compatible, 3-state
- Refresh : 4096 cycles/64 ms
- Fast page mode with EDO, read modify write capability
- CAS before RAS refresh, hidden refresh, RAS-only refresh capability
- Package options:
 - 42-Pin 400 mil plastic SOJ (SOJ42-P-400) (Product : MSM5116165A-xxJS)
 - 50/44-Pin 400 mil plastic TSOP (TSOP50/44-P-400/0.8-K) (Product : MSM5116165A-xxTS-K)
 xx indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t _{RAC}	t _{AA}	t _{CAC}	t _{OEA}		Operating (Max.)	Standby (Max.)
MSM5116165A-60	60 ns	30 ns	15 ns	15 ns	110 ns	605 mW	5.5 mW
MSM5116165A-70	70 ns	35 ns	20 ns	20 ns	130 ns	550 mW	
MSM5116165A-80	80 ns	40 ns	20 ns	20 ns	150 ns	495 mW	

PIN CONFIGURATION (TOP VIEW)



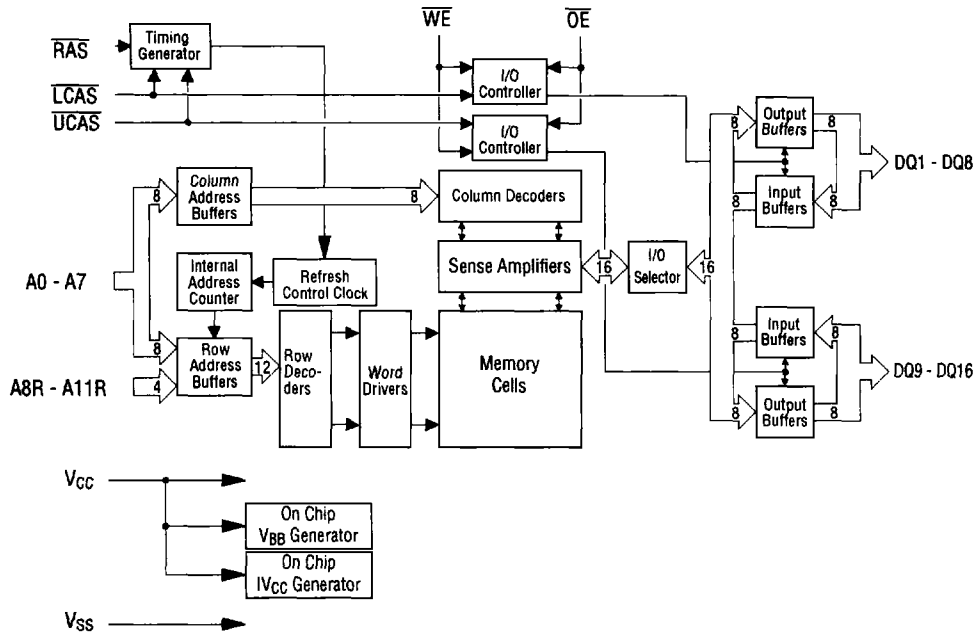
42-Pin Plastic SOJ

50/44-Pin Plastic TSOP
(K Type)

Pin Name	Function
A0 - A7, A8R - A11R	Address Input
RAS	Row Address Strobe
LCAS	Lower Byte Column Address Strobe
UCAS	Upper Byte Column Address Strobe
DQ1 - DQ16	Data Input/Data Output
OE	Output Enable
WE	Write Enable
V _{CC}	Power Supply (5 V)
V _{SS}	Ground (0 V)
NC	No Connection

Note : The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM



FUNCTION TABLE

Input Pin					DQ Pin		Function Mode
RAS	LCAS	UCAS	WE	OE	DQ1 - DQ8	DQ9 - DQ16	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	H	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	DOUT	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	DOUT	Upper Byte Read
L	L	L	H	L	DOUT	DOUT	Word Read
L	L	H	L	H	DIN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DIN	Upper Byte Write
L	L	L	L	H	DIN	DIN	Word Write
L	L	L	H	H	High-Z	High-Z	—

*: "H" or "L"

ELECTRICAL CHARACTERISTICS**Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V _{SS}	V _T	-1.0 to 7.0	V
Short Circuit Output Current	I _{OS}	50	mA
Power Dissipation	P _D *	1	W
Operating Temperature	T _{opr}	0 to 70	°C
Storage Temperature	T _{stg}	-55 to 150	°C

*: Ta = 25°C

Recommended Operating Conditions

(Ta = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V _{CC}	4.5	5.0	5.5	V
	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	6.5	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

Capacitance(V_{CC} = 5 V ±10%, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A7, A8R - A11R)	C _{IN1}	—	5	pF
Input Capacitance (<u>RAS</u> , <u>LCAS</u> , <u>UCAS</u> , <u>WE</u> , <u>OE</u>)	C _{IN2}	—	7	pF
Output Capacitance (DQ1 - DQ16)	C _{VO}	—	7	pF

DC Characteristics

(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C)

Parameter	Symbol	Condition	MSM5116165 A-60		MSM5116165 A-70		MSM5116165 A-80		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
			Output High Voltage	V _{OH}	I _{OH} = -5.0 mA	2.4	V _{CC}	2.4		
Output Low Voltage	V _{OL}	I _{OL} = 4.2 mA	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I _{LI}	0 V ≤ V _I ≤ 6.5 V; All other pins not under test = 0 V	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I _{LO}	DQ disable 0 V ≤ V _O ≤ 5.5 V	-10	10	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I _{CC1}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling, t _{RC} = Min.	—	110	—	100	—	90	mA	1, 2
Power Supply Current (Standby)	I _{CC2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ = V _{IH}	—	2	—	2	—	2	mA	1
		$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ ≥ V _{CC} - 0.2 V	—	1	—	1	—	1		
Average Power Supply Current ($\overline{\text{RAS}}$ -only Refresh)	I _{CC3}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ = V _{IH} , t _{RC} = Min.	—	110	—	100	—	90	mA	1, 2
Power Supply Current (Standby)	I _{CC5}	$\overline{\text{RAS}}$ = V _{IH} , $\overline{\text{CAS}}$ = V _{IL} , DQ = enable	—	5	—	5	—	5	mA	1
Average Power Supply Current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	I _{CC6}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	—	110	—	100	—	90	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I _{CC7}	$\overline{\text{RAS}}$ = V _{IL} , $\overline{\text{CAS}}$ cycling, t _{PC} = Min.	—	100	—	90	—	80	mA	1, 3

- Notes :
1. I_{CC} Max. is specified as I_{CC} for output open condition.
 2. Address can be changed once or less while $\overline{\text{RAS}}$ = V_{IL}.
 3. Address can be changed once or less while $\overline{\text{CAS}}$ = V_{IH}.

AC Characteristics (1/2)

(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM5116165 A-60		MSM5116165 A-70		MSM5116165 A-80		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t _{RC}	110	—	130	—	150	—	ns	
Read Modify Write Cycle Time	t _{RWC}	150	—	180	—	200	—	ns	
Fast Page Mode Cycle Time	t _{HPC}	25	—	30	—	35	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t _{PRWC}	80	—	95	—	100	—	ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}	—	60	—	70	—	80	ns	4, 5, 6
Access Time from $\overline{\text{CAS}}$	t _{CAC}	—	15	—	20	—	20	ns	4, 5
Access Time from Column Address	t _{AA}	—	30	—	35	—	40	ns	4, 6
Access Time from $\overline{\text{CAS}}$ Precharge	t _{CPA}	—	35	—	40	—	45	ns	4, 13
Access Time from $\overline{\text{OE}}$	t _{OEA}	—	15	—	20	—	20	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t _{CLZ}	0	—	0	—	0	—	ns	4
Data Output Hold After $\overline{\text{CAS}}$ Low	t _{DOH}	3	15	3	15	3	15	ns	
$\overline{\text{CAS}}$ to Data Output Buffer Turn-off Delay Time	t _{CEZ}	3	15	3	15	3	15	ns	7, 8
$\overline{\text{RAS}}$ to Data Output Buffer Turn-off Delay Time	t _{REZ}	3	15	3	15	3	15	ns	7, 8
$\overline{\text{OE}}$ to Data Output Buffer Turn-off Delay Time	t _{OEZ}	3	15	3	15	3	15	ns	7
$\overline{\text{WE}}$ to Data Output Buffer Turn-off Delay Time	t _{WEZ}	3	15	3	15	3	15	ns	7
Transition Time	t _T	3	50	3	50	3	50	ns	3
Refresh Period	t _{REF}	—	64	—	64	—	64	ms	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40	—	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode with EDO)	t _{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	15	—	20	—	20	—	ns	
$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	t _{ROH}	15	—	20	—	20	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode with EDO)	t _{CP}	10	—	10	—	10	—	ns	15
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	10	10,000	10	10,000	15	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	40	—	45	—	50	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5	—	5	—	5	—	ns	13
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{RHCP}	35	—	40	—	45	—	ns	13
$\overline{\text{OE}}$ Hold Time from $\overline{\text{CAS}}$ (DQ Disable)	t _{CHO}	5	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	45	20	50	20	60	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	15	40	ns	6
$\overline{\text{RAS}}$ to Second $\overline{\text{CAS}}$ Delay Time	t _{RSCD}	60	—	70	—	80	—	ns	
Row Address Set-up Time	t _{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	10	—	10	—	10	—	ns	
Column Address Set-up Time	t _{ASC}	0	—	0	—	0	—	ns	12
Column Address Hold Time	t _{CAH}	15	—	15	—	15	—	ns	12
Column Address Hold Time from $\overline{\text{RAS}}$	t _{AR}	40	—	45	—	50	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	30	—	35	—	40	—	ns	

AC Characteristics (2/2)

(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM5116165 A-60		MSM5116165 A-70		MSM5116165 A-80		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Command Set-up Time	t _{RCS}	0	—	0	—	0	—	ns	12
Read Command Hold Time	t _{RCH}	0	—	0	—	0	—	ns	9, 12
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t _{RRH}	0	—	0	—	0	—	ns	9
Write Command Set-up Time	t _{WCS}	0	—	0	—	0	—	ns	10, 12
Write Command Hold Time	t _{WCH}	10	—	15	—	15	—	ns	12
Write Command Hold Time from $\overline{\text{RAS}}$	t _{WCR}	40	—	45	—	50	—	ns	
Write Command Pulse Width	t _{WP}	10	—	15	—	15	—	ns	
$\overline{\text{WE}}$ Pulse Width (DQ Disable)	t _{WPE}	5	—	10	—	10	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t _{OEH}	15	—	20	—	20	—	ns	
$\overline{\text{OE}}$ Precharge Time	t _{OEP}	10	—	10	—	10	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t _{OCH}	10	—	10	—	10	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t _{RWL}	15	—	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t _{CWL}	15	—	20	—	20	—	ns	14
Data-in Set-up Time	t _{DS}	0	—	0	—	0	—	ns	11, 12
Data-in Hold Time	t _{DH}	15	—	15	—	15	—	ns	11, 12
Data-in Hold Time from $\overline{\text{RAS}}$	t _{DHR}	40	—	45	—	50	—	ns	
$\overline{\text{OE}}$ to Data-in Delay Time	t _{OED}	15	—	15	—	15	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	35	—	45	—	45	—	ns	10
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	50	—	60	—	65	—	ns	10
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	80	—	95	—	105	—	ns	10
$\overline{\text{CAS}}$ Precharge $\overline{\text{WE}}$ Delay Time	t _{CPWD}	55	—	65	—	70	—	ns	10
$\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge	t _{RPC}	5	—	5	—	5	—	ns	12
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CSR}	5	—	5	—	5	—	ns	12
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CHR}	10	—	15	—	15	—	ns	13
$\overline{\text{CAS}}$ Precharge Time (Refresh Counter Test)	t _{CPT}	20	—	30	—	40	—	ns	15

- Notes:
1. A start-up delay of 200 μ s is required after power-up, followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) before proper device operation is achieved.
 2. The AC characteristics assume $t_T = 5$ ns.
 3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL} .
 4. This parameter is measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, access time is controlled by t_{CAC} .
 6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, access time is controlled by t_{AA} .
 7. t_{CEZ} (Max.), t_{REZ} (Max.), t_{WEZ} (Max.) and t_{OEZ} (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
 8. t_{CEZ} and t_{REZ} must be satisfied for open circuit condition.
 9. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 10. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 11. These parameters are referenced to $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$, leading edge in an early write cycle, and to $\overline{\text{WE}}$ leading edge in an $\overline{\text{OE}}$ control write cycle or a read modify write cycle.
 12. These parameters are determined by the falling edge of $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$, whichever is earlier.
 13. These parameters are determined by the rising edge of $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$, whichever is later.
 14. t_{CWL} should be satisfied by both $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$.
 15. t_{CP} and t_{CPT} are determined by the time both $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ are high.

See ADDENDUM H for AC Timing Waveforms