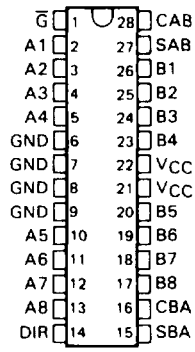
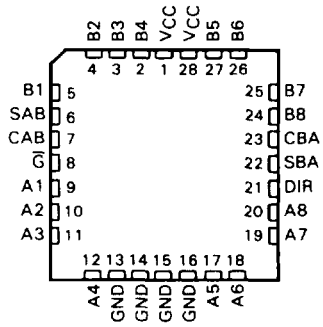
D2957, JULY 1987 – REVISED MARCH 1990

- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic DIPs

54ACT11646 . . . JT PACKAGE
74ACT11646 . . . DW OR NT PACKAGE
(TOP VIEW)



54ACT11646 . . . FK PACKAGE
(TOP VIEW)



description

These devices consist of bus transceiver circuits, 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch which occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus will receive data when enable $\overline{G}$ is active (low). In the isolation mode (control $\overline{G}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The 54ACT11646 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11646 is characterized for operation from −40°C to 85°C.

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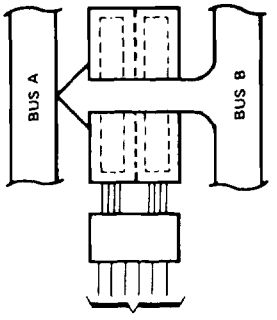
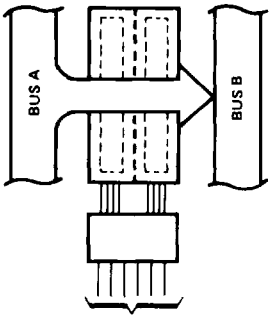


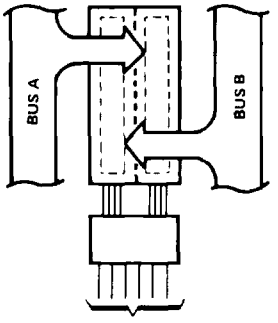
1 $\overline{G}$	14 DIR	28 CAB	16 CBA	27 SAB	15 SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



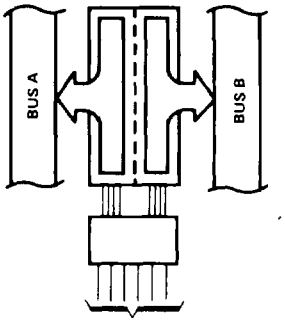
1 $\overline{G}$	14 DIR	28 CAB	16 CBA	27 SAB	15 SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



1 $\overline{G}$	14 DIR	28 CAB	16 CBA	27 SAB	15 SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



1 $\overline{G}$	14 DIR	28 CAB	16 CBA	27 SAB	15 SBA
L	L	X	HorL	X	H
L	H	HorL	X	H	X

TRANSFER STORED DATA
TO A OR B

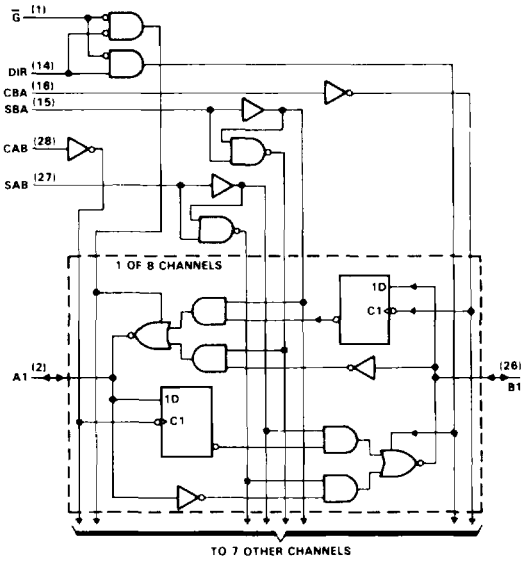
FIGURE 1. BUS-MANAGEMENT FUNCTIONS

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

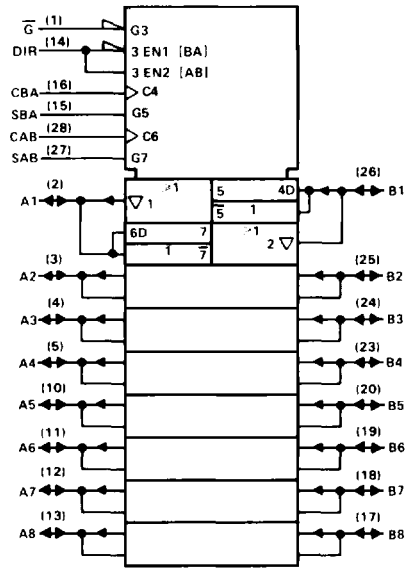
† The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

functional block diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ± 50 mA
Continuous current through V_{CC} or GND pins . . . . . ± 200 mA
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11646		74ACT11646		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	40	85	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11646		74ACT11646		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	A or B ports‡	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	$\overline{G}$ or DIR	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i		V_I = V_{CC} or GND	5 V		4.5						pF
C_o		V_O = V_{CC} or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements, V_{CC} = 5 ± 0.5 V (see Note 2)

		T_A = 25°C		54ACT11646		74ACT11646		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	105	0	105	0	105	MHz
t_w	Pulse duration, CAB or CBA high or low	4.8		4.8		4.8		ns
t_{su}	Setup time, A before CLK↑ or B before CBA↑	4.5		4.5		4.5		ns
t_h	Hold time, A after CAB↑ or B after CBA↑	2.5		2.5		2.5		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

switching characteristics, V_{CC} = 5 V ± 0.5 V (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11646		74ACT11646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			105			105		105		MHz
t_{PLH}	A or B	B or A	1.5	7.3	10.1	1.5	12.5	1.5	11.5	ns
t_{PHL}			1.5	7.2	11	1.5	12.9	1.5	12	
t_{PZH}	$\overline{G}$	A or B	1.5	7.7	12.8	1.5	15.5	1.5	14.4	ns
t_{PZL}			1.5	9.2	13.8	1.5	16.7	1.5	15.3	
t_{PHZ}	$\overline{G}$	A or B	1.5	8.6	10.7	1.5	12.3	1.5	11.6	ns
t_{PLZ}			1.5	7.8	9.7	1.5	11.2	1.5	10.6	
t_{PLH}	CBA or CAB	A or B	1.5	8.8	11.9	1.5	14.7	1.5	13.5	ns
t_{PHL}			1.5	10	13.4	1.5	15.9	1.5	14.9	
t_{PZH}	DIR	A or B	1.5	10.2	13.7	1.5	16.7	1.5	15.3	ns
t_{PZL}			1.5	10.9	14.8	1.5	18	1.5	16.5	
t_{PHZ}	DIR	A or B	1.5	7.9	10.5	1.5	11.8	1.5	11.3	ns
t_{PLZ}			1.5	7.3	9.5	1.5	10.7	1.5	10.3	
t_{PLH}	SBA or SAB (A or B high)	A or B	1.5	6.7	10.3	1.5	12.4	1.5	11.5	ns
t_{PHL}			1.5	9.1	12.1	1.5	14.5	1.5	13.5	
t_{PLH}	SBA or SAB (A or B low)	A or B	1.5	8	10.9	1.5	13.6	1.5	12.4	ns
t_{PHL}			1.5	8.1	11.9	1.5	14	1.5	13.1	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	63	pF
		Outputs disabled		14	

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