

# FAST 74F379 Register

Quad Parallel Register With Enable

## FAST Products

### FEATURES

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- Buffered common Enable input
- True and complementary outputs

### DESCRIPTION

The 74F379 is a 4-bit register with buffered common Enable ( $\bar{E}$ ). This device is similar to the 'F175 but features the common Enable rather common Master Reset.

### Product Specification

TYPE	TYPICAL $f_{MAX}$	TYPICAL SUPPLY CURRENT (TOTAL)
74F379	120MHz	28mA

### ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$
16-Pin Plastic DIP	N74F379N
16-Pin Plastic SO	N74F379D

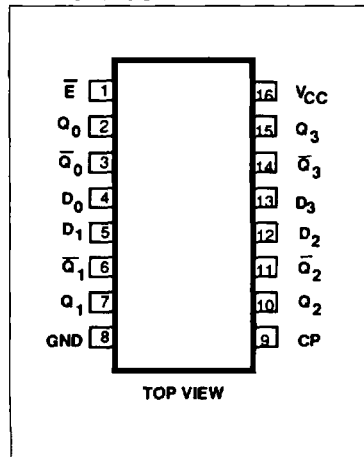
### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_3$	Data inputs	1.0/1.0	20 $\mu$ A/0.6mA
$\bar{E}$	Enable input (active Low)	1.0/1.0	20 $\mu$ A/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20 $\mu$ A/0.6mA
$Q_0 - Q_3$	True outputs	50/33	1.0mA/20mA
$\bar{Q}_0 - \bar{Q}_3$	Complementary outputs	50/33	1.0mA/20mA

#### NOTE:

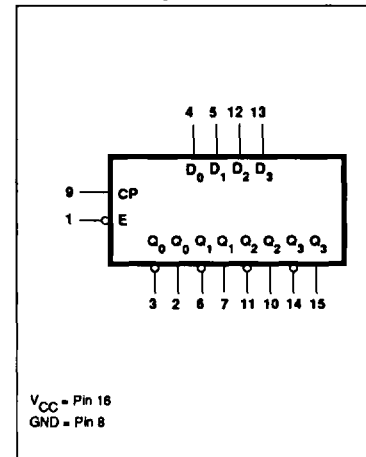
One (1.0) FAST Unit Load is defined as: 20 $\mu$ A in the High state and 0.6mA in the Low state.

### PIN CONFIGURATION



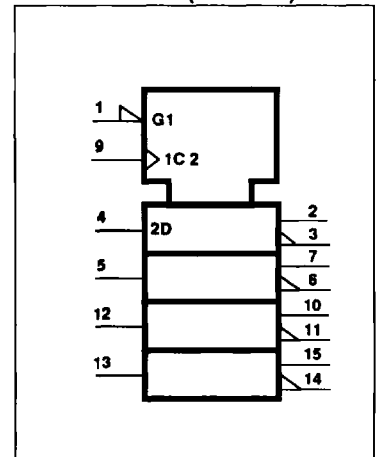
March 28, 1989

### LOGIC SYMBOL



6-400

### LOGIC SYMBOL (IEEE/IEC)

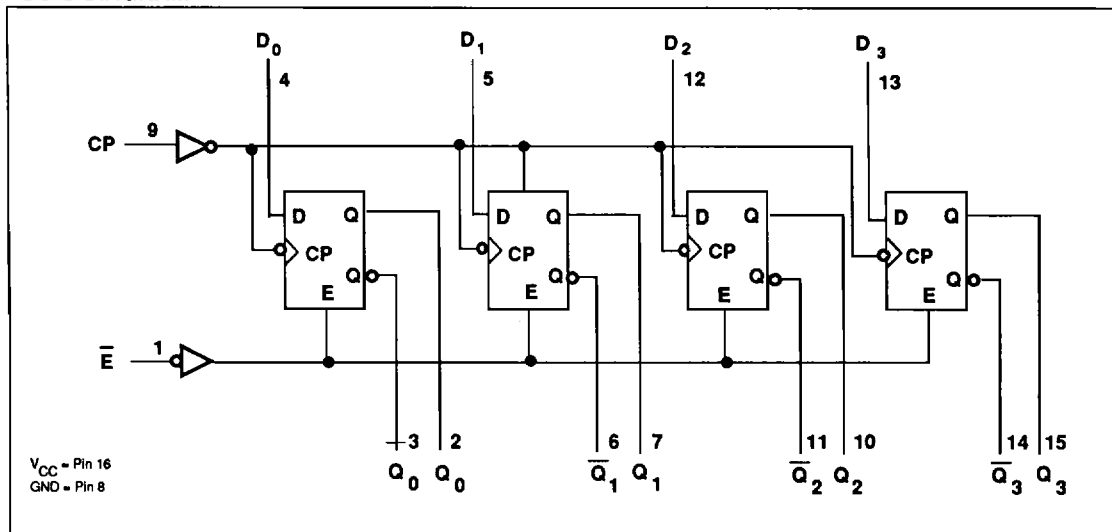


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# Quad Register

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## LOGIC DIAGRAM



## FUNCTION TABLE

INPUTS			OUTPUTS	
$\bar{E}$	CP	$D_n$	$Q_n$	$\bar{Q}_n$
H	↑	X	NC	NC
L	↑	h	H	L
L	↑	l	L	H

- H = High voltage level
- h = High voltage level one set-up time prior to the Low-to-High clock transition
- L = Low voltage level
- l = Low voltage level one set-up time prior to the Low-to-High clock transition
- X = Don't care
- ↑ = Low-to-High clock transition
- NC = No change

## ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	-0.5 to +7.0	V
$V_{IN}$	Input voltage	-0.5 to +7.0	V
$I_{IN}$	Input current	-30 to +5	mA
$V_{OUT}$	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
$I_{OUT}$	Current applied to output in Low output state	40	mA
$T_A$	Operating free-air temperature range	0 to +70	°C
$T_{STG}$	Storage temperature	-65 to +150	°C

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current			-1	mA
$I_{OL}$	Low-level output current			20	mA
$T_A$	Operating free-air temperature range	0		70	°C

## DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT		
			Min	Typ <sup>2</sup>	Max			
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$	$\pm 10\%V_{CC}$	2.5		V		
		$V_{IH} = \text{MIN}, I_{OH} = \text{MAX}$	$\pm 5\%V_{CC}$	2.7	3.4	V		
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$	$\pm 10\%V_{CC}$		0.30	0.50	V	
		$V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$	$\pm 5\%V_{CC}$		0.30	0.50	V	
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-0.73	-1.2	V	
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0\text{V}$				100	$\mu\text{A}$	
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$				20	$\mu\text{A}$	
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$				-0.6	mA	
$I_{OS}$	Short circuit output current <sup>3</sup>	$V_{CC} = \text{MAX}$			-60		mA	
$I_{CC}$	Supply current (total)	$V_{CC} = \text{MAX}, D_n = \bar{E} = 4.5\text{V}, CP = \uparrow$				28	40	mA

## NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ .
- Not more than one output should be shorted at a time. For testing  $I_{OS}$ , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.

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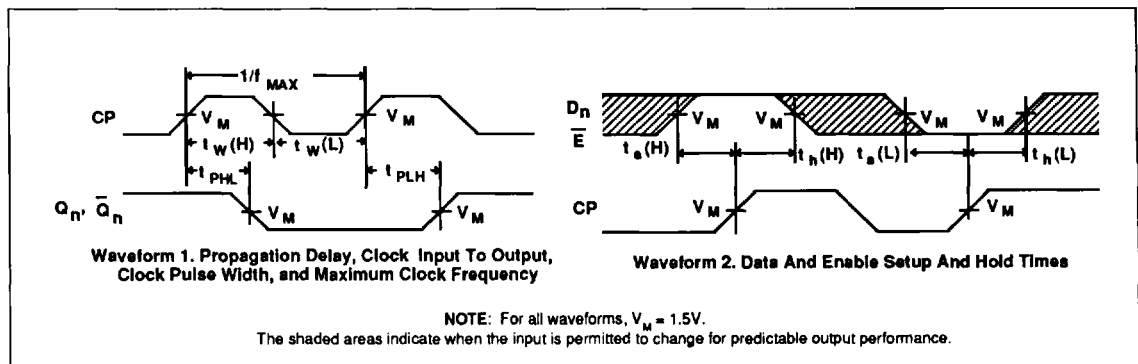
## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T <sub>A</sub> = +25°C V <sub>CC</sub> = 5V C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω			T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = 5V ±10% C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω		
			Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum clock frequency	Waveform 1	100	120		90		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Q <sub>n</sub> or $\bar{Q}_n$	Waveform 1	3.5 4.5	5.0 6.5	7.0 8.5	3.5 4.5	8.0 9.5	ns

## AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T <sub>A</sub> = +25°C V <sub>CC</sub> = 5V C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω			T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = 5V ±10% C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω		
			Min	Typ	Max	Min	Max	
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup time, High or Low D <sub>n</sub> to CP	Waveform 2	3.0 3.0			3.0 3.0		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, High or Low D <sub>n</sub> to CP	Waveform 2	1.0 1.0			1.0 1.0		ns
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup time, High or Low E to CP	Waveform 2	6.0 6.0			6.0 6.0		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, High or Low E to CP	Waveform 2	0.0 0.0			0.0 0.0		ns
t <sub>w</sub> (H) t <sub>w</sub> (L)	CP Pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns

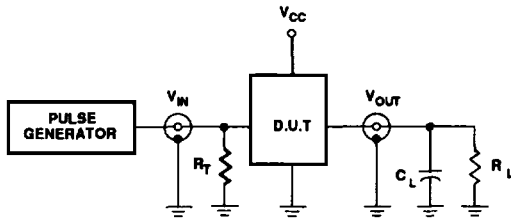
## AC WAVEFORMS



# Quad Register

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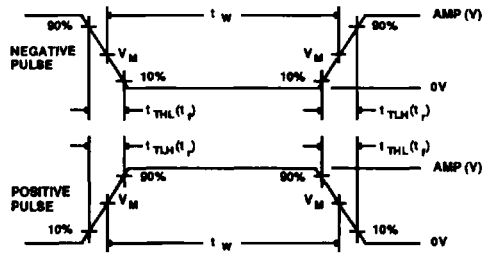
## TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs

**DEFINITIONS**

- $R_L$  = Load resistor; see AC CHARACTERISTICS for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	$t_W$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1MHz	500ns	2.5ns	2.5ns