



**CMOS DUAL-PORT RAM
8K (1K x 8-BIT)**

IDT7130SA/LA
IDT7140SA/LA

T-46-23-12

Integrated Device Technology, Inc.

FEATURES

- High-speed access
 - Military: 25/30/35/45/55/70/90/100/120ns (max.)
 - Commercial: 20/25/30/35/45/55/70/90/100ns (max.)
- Low-power operation
 - IDT7130/IDT7140SA
 - Active: 325mW (typ.)
 - Standby: 5mW (typ.)
 - IDT7130/IDT7140LA
 - Active: 325mW (typ.)
 - Standby: 1mW (typ.)
- MASTER IDT7130 easily expands data bus width to 16-or-more-bits using SLAVE IDT7140
- On-chip port arbitration logic (IDT7130 Only)
- **BUSY** output flag on IDT7130; **BUSY** input on IDT7140
- **INT** flag for port-to-port communication
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible, single 5V ±10% power supply
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-86875
- Industrial temperature range (-40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION

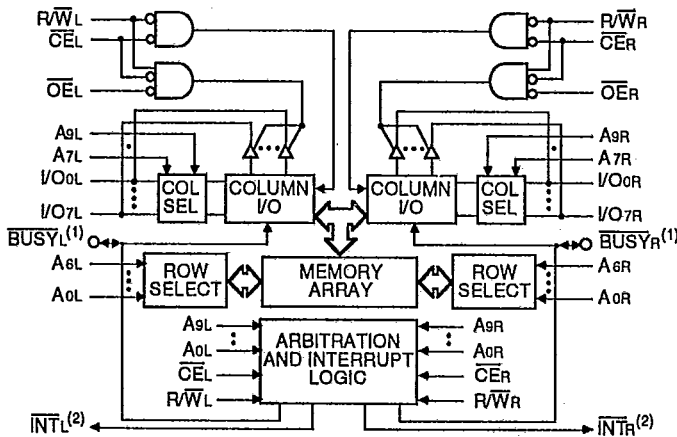
The IDT7130/IDT7140 are high speed 1K x 8 dual-port static RAMs. The IDT7130 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7140 "SLAVE" dual-port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address, and I/O pins that permit independent asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by **CE**, permits the on chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 325mW of power at maximum access times as fast as 20ns. Low-power (LA) versions offer battery backup data retention capability, with each dual-port typically consuming 200µW from a 2V battery.

The IDT7130/IDT7140 devices are packaged in 48-pin sidebraze or plastic DIPs, 48- or 52-pin LCCs, 52-pin PLCCs, and 48-Lead flatpacks. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



- NOTES:**
1. IDT7130 (MASTER): **BUSY** is open drain output and requires pullup resistor.
 - IDT7140 (SLAVE): **BUSY** is Input.
 2. Open drain output; requires pullup resistor.

2689 drw 01

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

APRIL 1992

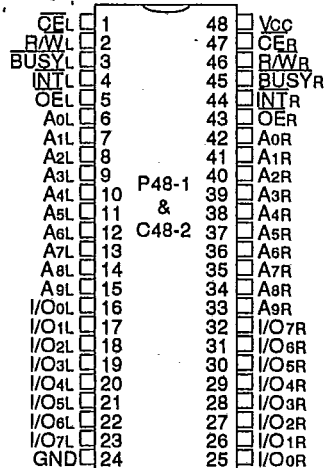


IDT7130SA/LA AND IDT7140SA/LA
CMOS DUAL-PORT RAM 8K (1K x 8-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

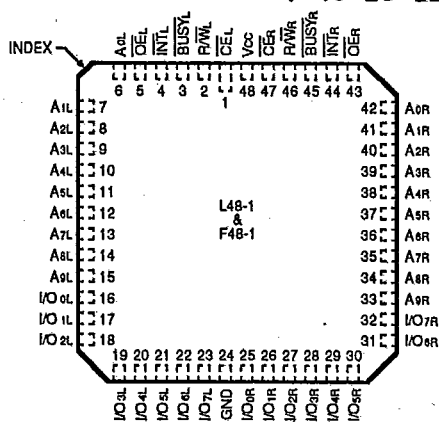
PIN CONFIGURATIONS

T-46-23-12



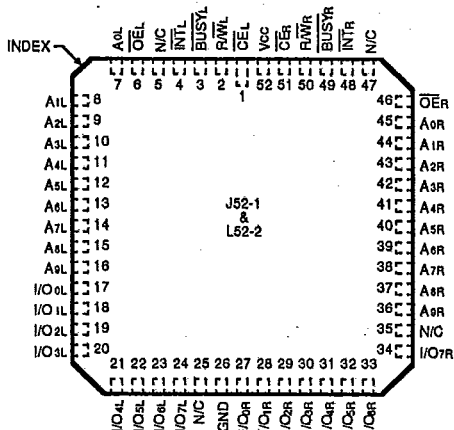
2689 drw 02

DIP
TOP VIEW



2689 drw 03

48-PIN LCC/FLATPACK
TOP VIEW



2689 drw 04

52-PIN LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating	Commercial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

2689 tbl 01

- NOTE:
- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
 - VTERM must not exceed Vcc + 0.5V.

RECOMMENDED
DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
Vih	Input High Voltage	2.2	—	6.0 ⁽²⁾	V
Vil	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

2689 tbl 02

- NOTE:
- Vil (min.) = -3.0V for pulse width less than 20ns.
 - VTERM must not exceed Vcc + 0.5V.

RECOMMENDED OPERATING
TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2689 tbl 03

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ±10%)

T-46-23-12

Symbol	Parameter	Test Conditions	IDT7130SA IDT7140SA		IDT7130LA IDT7140LA		Unit
			Mln.	Max.	Max.	Max.	
I _I	Input Leakage Current ⁽⁹⁾	V _{CC} = 5.5V, V _{IN} = 0V to V _{CC}	—	10	—	5	μA
I _O	Output Leakage Current	$\overline{CE} = V_{IH}$, V _{OUT} = 0V to V _{CC}	—	10	—	5	μA
V _{OL}	Output Low Voltage (V _{CC} -V _{O7})	I _{OL} = 4.0mA	—	0.4	—	0.4	V
V _{OL}	Open Drain Output Low Voltage (BUSY, INT)	I _{OL} = 16mA	—	0.5	—	0.5	V
V _{OH}	Output High Voltage	I _{OH} = -4mA	2.4	—	2.4	—	V

2689 tbt 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (1,8) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version	7130 x 20 ^(2,6) 7140 x 20 ^(2,6)		7130 x 25 ⁽⁶⁾ 7140 x 25 ⁽⁶⁾		7130 x 30 ⁽⁶⁾ 7140 x 30 ⁽⁶⁾		7130 x 35 ⁽⁷⁾ 7140 x 35 ⁽⁷⁾		7130 x 45 7140 x 45		Unit	
				Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.		Typ.
I _{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} = V_{IL}$ Outputs Open f = f _{MAX} ⁽⁴⁾	Mil.	SA	—	—	125	300	125	295	125	290	75	230	mA
				LA	—	—	125	240	125	235	125	230	75	185	
			Com'l.	SA	125	265	125	260	125	255	75	195	75	190	mA
				LA	125	215	125	210	125	205	75	155	75	145	
I _{SB1}	Standby Current (Both Ports - TTL Level Inputs)	\overline{CE}_L and $\overline{CE}_R \geq V_{IH}$ f = f _{MAX} ⁽⁴⁾	Mil.	SA	—	—	30	80	30	80	30	80	25	65	mA
				LA	—	—	30	60	30	60	30	60	25	55	
			Com'l.	SA	30	65	30	65	30	65	25	65	25	65	mA
				LA	30	45	30	45	30	45	25	45	25	45	
I _{SB2}	Standby Current (One Port - TTL Level Inputs)	\overline{CE}_L or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open, f = f _{MAX} ⁽⁴⁾	Mil.	SA	—	—	80	195	80	190	80	185	40	135	mA
				LA	—	—	80	160	80	155	80	150	40	110	
			Com'l.	SA	80	180	80	175	80	170	40	130	40	120	mA
				LA	80	145	80	140	80	135	40	95	40	85	
I _{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports \overline{CE}_L and $\overline{CE}_R \geq V_{CC} - 0.2V$ V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0 ⁽⁵⁾	Mil.	SA	—	—	1.0	30	1.0	30	1.0	30	1.0	30	mA
				LA	—	—	0.2	10	0.2	10	0.2	10	0.2	10	
			Com'l.	SA	1.0	15	1.0	15	1.0	15	1.0	15	1.0	15	mA
				LA	0.2	5	0.2	5	0.2	5	0.2	4	0.2	4	
I _{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	One Port \overline{CE}_L or $\overline{CE}_R \geq V_{CC} - 0.2V$ V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V Active Port Outputs Open, f = f _{MAX} ⁽⁴⁾	Mil.	SA	—	—	70	185	70	180	70	175	40	125	mA
				LA	—	—	70	150	70	145	70	140	35	95	
			Com'l.	SA	70	175	70	170	70	165	40	115	40	105	mA
				LA	70	140	70	135	70	130	35	90	35	80	



NOTES:

- "x" in part numbers indicates power rating (SA or LA).
- 0°C to +70°C temperature range only.
- 55°C to +125°C temperature range only.
- At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of Input levels of GND to 3V.
- f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
- Not available in DIP packages, see 7030/40 data sheet.
- DIP packages for 0°C to +70°C only, see 7030/40 data sheet.
- V_{CC} = 5V, T_A = +25°C for Typ.
- At V_{CC} ≤ 2.0V input leakages are undefined.

2689 tbt 05

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (1,6) (Continued) (V_{CC} = 5.0V ±10%)

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Symbol	Parameter	Test Conditions	Version	7130 x 55		7130 x 70		7130 x 80		7130 x 100		7130 x 120 ⁽³⁾		Unit	
				7140 x 55	Typ. Max.	7140 x 70	Typ. Max.	7140 x 80	Typ. Max.	7140 x 100	Typ. Max.	7140 x 120 ⁽³⁾	Typ. Max.		
I _{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} = V_{IL}$ Outputs Open $f = f_{MAX}^{(4)}$	Mil.	SA	65	230	65	225	65	200	65	190	65	190	mA
				LA	65	185	65	180	65	160	65	155	65	155	
I _{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE_L}$ and $\overline{CE_R} \geq V_{IH}$ $f = f_{MAX}^{(4)}$	Mil.	SA	25	65	25	65	25	65	25	65	25	65	mA
				LA	25	55	25	55	25	45	25	45	25	45	
I _{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE_L}$ or $\overline{CE_R} \geq V_{IH}$ Active Port Outputs Open, $f = f_{MAX}^{(4)}$	Mil.	SA	40	135	40	135	40	125	40	125	40	125	mA
				LA	40	110	40	110	40	100	40	100	40	100	
I _{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE_L}$ and $\overline{CE_R} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0^{(5)}$	Mil.	SA	1.0	30	1.0	30	1.0	30	1.0	30	1.0	30	mA
				LA	0.2	10	0.2	10	0.2	10	0.2	10	0.2	10	
I _{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	One Port $\overline{CE_L}$ or $\overline{CE_R} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ Active Port Outputs Open, $f = f_{MAX}^{(4)}$	Mil.	SA	40	120	40	115	40	110	40	110	40	110	mA
				LA	35	90	35	85	35	80	35	80	35	80	
			Com'l.	SA	65	180	65	180	65	180	65	180	—	—	
				LA	65	140	65	135	65	130	65	130	—	—	
				SA	25	65	25	60	25	55	25	55	—	—	
				LA	25	45	25	40	25	35	25	35	—	—	
				SA	40	135	40	135	40	125	40	125	40	125	
				LA	40	110	40	110	40	100	40	100	40	100	
				SA	40	115	40	110	40	110	40	110	—	—	
				LA	40	85	40	85	40	75	40	75	—	—	
				SA	1.0	30	1.0	30	1.0	30	1.0	30	1.0	30	
				LA	0.2	10	0.2	10	0.2	10	0.2	10	0.2	10	
				SA	1.0	15	1.0	15	1.0	15	1.0	15	—	—	
				LA	0.2	4	0.2	4	0.2	4	0.2	4	—	—	
				SA	40	100	40	100	40	95	40	95	—	—	
				LA	35	75	35	75	35	70	35	70	—	—	

NOTES:

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- *x* In part numbers indicates power rating (SA or LA).
- 0°C to +70°C temperature range only.
- 55°C to +125°C temperature range only.
- At $f = f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/trc, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
- f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
- V_{CC}=5V, T_A=+25°C for Typ.

DATA RETENTION CHARACTERISTICS (LA Version Only)

Symbol	Parameter	Test Conditions	IDT7130LA/IDT7140LA			Unit	
			Min.	Typ. ⁽¹⁾	Max.		
V _{DR}	V _{CC} for Data Retention		2.0	—	0	V	
I _{CCDR}	Data Retention Current	V _{CC} = 2.0V, $\overline{CE} \geq V_{CC} - 0.2V$	Mil.	—	100	4000	μA
			Com'l.	—	100	1500	μA
t _{CDR} ⁽³⁾	Chip Deselect to Data Retention Time	V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	0	—	—	ns	
t _R ⁽³⁾	Operation Recovery Time		t _{RC} ⁽²⁾	—	—	ns	

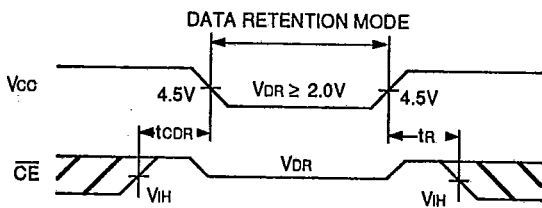
NOTES:

2689 tbl 07

- V_{CC} = 2V, T_A = +25°C
- t_{RC} = Read Cycle Time
- This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM

T-46-23-12



2689 drw 05

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2, and 3

2689 tbi 08

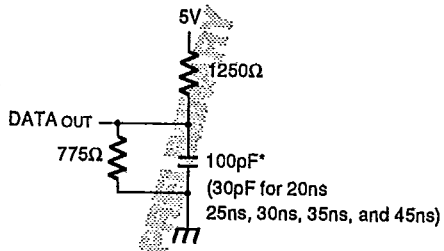


Figure 1. Output Load

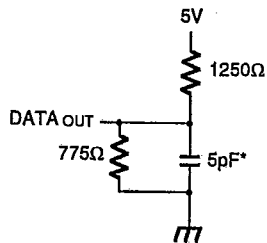


Figure 2. Output Load
(for tHZ, tLZ, tWZ, and tOW)

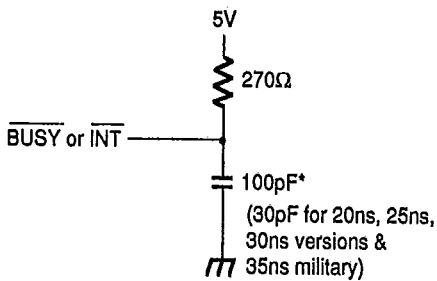


Figure 3. BUSY and INT
Output Load

* Including scope and jig

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AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE⁽⁵⁾

Symbol	Parameter	7130 x 20 ^(2,6) 7140 x 20 ^(2,6)		7130 x 25 ⁽⁶⁾ 7140 x 25 ⁽⁶⁾		7130 x 30 ⁽⁶⁾ 7140 x 30 ⁽⁶⁾		7130 x 35 ⁽⁷⁾ 7140 x 35 ⁽⁷⁾		7130 x 45 7140 x 45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t _{RC}	Read Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
t _{AA}	Address Access Time	—	20	—	25	—	30	—	35	—	45	ns
t _{ACE}	Chip Enable Access Time	—	20	—	25	—	30	—	35	—	45	ns
t _{AOE}	Output Enable Access Time	—	10	—	12	—	15	—	25	—	30	ns
t _{OH}	Output Hold From Address Change	0	—	0	—	0	—	0	—	0	—	ns
t _{lZ}	Output Low Z Time ^(1,4)	0	—	0	—	0	—	5	—	5	—	ns
t _{hZ}	Output High Z Time ^(1,4)	—	8	—	10	—	12	—	15	—	20	ns
t _{PU}	Chip Enable to Power Up Time ⁽⁴⁾	0	—	0	—	0	—	0	—	0	—	ns
t _{PD}	Chip Disable to Power Down Time ⁽⁴⁾	—	50	—	50	—	50	—	50	—	50	ns

2689 tbl 09

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE⁽⁵⁾ (Continued)

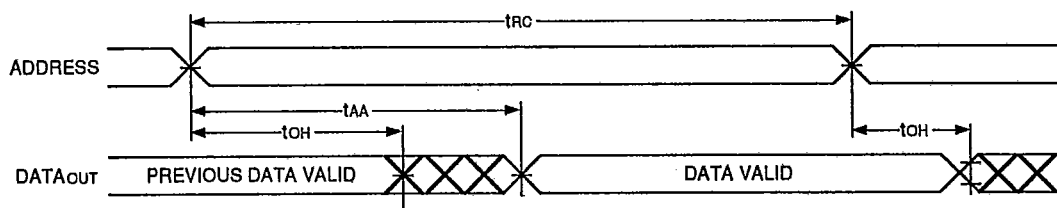
Symbol	Parameter	7130 x 55 7140 x 55		7130 x 70 7140 x 70		7130 x 90 7140 x 90		7130 x 100 7140 x 100		7130 x 120 ⁽³⁾ 7140 x 120 ⁽³⁾		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t _{RC}	Read Cycle Time	55	—	70	—	90	—	100	—	120	—	ns
t _{AA}	Address Access Time	—	55	—	70	—	90	—	100	—	120	ns
t _{ACE}	Chip Enable Access Time	—	55	—	70	—	90	—	100	—	120	ns
t _{AOE}	Output Enable Access Time	—	35	—	40	—	40	—	40	—	60	ns
t _{OH}	Output Hold From Address Change	0	—	0	—	10	—	10	—	10	—	ns
t _{lZ}	Output Low Z Time ^(1,4)	5	—	5	—	5	—	5	—	5	—	ns
t _{hZ}	Output High Z Time ^(1,4)	—	30	—	35	—	40	—	40	—	40	ns
t _{PU}	Chip Enable to Power Up Time ⁽⁴⁾	0	—	0	—	0	—	0	—	0	—	ns
t _{PD}	Chip Disable to Power Down Time ⁽⁴⁾	—	50	—	50	—	50	—	50	—	50	ns

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NOTES:

1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2, and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. "x" in part numbers indicates power rating (SA or LA).
6. Not available in DIP packages, see 7030/40 data sheet.
7. DIP packages for 0°C to +70°C only, see 7030/40 data sheet.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE (1, 2, 4)



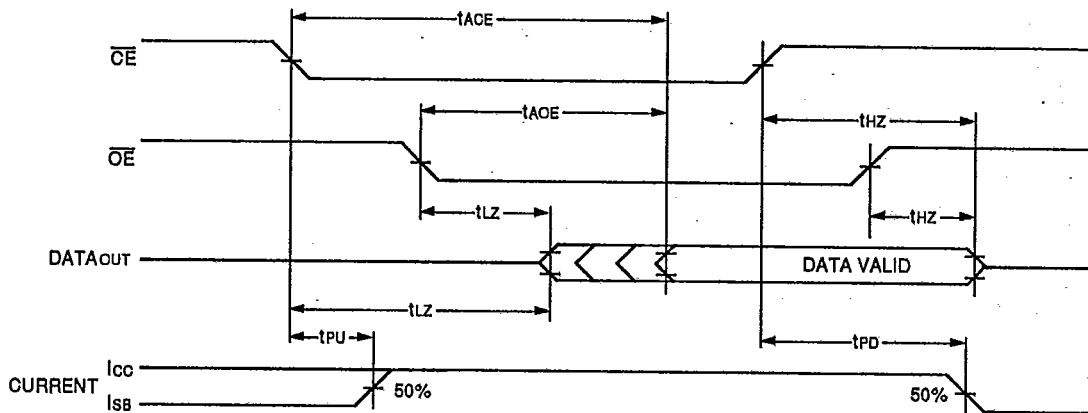
2689 drw 07

NOTES:

1. R/W is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE} = V_{IL}$.
3. Addresses valid prior to or coincident with \overline{CE} transition low.
4. $\overline{CE} = V_{IL}$.

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1, 3)

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2689 drw 08

NOTES:

1. R/W is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE} = V_{IL}$.
3. Addresses valid prior to or coincident with \overline{CE} transition low.
4. $\overline{OE} = V_{IL}$.



AC ELECTRICAL CHARACTERISTICS OVER THE
OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (7)

T-46-23-12

Symbol	Parameter	7130 x 20 ^(2,9)		7130 x 25 ⁽⁹⁾		7130 x 30 ⁽⁹⁾		7130 x 35 ⁽⁹⁾		7130 x 45		Unit
		7140 x 20 ^(2,9)	7140 x 25 ⁽⁹⁾	7140 x 30 ⁽⁹⁾	7140 x 35 ⁽⁹⁾	7140 x 45	7140 x 45	Min.	Max.	Min.	Max.	
Write Cycle												
tWC	Write Cycle Time ⁽⁵⁾	20	—	25	—	30	—	35	—	45	—	ns
tEW	Chip Enable to End of Write	15	—	20	—	25	—	30	—	35	—	ns
tAW	Address Valid to End of Write	15	—	20	—	25	—	30	—	35	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width ⁽⁶⁾	15	—	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	10	—	12	—	15	—	20	—	20	—	ns
tHZ	Output High Z Time ^(1,4)	—	8	—	10	—	12	—	15	—	20	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z ^(1,4)	—	8	—	10	—	12	—	15	—	20	ns
tOW	Output Active From End of Write ^(1,4)	0	—	0	—	0	—	0	—	0	—	ns

2689 tbl 11

AC ELECTRICAL CHARACTERISTICS OVER THE
OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (7)

Symbol	Parameter	7130 x 55		7130 x 70		7130 x 90		7130 x 100		7130 x 120 ⁽³⁾		Unit
		7140 x 55	7140 x 70	7140 x 90	7140 x 100	7140 x 120 ⁽³⁾	7140 x 120 ⁽³⁾	Min.	Max.	Min.	Max.	
Write Cycle												
tWC	Write Cycle Time ⁽⁵⁾	55	—	70	—	90	—	100	—	120	—	ns
tEW	Chip Enable to End of Write	40	—	50	—	85	—	90	—	100	—	ns
tAW	Address Valid to End of Write	40	—	50	—	85	—	90	—	100	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width ⁽⁶⁾	40	—	50	—	55	—	55	—	65	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	20	—	30	—	40	—	40	—	40	—	ns
tHZ	Output High Z Time ^(1,4)	—	30	—	35	—	40	—	40	—	40	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z ^(1,4)	—	30	—	35	—	40	—	40	—	50	ns
tOW	Output Active From End of Write ^(1,4)	0	—	0	—	0	—	0	—	0	—	ns

2689 tbl 12

NOTES:

1. Transition is measured ±500mV from low or high Impedance voltage with load (Figures 1, 2, and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, tWC = tBAA + tWP.
6. Specified for OE at high (Refer to "Timing Waveform of Write Cycle", Note 7)
7. "x" in part numbers indicates power rating (SA or LA).
8. Not available in DIP packages, see 7030/40 data sheet.
9. DIP packages for 0°C to +70°C only, see 7030/40 data sheet.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

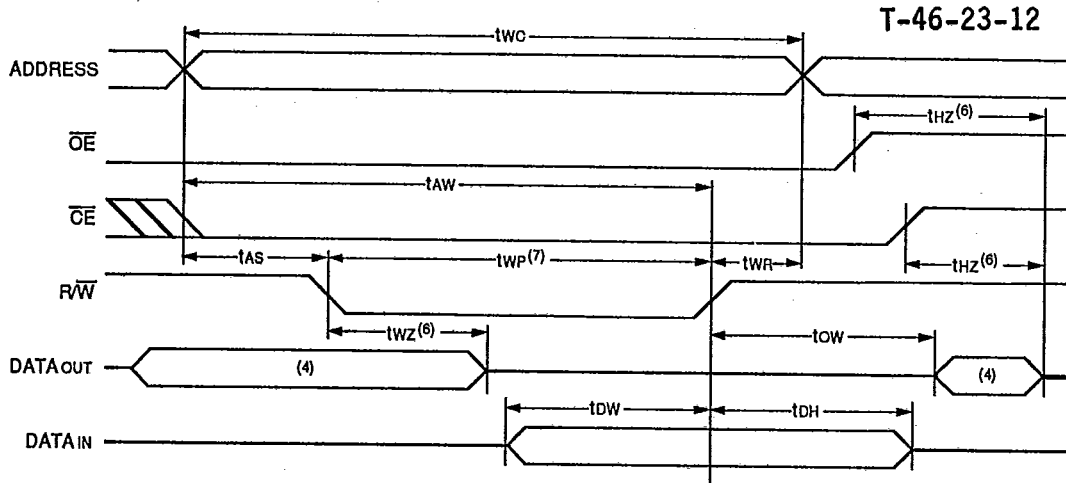
Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VIN = 0V	11	pF

2689 tbl 13

NOTE:

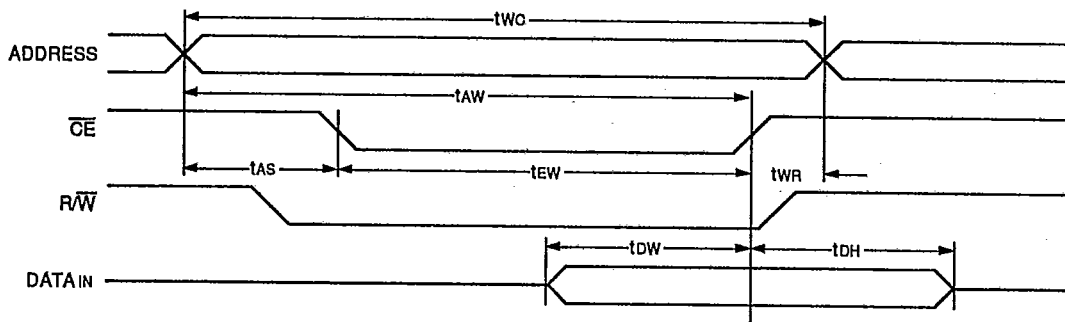
1. This parameter is determined by device characterization but is not production tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/W CONTROLLED TIMING) (1,2,3,7)



2689 drw 09

TIMING WAVEFORM OF WRITE CYCLE NO. 2, (CE CONTROLLED TIMING) (1,2,3,5)



2689 drw 10



- NOTES:**
1. R/W must be high during all address transitions.
 2. A write occurs during the overlap (tew or twp) of a low CE and a low R/W.
 3. tWR is measured from the earlier of CE or R/W going high to the end of the write cycle.
 4. During this period, the I/O pins are in the output state and input signals must not be applied.
 5. If the CE low transition occurs simultaneously with or after the R/W low transition, the outputs remain in the high impedance state.
 6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig).
 7. If CE is low during a R/W controlled write cycle, the write pulse width must be larger of twp or (twz + tow) to allow the I/O drivers to turn off and data to be placed on the bus for the required tow. If CE is high during an R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified twp.

AC ELECTRICAL CHARACTERISTICS OVER THE
OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (8)

T-46-23-12

Symbol	Parameter	7130 x 20 ^(1,10)		7130 x 25 ⁽¹⁰⁾		7130 x 30 ⁽¹⁰⁾		7130 x 35 ⁽¹¹⁾		7130 x 45		Unit
		7140 x 20 ^(1,10)	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	
BUSY TIMING (FOR MASTER IDT7130 ONLY)												
tBAA	BUSY Access Time to Address	—	20	—	25	—	30	—	35	—	35	ns
tBDA	BUSY Disable Time to Address	—	20	—	20	—	25	—	30	—	35	ns
tBAC	BUSY Access Time to Chip Enable	—	20	—	20	—	25	—	30	—	30	ns
tBDC	BUSY Disable Time to Chip Enable	—	20	—	20	—	25	—	25	—	25	ns
tWDD	Write Pulse to Data Delay ⁽³⁾	—	50	—	50	—	50	—	60	—	70	ns
tDDD	Write Data Valid to Read Data Delay ⁽³⁾	—	35	—	35	—	35	—	35	—	45	ns
tAPS	Arbitration Priority Set-up Time ⁽⁴⁾	5	—	5	—	5	—	5	—	5	—	ns
tBDD	BUSY Disable to Valid Data ⁽⁵⁾	—	Note 5	—	Note 5	—	Note 5	—	Note 5	—	Note 5	ns
BUSY INPUT TIMING (FOR SLAVE IDT7140 ONLY)												
tWB	Write to BUSY Input ⁽⁶⁾	0	—	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After BUSY ⁽⁷⁾	12	—	15	—	20	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay ⁽⁹⁾	—	50	—	50	—	50	—	60	—	70	ns
tDDD	Write Data Valid to Read Data Delay ⁽⁹⁾	—	35	—	35	—	35	—	35	—	45	ns

2689 tbl 14

AC ELECTRICAL CHARACTERISTICS OVER THE
OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (8)

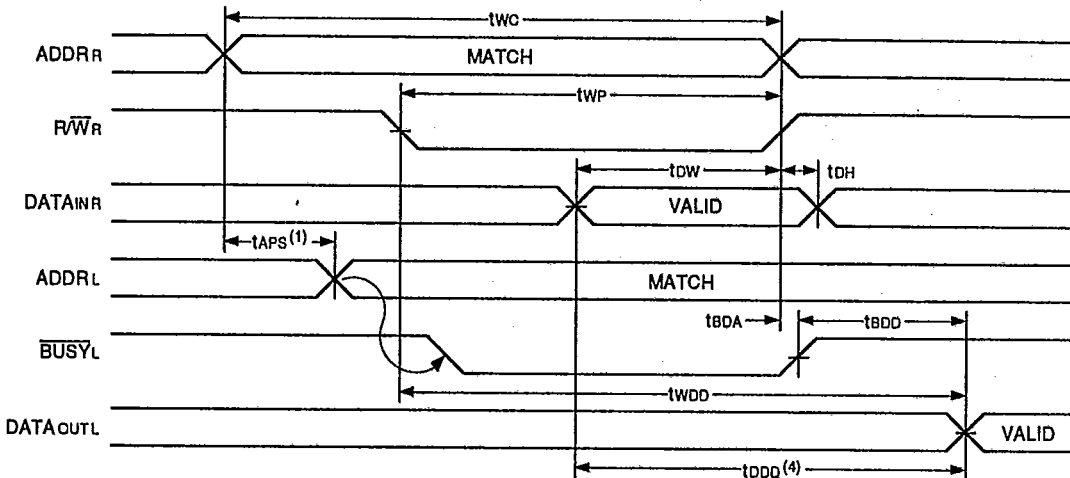
Symbol	Parameter	7130 x 55		7130 x 70		7130 x 90		7130 x 100		7130 x 120 ⁽²⁾		Unit
		7140 x 55	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	
BUSY TIMING (FOR MASTER IDT7130 ONLY)												
tBAA	BUSY Access Time to Address	—	45	—	45	—	45	—	50	—	60	ns
tBDA	BUSY Disable Time to Address	—	40	—	40	—	45	—	50	—	60	ns
tBAC	BUSY Access Time to Chip Enable	—	35	—	35	—	45	—	50	—	60	ns
tBDC	BUSY Disable Time to Chip Enable	—	30	—	30	—	45	—	50	—	60	ns
tWDD	Write Pulse to Data Delay ⁽³⁾	—	80	—	90	—	100	—	120	—	140	ns
tDDD	Write Data Valid to Read Data Delay ⁽³⁾	—	55	—	70	—	90	—	100	—	120	ns
tAPS	Arbitration Priority Set-up Time ⁽⁴⁾	5	—	5	—	5	—	5	—	5	—	ns
tBDD	BUSY Disable to Valid Data ⁽⁵⁾	—	Note 5	—	Note 5	—	Note 5	—	Note 5	—	Note 5	ns
BUSY INPUT TIMING (FOR SLAVE IDT7140 ONLY)												
tWB	Write to BUSY Input ⁽⁶⁾	0	—	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After BUSY ⁽⁷⁾	20	—	20	—	20	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay ⁽⁹⁾	—	80	—	90	—	100	—	120	—	140	ns
tDDD	Write Data Valid to Read Data Delay ⁽⁹⁾	—	55	—	70	—	90	—	100	—	120	ns

2689 tbl 15

NOTES:

- 0°C to +70°C temperature range only.
- 55°C to +125°C temperature range only.
- Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With BUSY (For Master IDT7130 only)".
- To ensure that the earlier of the two ports wins.
- tBDD is a calculated parameter and is the greater of 0, tWDD-tWP (actual) or tDDD-tW (actual).
- To ensure that the write cycle is inhibited during contention.
- To ensure that a write cycle is completed after contention.
- "x" in part numbers indicates power rating (SA or LA).
- Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With Port-to-Port Delay (For Slave IDT7140 Only)".
- Not available in DIP packages, see 7030/40 data sheet.
- DIP packages for 0°C to +70°C only, see 7030/40 data sheet.

TIMING WAVEFORM OF READ WITH $\overline{\text{BUSY}}$ (1,2,3) (FOR MASTER IDT7130 ONLY)

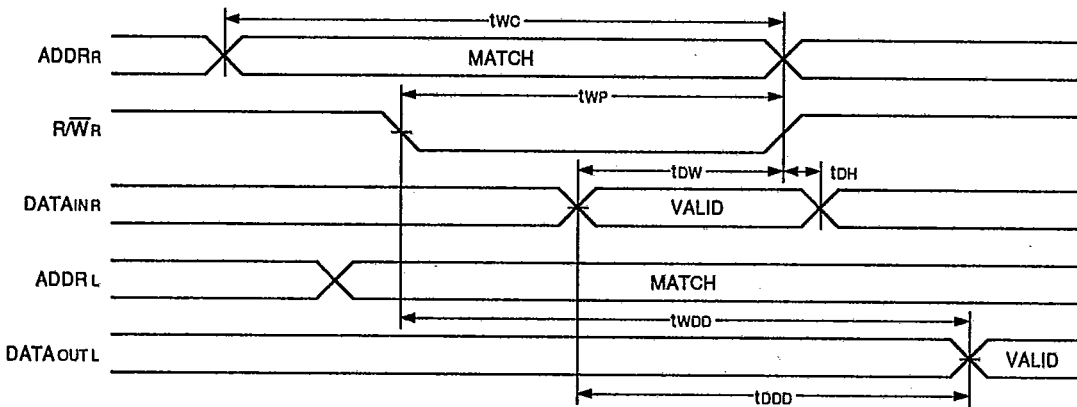


NOTES:

1. To ensure that the earlier of the two ports wins.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.
4. $\overline{\text{OE}}$ at LO for the reading port.

2689 drw 11

TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY (1,2,3) (FOR SLAVE IDT7140 ONLY)

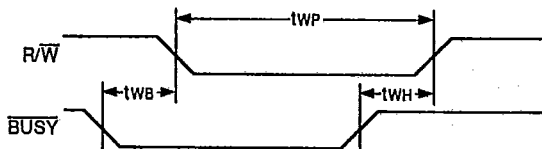


NOTES:

1. Assume $\overline{\text{BUSY}}$ Input at HI for the writing port, and $\overline{\text{OE}}$ at LO for the reading port.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.

2689 drw 12

TIMING WAVEFORM OF WRITE WITH $\overline{\text{BUSY}}$ INPUT (FOR SLAVE IDT7140 ONLY)



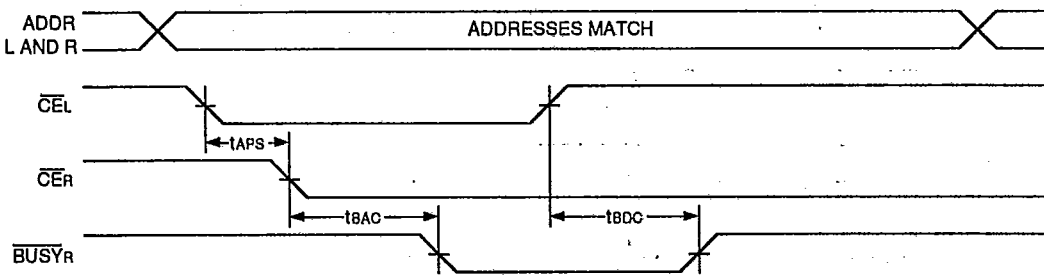
2689 drw 13



TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, \overline{CE} ARBITRATION (FOR MASTER IDT7130 ONLY)

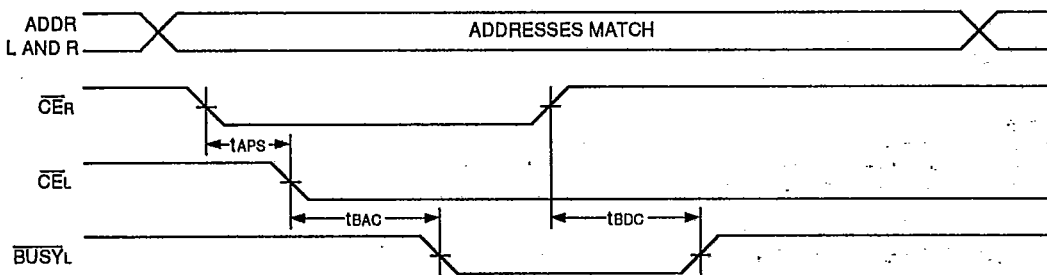
T-46-23-12

\overline{CE} L VALID FIRST:



\overline{CE} R VALID FIRST:

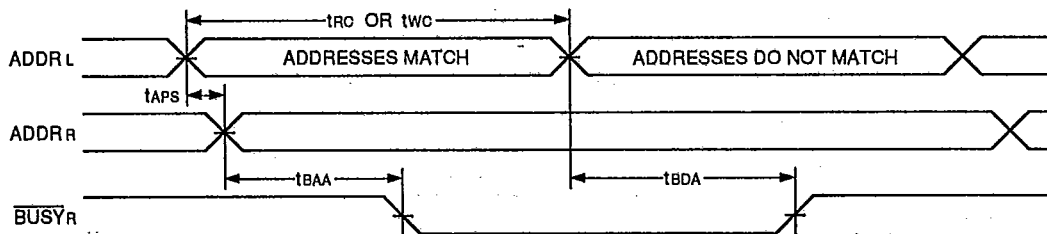
2689 drw 14



TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION⁽¹⁾ (FOR MASTER IDT7130 ONLY)

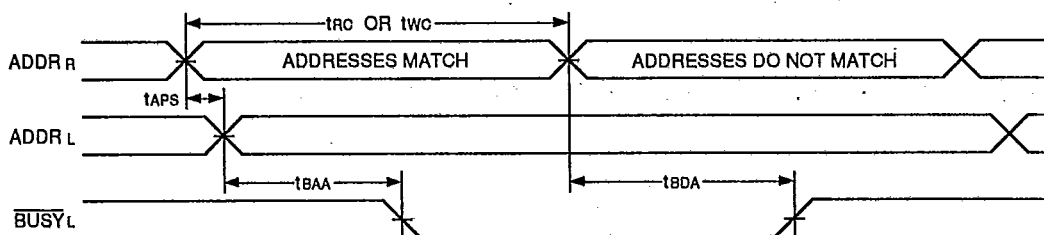
2689 drw 15

LEFT ADDRESS VALID FIRST:



2689 drw 16

RIGHT ADDRESS VALID FIRST:



2689 drw 17

NOTE:
1. \overline{CE} L = \overline{CE} R = V_L

T-46-23-12

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (3)

Symbol	Parameter	7130 x 20 ^(1,4)		7130 x 25 ⁽⁴⁾		7130 x 30 ⁽⁴⁾		7130 x 35 ⁽⁵⁾		7130 x 45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Interrupt Timing												
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	20	—	25	—	30	—	35	—	40	ns
tINR	Interrupt Reset Time	—	20	—	25	—	30	—	35	—	40	ns

2689 tbl 16

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

Symbol	Parameter	7130 x 55		7130 x 70		7130 x 90		7130 x 100		7130 x 120 ⁽²⁾		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Interrupt Timing												
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	45	—	50	—	55	—	60	—	70	ns
tINR	Interrupt Reset Time	—	45	—	50	—	55	—	60	—	70	ns

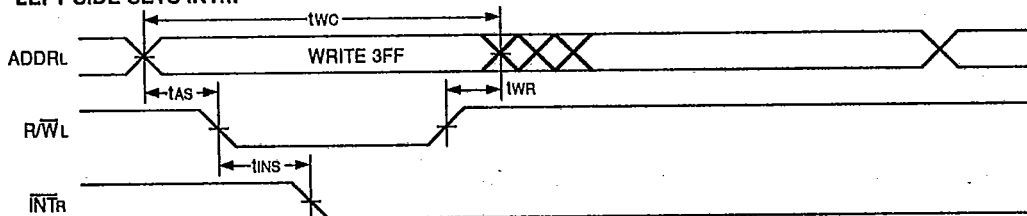
2689 tbl 17

NOTES:

- 0°C to +70°C temperature range only.
- 55°C to +125°C temperature range only.
- "x" in part numbers indicates power rating (SA or LA).
- Not available in DIP packages, see 7030/40 data sheet.
- DIP packages for 0°C to +70°C only, see 7030/40 data sheet.

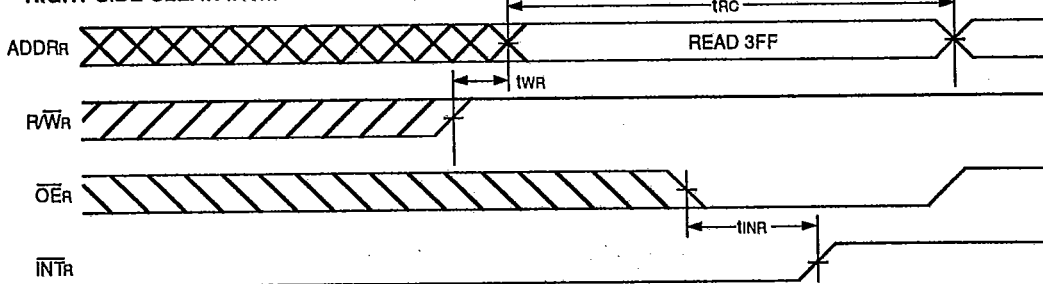
TIMING WAVEFORM OF INTERRUPT MODE (1, 2)

LEFT SIDE SETS INTR:



2689 drw 18

RIGHT SIDE CLEAR INTR:



2689 drw 19

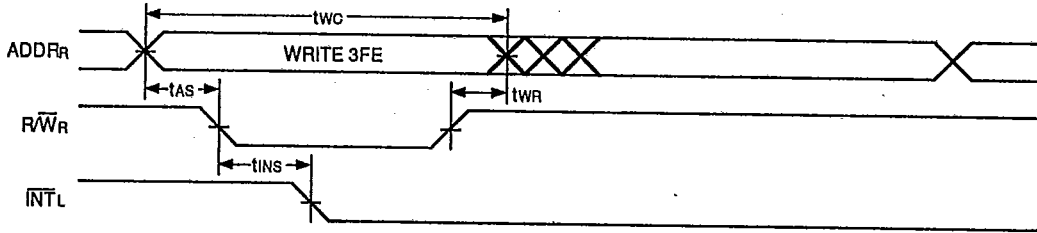
NOTES:

- $\overline{OEL} = \overline{OER} = V_{IL}$
- INTL and INTR are reset (high) during power up.

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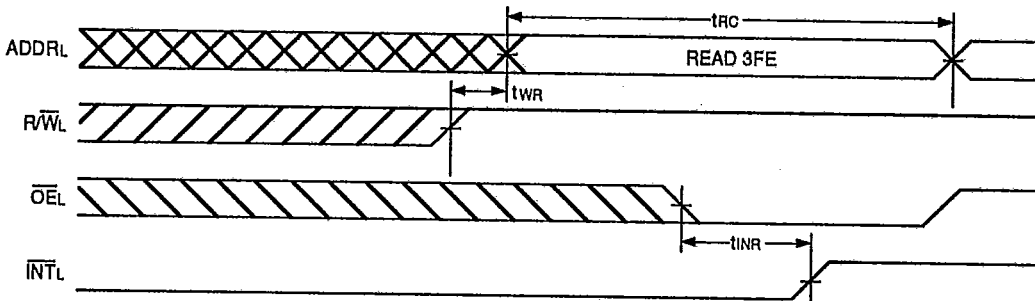
TIMING WAVEFORM OF INTERRUPT MODE(1, 2)

RIGHT SIDE SETS \overline{INTL} :



2689 drw 20

LEFT SIDE CLEAR \overline{INTL} :

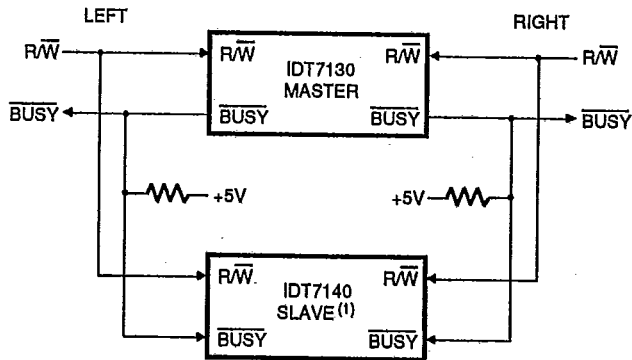


2689 drw 21

NOTES:

1. $\overline{CEL} = \overline{CER} = V_L$
2. \overline{INTR} and \overline{INTL} are reset (high) during power up.

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



2689 drw 22

NOTE:

1. No arbitration in IDT7140 (SLAVE). $\overline{BUSY-IN}$ inhibits write in IDT7140 (SLAVE).

FUNCTIONAL DESCRIPTION:

The IDT7130/IDT7140 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any locations in memory. The IDT7130/IDT7140 has an automatic power down feature controlled by \overline{CE} . The \overline{CE} controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected (\overline{CE} high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control (\overline{OE}). In the read mode, the port's \overline{OE} turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table 1.

The interrupt flag (\overline{INT}) permits communication between ports or systems. If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag (\overline{INTL}) is set when the right port writes to memory location 3FE (HEX). The left port clears the interrupt by reading address location 3FE. Likewise, the right port interrupt flag (\overline{INTR}) is set when the left port writes to memory location 3FF (HEX) and to clear the interrupt flag (\overline{INTR}), the right port must read the memory location 3FF. The message (8-bits) at 3FE or 3FF is user defined. If the interrupt function is not used, address locations 3FE or 3FF are not used as mailboxes, but as part of the random access memory. Refer to Table II for the interrupt operation.

ARBITRATION LOGIC**FUNCTIONAL DESCRIPTION:**

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active \overline{BUSY} flag will be set for the delayed port.

The \overline{BUSY} flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's \overline{BUSY} flag. \overline{BUSY} is set at speeds that permit the processor to hold the operation and its respective address data. It is important to note that the write operation is invalid for the

port that has \overline{BUSY} set LOW. The delayed port will have access when \overline{BUSY} goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before \overline{CE} , on-chip control logic arbitrates between \overline{CEL} and \overline{CER} for access; or (2) if the \overline{CE} s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table II). In either mode of arbitration, the delayed port's \overline{BUSY} flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION**MASTER/SLAVE DESCRIPTION:**

Expanding the data bus width to sixteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its \overline{BUSYL} while another activates its \overline{BUSYR} signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one arbitrator, in the MASTER, is used. The SLAVE has \overline{BUSY} inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed, until after the \overline{BUSY} input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past \overline{BUSY} to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to \overline{BUSY} from the MASTER.

TRUTH TABLES

T-46-23-12

TABLE I - NON-CONTENTION
READ/WRITE CONTROL(4)

Left Or Right Port(1)				Function
R/W	CE	OE	D0-7	
X	H	X	Z	Port Disabled and in Power Down Mode IsB2 or IsB4
X	H	X	Z	CE _R = CE _L = H, Power Down Mode, IsB1 or IsB3
L	L	X	DATA _{IN}	Data on Port Written into Memory(2)
H	L	L	DATA _{OUT}	Data in Memory Output on Port(3)
H	L	H	Z	High Impedance Outputs

2689 tbl 18

NOTES:

1. A0L-A9L = A0R-A9R
2. If BUSY = L, data is not written
3. If BUSY = L, data may not be valid, see t_{W02} and t_{W03} timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

TABLE II - INTERRUPT FLAG(1, 4)

Left Port					Right Port					Function
R/WL	CEL	OEL	A0L-A9L	INTL	R/WR	CE _R	OER	A0L-A9R	INTR	
L	L	X	3FF	X	X	X	X	X	L(2)	Set Right INTR Flag
X	X	X	X	X	X	L	L	3FF	H(3)	Reset Right INTR Flag
X	X	X	X	L(3)	L	L	X	3FE	X	Set Left INTL Flag
X	L	L	3FE	H(2)	X	X	X	X	X	Reset Left INTL Flag

2689 tbl 19

NOTES:

1. Assumes BUSYL = BUSYR = H.
2. If BUSYL = L, then NC.
3. If BUSYR = L, then NC.
4. H = HIGH, L = LOW, X = DON'T CARE, NC = NO CHANGE

TABLE III - ARBITRATION(2)

Left Port		Right Port		Flags(1)		Function
CEL	A0L-A9L	CE _R	A0R-A9R	BUSYL	BUSYR	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	≠ A0R-A9R	L	≠ A0L-A9L	H	H	No Contention
Address Arbitration With CE Low Before Address Match						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
CE Arbitration With Address Match Before CE						
LL5R	= A0R-A9R	LL5R	= A0L-A9L	H	L	L-Port Wins
RL5L	= A0R-A9R	RL5L	= A0L-A9L	L	H	R-Port Wins
LW5R	= A0R-A9R	LW5R	= A0L-A9L	H	L	Arbitration Resolved
LW5R	= A0R-A9R	LW5R	= A0L-A9L	L	H	Arbitration Resolved

2689 tbl 20

NOTES:

1. INT Flags Don't Care.
2. X = DON'T CARE, L = LOW, H = HIGH
LV5R = Left Address Valid ≥ 5ns before right address.
RV5L = Right Address Valid ≥ 5ns before left address.
LL5R = Left CE = LOW ≥ 5ns before Right CE.
RL5L = Right CE = LOW ≥ 5ns before Left CE.
LW5R = Left and Right CE = LOW within 5ns of each other.