

LINEAR INTEGRATED CIRCUITS

PROGRAMMABLE, OFF-LINE, PWM CONTROLLER

DESCRIPTION

Although containing most of the features required by all types of switching power supply controllers, the SG1840 family has been optimized for highly-efficient boot-strapped primary-side operation in forward or flyback power converters. Two important features for this mode are a starting circuit which requires little current from the second operation over a wide input voltage range.

In addition to startup and normal regulating PWM functions, these devices offer a built-in protection from over-voltage, under-voltage, and over-current fault conditions. This monitoring circuitry contains the added features that any fault will initiate a complete shutdown with provisions for either latch-off or automatic restart. In the latch-off mode, the controller may be started and stopped with external pulsed or steady-state commands.

Other performance features of these devices include a 1% accurate reference, provision for slow-turn-on and duty-cycle limiting, and high-speed pulse-by-pulse current limiting in addition to current fault shutdown.

The SG1840 PWM output stage includes a latch to insure only a single pulse per period and is designed to optimize the turn off of an external switching device by conducting during the "OFF" time with a capability for both high peak current and low saturation voltage. These devices are available in an 18-pin dual-in-line plastic or ceramic package.

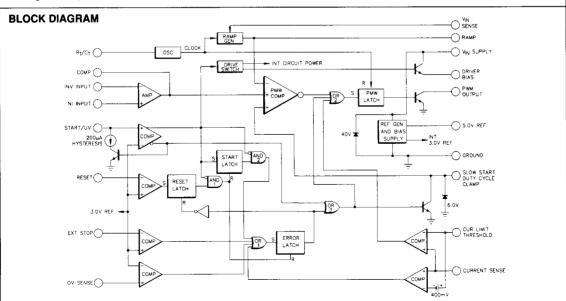
The SG1840 is characterised for operation over the full military ambient temperature range or -55°C to 125°C. The SG2840 and SG3840 are designed for operation from -25°C to 85°C and 0°C to 70°C, respectively.

FEATURES

- All control, driving, monitoring, and protection functions included
- High Frequency Initial Accuracy
- . Low-current, Off-line start circuit
- Feed-forward line regulation over 4 to 1 input range
- PWM latch for single pulse per period
- Pulse-by-pulse current limiting plus shutdown for over-current fault
- . No start-up or shutdown transients
- . Slow turn-on and maximum duty-cycle clamp
- Shutdown upon over- or under-voltage sensing
- Latch off or continuous retry after fault
- · Remote, pulse-commandable start/stop
- PWM output switch usable to 1A peak current
- 1% reference accuracy
- 500kHz operation
- 70dB PSRR
- · Linear frequency response

HIGH RELIABILITY FEATURES-SG1840

- + Available to MIL-STD-883
- ◆ SG Level "S" processing available

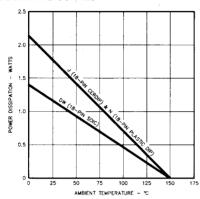


ABSOLUTE MAXIMUM RATINGS (Note 1)

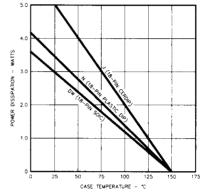
Supply Voltage (+ V _{IN})	
Voltage Driven	32V
Current Driven (self-limiting)	100mA
PWM Output Voltage (Pin 12)	40V
PWM Output Current (continuous)	
PWM Output Peak Energy Discharge	20µ Joules
Driver Bias Current (Pin 14)	200mA
Reference Output Current (Pin 16)	50mA
Slow-start Sink Current (Pin 8)	20 mA
Note 1. Values beyond which damage may occur.	

+ V _{IN} Sense Current (Pin 11)	10mA
Current Limit Inputs (Pins 6 & 7)	
Comparator Inputs (Pins 2,3,4,5,17,18)	0.3V to V _{IN}
Operating Junction Temperature	
Hermetic (J package)	150°C
Plastic (N, DW packages)	150°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 Seconds)	300°C

THERMAL DERATING CURVES







MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage Range	8V to 30V	Oscillator I
Error Amp Common Mode Range	1.5V to 5.5V	Oscillator 7
PWM Output Current (continuous)	0 to 200mA	Oscillator 7
Driver Bias Output Current	0 to 50mA	Operating
Reference Load Current	0 to 20mA	SG1840
+ V _{IN} Sense Current Range	10μA to 1.0mA	SG2840
Ramp Generator Capacitor Range	620pF to 0.1µF	SG3840
Note 2. Range over which the device is functional a	and parameter limits are	e guaranteed.

Oscillator Frequency Hange	100Hz to 500KHz
Oscillator Timing Resistor (R _T)	1K Ω to 100K Ω
Oscillator Timing Capacitor (C _T)	620pF to 0.1μF
Operating Ambient Temperature Range:	
SG1840	55°C to 125°C
SG2840	25°C to 85°C
SG2840SG3840	

ELECTRICAL SPECIFICATIONS

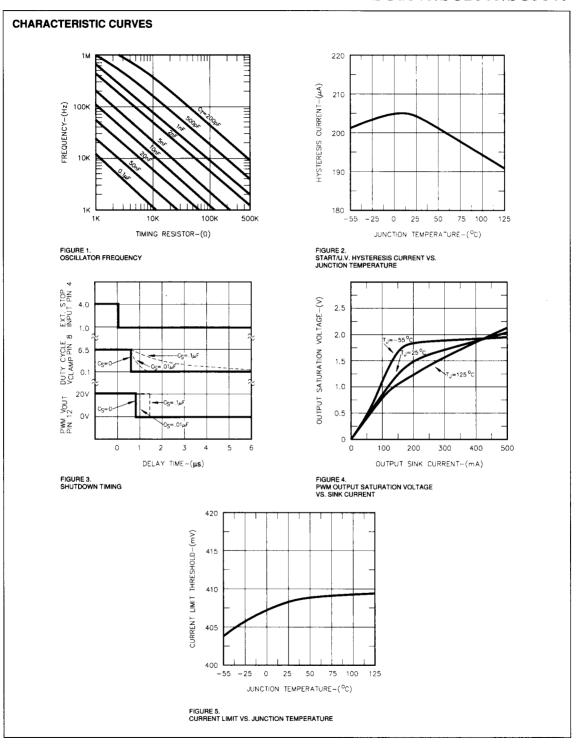
(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1840 with -55°C \leq T_{Λ} \leq 125°C, SG2840 with -25°C \leq T_{Λ} \leq 85°C, SG3840 with 0°C \leq T_{Λ} \leq 70°C, V_{$|_{N}$} = 20V. R_{$_{T}$} = 20K Ω , C_{$_{T}$} = 0.001 μ F, C_{$_{R}$} = 0.001 μ F, and Current Limit Threshhold = 200mV. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Lest Conditions		SG1840/2840			SG3840		
Faranielei			Тур.	Max.	Min.	Тур.	Max.	Units
Power Inputs Section							•	
Start-Up Current	V _{IN} = 30V, Pin 2 = 2.5V, T _i = 25°C	T	5	7		5	7	mA
Start-Up Current T.C. (Note 3)	$V_{IN} = 30V$, Pin 2 = 2.5V	Ī	-0.1	-0.2		-0.1	-0.2	%/°C
Operating Current	$V_{IN}^{(1)} = 30V$, Pin 2 = 3.5V	5	10	15	5	10	15	mA
Supply OV Clamp	I _{IN} = 20mA	33	40	45	33	40	48	V
Reference Section								
Reference Voltage	T ₁ = 25°C	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation	V _{IN} = 8 to 30V		10	15		10	20	mV
Load Regulation	I, = 0 to 20mA	- 1	10	20		10	30	mV
Temperature Coefficient (Note 3)	Över operating temperature range	1		±0.4			±0.4	mV/°C
Short Circuit Current	V _{REF} = 0, T _{.I} = 25°C	1	-80	-100		-80	-100	mA

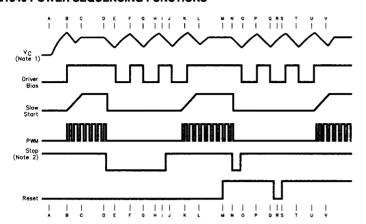
ELECTRICAL SPECIFICATIONS (continued)

Parameter	lest Conditions I		SG1840/2840			SG3840		
		Min.	Тур.	Max.	Min.	Тур.	Max.	Unit
Oscillator Section				,				
Nominal Frequency	T _J = 25°C	47	50	53	45	50	55	KH
H.F. Initial Accuracy (Note 3)	$R_T = 3K\Omega$, $C_T = 910pF$	270	300	330	270	300	330	KH
Voltage Stability	V _{IN} = 8 to 30V		0.5	1"		0.5	1 1	%
Temperature Coefficient (Note 3)	Over operating temperature range	1	}	±.08	Ī		±.08	%/°
Maximum Frequency	$R_{r} = 2K\Omega, C_{r} = 620pF$	500			500			Κŀ
Ramp Generator Section								
Ramp Current, Minimum	I _{SENSE} = -10μA		-11	-14		-11	-14	μA
Ramp Current, Maximum	I _{SENSE} = 1.0mA	-0.9	-0.95		-0.9	-0.95		m
Ramp Valley	SENSE	0.3	0.5		0.3	0.5		Ϊ́ν
Ramp Peak	Clamping Level	3.9	4.2	4.5	3.9	4.2	4.5	ľv
Error Amplifier Section	Oldinping 2000	1 0.0		7.0	0.0	7.2	7.5	
Input Offset Voltage	V _{CM} = 5.0V		0.5	5		2	10	m\
Input Bias Current	-CM - 0.0	Ì	0.5	2	•	1	5	μ/
Input Offset Current			0.5	0.5		'	0.5	μ/ μ/
Open Loop Gain	AV 1 to 2V	60	66	0.5		66	0.5	μν di
•	ΔV _o = 1 to 3V Minimum Total Range	0.3	00	25	60	סס	25	
Output Swing (Max. Output ≤ Ramp Peak - 100mV)		1		3.5	0.3		3.5	V
CMRR	V _{CM} = 1.5 to 5.5V	70	80		70	80		d
PSRR	V _{IN} = 8 to 30V	70	90	[70	90		d₽
Short Circuit Current	$V_{\text{comp}} = 0V$	1	-4	-10		-4	-10	m.
Gain Bandwidth (Note 3)	T, = 25°C, A _{vot} = 0dB	1	2		1	2		MH
Siew Rate (Note 3)	$T_J = 25^{\circ}C$, $A_{VCL} = 0dB$	1	0.8			0.8		V/,
PWM Section								
Continuous Duty Cycle Range	Minimum Total Continuous Range, Ramp	5		95	5		95	%
(other than zero) (Note 3)	Peak < 4.2V	İ			i - '			
Output Saturation	I _{out} = 20mA		0.2	0.4	i i	0.2	0.4	Ιv
	I _{OUT} = 200mA	1	1.7	2.2	1	1.7	2.2	ľv
Output Leakage	V _{OUT} = 40V	1	0.1	10	•	0.1	10	u.A
Comparator Delay (Note 3)	Pin 8 to Pin 12	1	300	500	•	300	500	ns
Comparator Delay (Note 3)	T ₁ = 25°C, R ₁ = 1kΩ	ł	300	300	l I	300	300	118
O	1			L				
Sequencing Functions Section Comparator Thresholds	- Bino 0 2 4 5	100	0.0					V
	Pins 2, 3, 4, 5	2.8	3.0	3.2	2.8	3.0	3.2	
Input Bias Current	Pins 3, 4, 5 = 0V		-1.0	-3.0		-1.0	-3.0	μ/
Start/UV Hysteresis Current	Pin 2 = 2.5V	150	200	250	150	200	250	μ/
Input Leakage	Input V = 20V	Ţ	0.1	10	1 .	0.1	10	μ/
Driver Bias Saturation Voltage	I _B = -50mA	1	2	3		2	3	١V
Driver Bias Leakage	$V_B = 0V$		-0.1	-10	l .	-0.1	-10	μ/
Slow-Start Saturation	I _s = 2mA	1	0.2	0.5		0.2	0.5	V
Slow-Start Leakage	$V_{s} = 4.5V$		0.1	2.0	l	0.1	2.0	μ/
Current Control Section								
Current Limit Offset		T	0	5		0	10	m'
Current Shutdown Offset		370	400	430	360	400	440	m'
Input Bias Current	Pin 7 = 0V		-2	-5		-2	-5	μ/
Common Mode Range (Note 3)		-0.4	_	3.0	-0.4	_	3.0	ľ
	T _J = 25°C, Pin 7 to 12, R _L = 1k	1 5.7	1	0.0	1	l	400	

Note 3. These parameters, although guaranteed over the recommended operating condition, are not 100% tested in production.



SG1840 POWER SEQUENCING FUNCTIONS

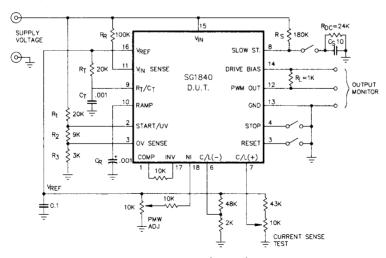


Note 1. V_C represents an analog of the output voltage generated by a primary-referenced secondary winding on the power transformer. It is the voltage monitored by the start/UV comparator and, in most cases, is the supply voltage, V_{IN}, for the SG1840.

Note 2. Although input to External Stop, Pin 4, is shown, results are the same for any fault input which sets the Error Latch.

TIME	EVENT	TIME	EVENT
Α	Initial turn-on. V _c rises with light load	L	Return to normal run state
В	Start threshold. Driver Bias Loads V	М	Reset Latch set signal removed
С	Operating PWM regulates V _c	N	Error Latch set with momentary fault
D	Stop input sets Error Latch turning off PWM	0	Error Latch does not reset as Reset Latch is reset
E F	UV low threshold. Error Latch remains set Start turns on Driver Bias but Error Latch still set	P }	${\rm V_{\rm c}}$ and Driver Bias recycle with no turn-on
$_{H}^{G}\}$	V _c and Driver Bias continue to cycle	R S	Reset Latch set is set with momentary Reset signal V _c must complete cycle to turn-on
1	Stop command removed	T	Start and Error Latches reset
J	Error Latch reset at UV low threshold	U	Normal start initiated
K	Start threshold now removes slow-start clamp	V	Return to normal run state

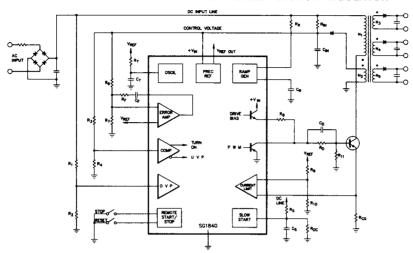
OPEN LOOP TEST CIRCUIT



Nominal Frequency
$$=\frac{1}{R_{T}C_{T}}=50$$
KHz UV Fault Voltage $=3\left(\frac{R_{1}+R_{2}+R_{3}}{R_{2}+R_{3}}\right)=8$ V Current Limit $=200$ mV Current Fault Voltage $=600$ mV Start Voltage $=3\left(\frac{R_{1}+R_{2}+R_{3}}{R_{2}+R_{3}}\right)+0.2$ R₁ $=12$ V OV Fault Voltage $=3\left(\frac{R_{1}+R_{2}+R_{3}}{R_{2}+R_{3}}\right)=32$ V Duty Cycle $=50$ %

FUNCTIONAL DESCRI	PTION
PWM Control	
1. Oscillator	Generates a fixed-frequency internal clock from an external R_{τ} and C_{τ} . Frequency = $\frac{1}{R_{\tau}C_{\tau}}$
2. Ramp Generator	Develops a linear ramp with a slope defined externally by $\frac{dv}{dt} = \frac{\text{sense voltage}}{R_R C_R}$ C_R is normally selected $\leq C_R$ and its value will have some effect upon valley voltage. C_R terminal can be used as an input port for current mode control.
3. Error Amplifier	Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance; unity-gain stable.
4. Reference Generator	Precision 5.0V for internal and external usage to 50mA. Tracking 3.0V reference for internal usage only with nominal accuracy of ±2%. 40V clamp zener for chip 0V protection. 100mA maximum current.
5. PWM Comparator	Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs.
6. PWM Latch	Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by pulse current limit comparator, or the error latch. Resets with each internal clock pulse.
7. PWM Output Switch	Transistor capable of sinking current to ground which is off during the PWM on-time and turns on to terminate the power pulse. Current capacity is 400mA saturated with peak capacitance discharge in excess of one amp.
Sequencing Functions	
1. Start/UV Sense	This comparator performs three functions— With an increasing voltage, it generates a turn-on signal at a start threshold. With a decreasing voltage, it generates a UV fault signal at a lower level separated by a 200µA hysteresis current. At the UV threshold, it also resets the Error Latch if the Reset Latch has been set.
2. Drive Switch	Disables most of the chip to hold internal current consumption low, and Driver Bias OFF, until input voltage reaches start threshold.
3. Driver Bias	Supplies drive current to external power switch to provide turn-on bias.
4. Slow Start	Clamps low to hold PWM OFF. Upon release, rises with rate controlled by R_sC_s for slow increase of output pulse width. Also used to clamp maximum duty cycle with divider $R_s R_{DC}$.
5. Start Latch	Keeps low input voltage at initial turn-on from being defined as a UV fault. Sets at start level to monitor for UV fault.
6. Reset Latch	When reset, this latch insures no reset signal to either Start or Error latches so that first fault will lock the PWM off. When set, this latch resets the Start and Error latches at the UV low threshold, allowing a restart.
Protection Functions	Then set, this later resets the otal and Eller lateres at the OV low threshold, allowing a restart.
1. Error Latch	When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset. Inputs to Error Latch are: a. UV low (after turn-on) b. OV high c. Stop low d. Current Sense 400mV over threshold Error Latch resets at UV threshold if Reset Latch is set.
2. Current Limiting	Differential input comparator terminates individual output pulses each time sense voltage rises above threshold. When sense voltage rises to 400mV above threshold, a shutdown signal is sent to Error Latch.

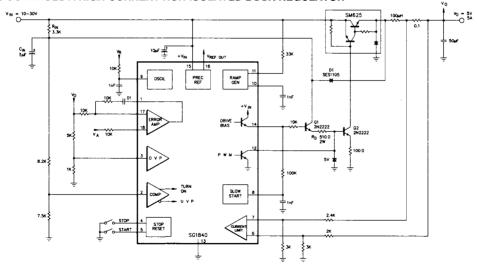
SG1840 PROGRAMMABLE PWM CONTROLLER IN A SIMPLIFIED FLYBACK REGULATOR



In this application, complete control is maintained on the primary side. Control power is provided by $R_{\rm IN}$ and $C_{\rm IN}$ during start-up, and by a primary-referenced low voltage winding, N2, for efficient operation after start. The error amplifier loop is closed to regulate the DC voltage from N2 with other outputs following through their magnetic coupling - a task made even easier with the SG1840's feed-forward line regulation.

Not shown are protective snubbers or additional interface circuitry which may be required by the choice of the high-voltage switch, Qs, or the application.

SG1840 CONTROLS A HIGH-CURRENT NON-ISOLATED BUCK REGULATOR



Although primarily intended for transformer-coupled power systems, the SG1840's advantages of feed-forward for high ripple-rejection, a fully contained fault monitoring system and remote start/stop capability make it worth considering for other types of regulators. Since the fault logic within the SG1840 requires recycling the voltage sensed by the Start/UV Comparator to reset the error latch, a need for automatic restart must be addressed in a manner similar to that shown. In this simple, non-isolated, buck regulator, diode D1 provides a low-impedence bootstrapped drive power source after start-up is achieved through R_{IN} and C_{IN}. When a fault shutdown terminates switching action, the loading of Q1 and R_d will lower the voltage on pin 2 to effect an automatic re-start attempt which will continuously recycle until the fault is removed.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
8-PIN CERAMIC DIP	SG1840J/883B	-55°C to 125°C	COMPENSATION 1 18 NON-INV INPUT
- PACKAGE	SG1840J	-55°C to 125°C	START UV 2 17 INVERTING INPUT
	SG2840J	-25°C to 85°C	OV SENSE 3 16 5.0V REF
			STOP 4 15 +V_SUPPLY
	SG3840J	0°C to 70°C	RESET _ 5 14 _ DRIVER BIAS
			CURRENT THRESHOLD = 6 13 GROUND
			CURRENT SENSE ☐ 7 12 ☐ PWM OUTPUT
8-PIN PLASTIC DIP	SG2840N	-25°C to 85°C	SLOW START = 8 11 = V _{IN} SENSE
I - PACKAGE	SG3840N	0°C to 70°C	R _T C _T ⊆ 910 □ RAMP
8-PIN WIDE BODY	SG2840DW	-25°C to 85°C	
LASTIC S.O.I.C.	SG3840DW	0°C to 70°C	COMPENSATION TTT 1 18 TT NON-INV INPUT
W - PACKAGE	0000.02	0 0 10 70 0	START UV 17 2 17 INVERTING INPU
			OV SENSE = 3 16 = 5.0V REF
			STOP 4 15 1 +V SUPPLY
			RESET 15 14 1 DRIVER BIAS
			CURRENT THRESHOLD T 6 13 T GROUND
			CURRENT SENSE 🔲 7 12 🛄 PWM OUTPUT
			SLOW START 3 8 11 7 V. SENSE
	ı		R,C, II 9 10 II RAMP

Note 1. Contact factory for JAN and DESC product availability.

2. All parts are viewed from the top.