Signetics

Military Logic Products

54175, 54LS175
Flip-Flops

Quad D Flip-Flops

Product Specification

FEATURES

- **Four edge-triggered D flip-flops**
- **Three speed-power ranges available**
- **Buffered common clock**
- **Buffered, asynchronous Master Reset**

DESCRIPTION

The 54175 and 54LS175 are quad, edge-triggered D-type flip-flop with individual D inputs and both Q and $\overline{Q}$ outputs. The common buffered clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All Q outputs will be forced Low independently of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where both true and complement outputs are required, and the Clock and Master Reset are common to all storage elements.

ORDERING INFORMATION

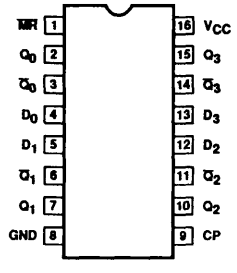
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54175/BEA 54LS175/BEA
16-Pin Ceramic FlatPack	54175/BFA 54LS175/BFA
16-Pin Ceramic LLCC	54LS175/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54	54LS
All	Inputs	1UL	1LSUL
All	Outputs	10UL	10LSUL

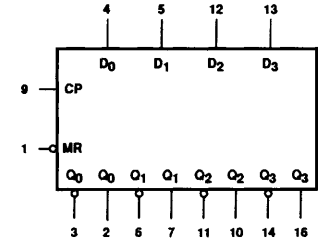
NOTE: Where a 54 Unit Load (UL) is understood to be 40μA I_{IH} and -1.6mA I_{IL}, and a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



For LLCC Pin Assignments see JEDEC Standard No. 2

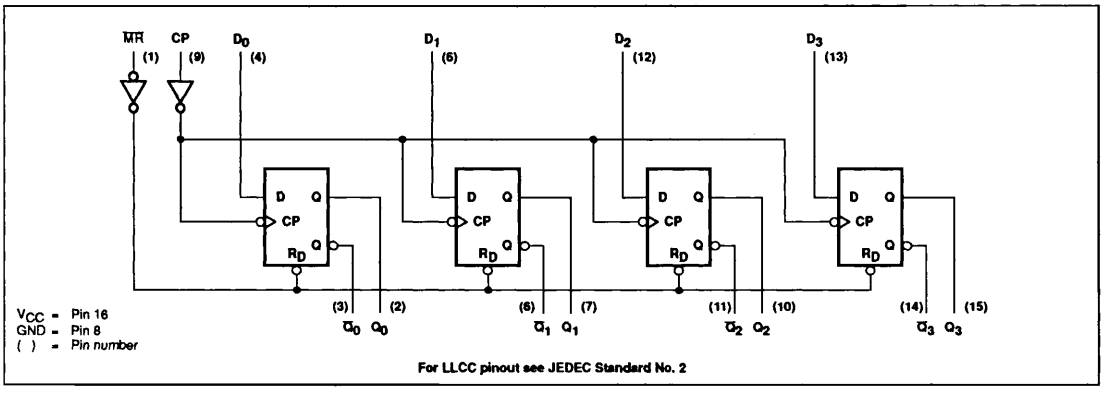
LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

For LLCC Pin Assignments see JEDEC Standard No. 2

LOGIC DIAGRAM



For LLCC pinout see JEDEC Standard No. 2

FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{MR}$	CP	D_n	Q_n	$\overline{Q}_n$
Reset (clear)	L	X	X	L	H
Load "1"	H	↑	h	H	L
Load "0"	H	↑	l	L	H

H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High Clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the Low-to-High Clock transition
X = Don't Care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	54	54LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_I	Input voltage range	-0.5 to +5.5	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	-30 to +1.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to $+V_{CC}$	-0.5 to $+V_{CC}$	V
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54			54LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			2.0			V
V_{IL}	Low-level input voltage			+0.8			+0.7	V
I_{IK}	Input clamp current			-12			-18	mA
I_{OH}	High-level output current			-800			-400	µA
I_{OL}	Low-level output current			16			4	mA
T_A	Operating free-air temperature range	-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		54175			54LS175			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.4	3.4		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max			0.2	0.4		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5			-1.5	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max	V_I = 5.5V			1.0				mA
			V_I = 7.0V						0.1	mA
I_{IH1}	High-level input current	V_{CC} = Max	V_I = 2.4V			40				µA
			V_I = 2.7V						20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V				-1.6			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-20		-57	-20		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max			30	45		11	18	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54[5]		54LS		UNIT
			C_L = 15pF		C_L = 15pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to outputs	Waveform 1		30 35		25 25	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to outputs	Waveform 3		25 35		30 30	ns ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		UNIT
			Min	Max	Min	Max	
t_w	Clock pulse width	Waveform 1	20		20		ns
t_w	Master Reset pulse width	Waveform 3	20		20		ns
t_s(H)	Setup time, High data to CP	Waveform 2	20		20		ns
t_h(H)	Hold time, High data to CP	Waveform 2	5		5		ns
t_s(L)	Setup time, Low data to CP	Waveform 2	20		20		ns
t_h(L)	Hold time, Low data to CP	Waveform 2	5		5		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 3	25		25		ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS[5]		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to outputs	Waveform 1		34 39		30 30	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to outputs	Waveform 3		29 39		35 35	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to outputs	Waveform 1		44 51		39 39	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to outputs	Waveform 3		33 51		46 46	ns ns

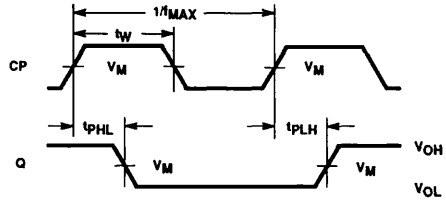
AC SETUP REQUIREMENTS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		UNIT
			Min	Max	Min	Max	
t_w	Clock pulse width	Waveform 1	20		20		ns
t_w	Master Reset pulse width	Waveform 3	20		20		ns
t_s(H)	Setup time, High data to CP	Waveform 2	20		20		ns
t_h(H)	Hold time, High data to CP	Waveform 2	5		5		ns
t_s(L)	Setup time, Low data to CP	Waveform 2	20		20		ns
t_h(L)	Hold time, Low data to CP	Waveform 2	5		5		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 3	25		25		ns

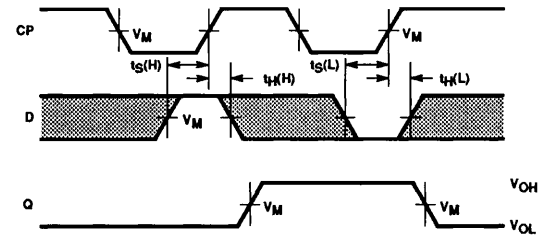
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With all outputs open and ≥4.0V applied to all Data and Master Reset inputs, I_{CC} is measured after a momentary ground, then 4.0V is applied to clock.
5. These parameters are guaranteed, but not tested.

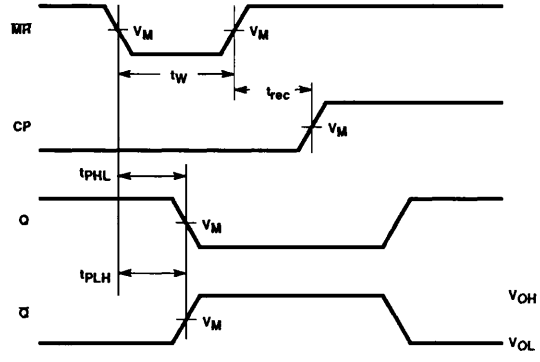
AC WAVEFORMS



Waveform 1. Clock to Output Delays and Clock Pulse Width



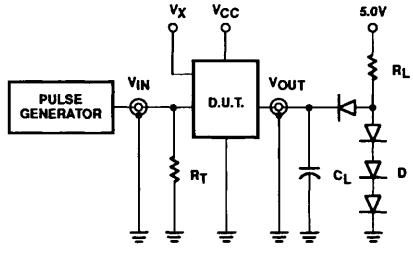
Waveform 2. Data Setup and Hold Times



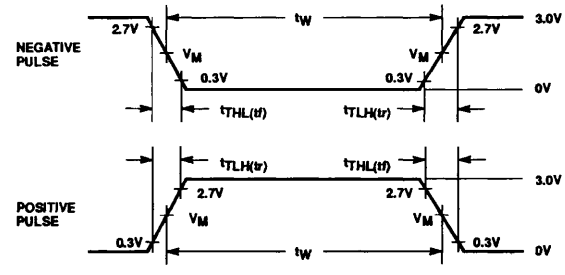
Waveform 3. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time

NOTE: For all waveforms V_M = 1.5V for 54 and 54S; V_M = 1.3V for 54LS
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns
54XXX	400Ω	1.5V	1MHz	500ns	≤7ns	≤7ns

DEFINITIONS:

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.