# DATA SHEET

## 74ABT2952
## Octal registered transceiver (3-State)

Product specification
Supersedes data of 1995 Jun 15
IC23 Data Handbook

1998 Feb 11

Philips
Semiconductors

PHILIPS

# Octal registered transceiver (3-State) 74ABT2952

## FEATURES

- 8-bit registered transceiver
- Independent registers for A and B buses
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Power-up 3-State
- Power-up reset
- Live insertion/extraction permitted

## DESCRIPTION

The 74ABT2952 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT2952 device is an 8-bit registered transceiver. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses. Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable ($\overline{CEXX}$) is Low. The data is then present at the 3-State output buffers, but is only accessible when the Output Enable ($\overline{OEXX}$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

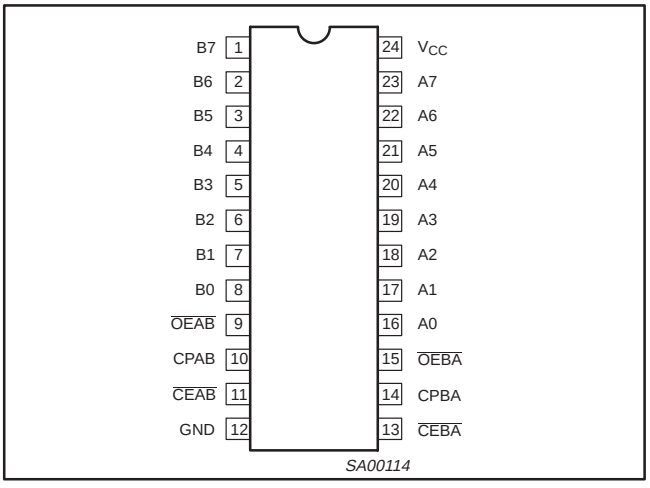
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS $T_{amb}$ = 25°C; GND = 0V | TYPICAL | UNIT |
|---|---|---|---|---|
| $t_{PLH}$ $t_{PHL}$ | Propagation delay CPBA to An or CPAB to Bn | $C_L$ = 50pF; $V_{CC}$ = 5V | 5.7 | ns |
| $C_{IN}$ | Input capacitance | $V_I$ = 0V or $V_{CC}$ | 4 | pF |
| $C_{I/O}$ | I/O capacitance | Outputs disabled; $V_O$ = 0V or $V_{CC}$ | 7 | pF |
| $I_{CCZ}$ | Total supply current | Outputs disabled; $V_{CC}$ =5.5V | 110 | µA |

## ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | DWG NUMBER |
|---|---|---|---|---|
| 24-Pin Plastic DIP | –40°C to +85°C | 74ABT2952 N | 74ABT2952 N | SOT222-1 |
| 24-Pin plastic SO | –40°C to +85°C | 74ABT2952 D | 74ABT2952 D | SOT137-1 |
| 24-Pin Plastic SSOP Type II | –40°C to +85°C | 74ABT2952 DB | 74ABT2952 DB | SOT340-1 |
| 24-Pin Plastic TSSOP Type I | –40°C to +85°C | 74ABT2952 PW | 7ABT2952PW DH | SOT355-1 |

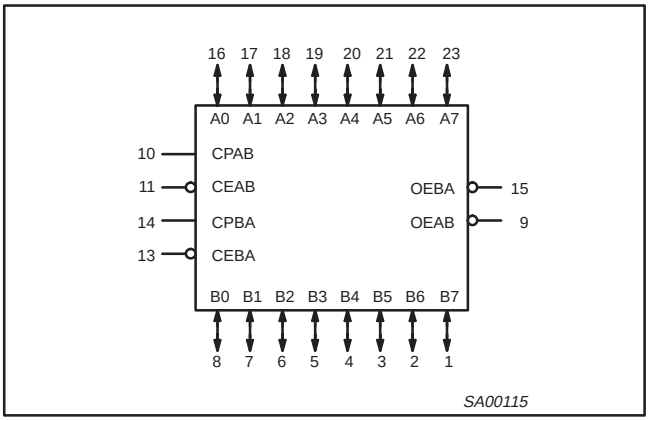
## PIN CONFIGURATION



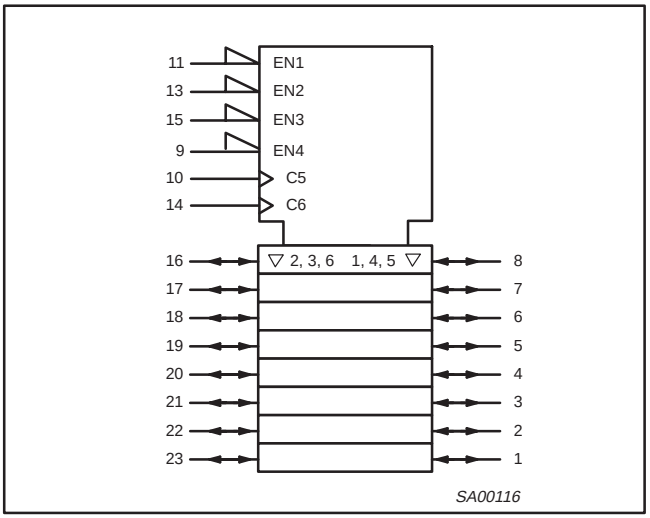

## PIN DESCRIPTION

| PIN NUMBER | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 10, 14 | CPAB / CPBA | Clock input A to B / Clock input B to A |
| 11, 13 | $\overline{CEAB}$ / $\overline{CEBA}$ | Clock enable input A to B / Clock enable input B to A |
| 16, 17, 18, 19, 20, 21, 22, 23 | A0 – A7 | Data inputs/outputs (A side) |
| 1, 2, 3, 4, 5, 6, 7, 8 | B0 – B7 | Data outputs/outputs (B side) |
| 9, 15 | $\overline{OEAB}$ / $\overline{OEBA}$ | Output enable inputs |
| 12 | GND | Ground (0V) |
| 24 | $V_{CC}$ | Positive supply voltage |

## LOGIC SYMBOL




## LOGIC SYMBOL (IEEE/IEC)




## FUNCTION TABLE for Register An or Bn

| INPUTS | | | INTERNAL Q | OPERATING MODE |
|---|---|---|---|---|
| An or Bn | CPXX | $\overline{CEXX}$ | | |
| X | X | H | NC | Hold data |
| L<br>H | ↑<br>↑ | L<br>L | L<br>H | Load data |

H = High voltage level
L = Low voltage level
↑ = Low–to–High transition
X = Don't care
XX = AB or BA
NC = No change

## FUNCTION TABLE for Output Enable

| INPUTS | INTERNAL Q | An or Bn OUTPUTS | OPERATING MODE |
|---|---|---|---|
| $\overline{OEXX}$ | | | |
| H | X | Z | Disable outputs |
| L<br>L | L<br>H | L<br>H | Enable outputs |

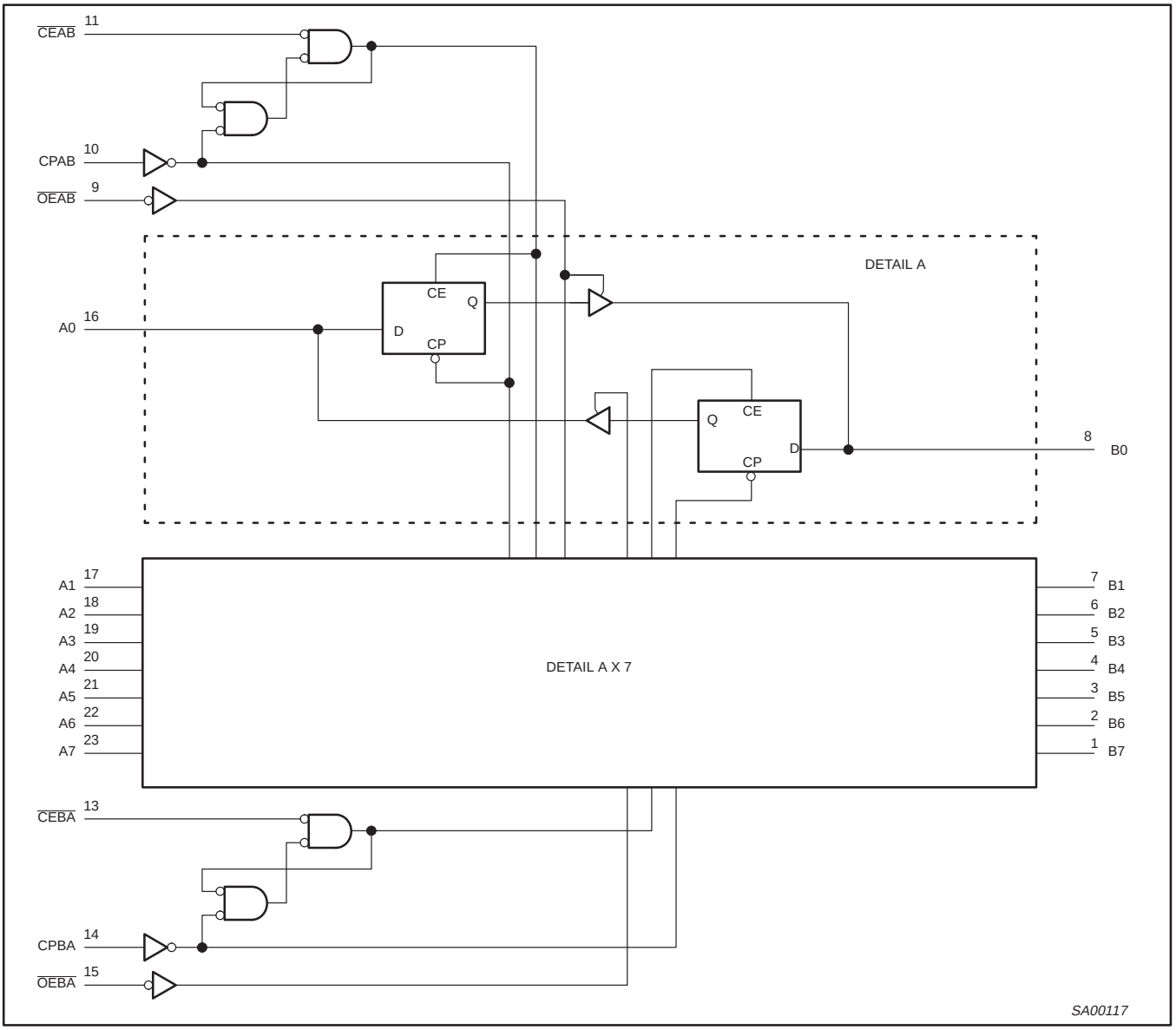
H = High voltage level
L = Low voltage level
X = Don't care
XX = AB or BA
Z = High impedance "off" state

## ABSOLUTE MAXIMUM RATINGS[1, 2]

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | DC supply voltage | | –0.5 to +7.0 | V |
| $I_{IK}$ | DC input diode current | $V_I < 0$ | –18 | mA |
| $V_I$ | DC input voltage[3] | | –1.2 to +7.0 | V |
| $I_{OK}$ | DC output diode current | $V_O < 0$ | –50 | mA |
| $V_{OUT}$ | DC output voltage[3] | output in Off or High state | –0.5 to +5.5 | V |
| $I_{OUT}$ | DC output current | output in Low state | 128 | mA |
| $T_{stg}$ | Storage temperature range | | –65 to 150 | °C |

**NOTES:**
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## LOGIC DIAGRAM




## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | UNIT |
|---|---|---|---|---|
| | | Min | Max | |
| $V_{CC}$ | DC supply voltage | 4.5 | 5.5 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | V |
| $V_{IH}$ | High-level input voltage | 2.0 | | V |
| $V_{IL}$ | Low-level Input voltage | | 0.8 | V |
| $I_{OH}$ | High-level output current | | –32 | mA |
| $I_{OL}$ | Low-level output current | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | 0 | 10 | ns/V |
| $T_{amb}$ | Operating free-air temperature range | –40 | +85 | °C |

## DC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | | TEST CONDITIONS | LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_{amb}$ = +25°C | | | $T_{amb}$ = –40°C to +85°C | | |
| | | | | Min | Typ | Max | Min | Max | |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = 4.5V; $I_{IK}$ = –18mA | | –0.9 | –1.2 | | –1.2 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = 4.5V; $I_{OH}$ = –3mA; $V_I$ = $V_{IL}$ or $V_{IH}$ | 2.5 | 3.5 | | 2.5 | | V |
| | | | $V_{CC}$ = 5.0V; $I_{OH}$ = –3mA; $V_I$ = $V_{IL}$ or $V_{IH}$ | 3.0 | 4.0 | | 3.0 | | V |
| | | | $V_{CC}$ = 4.5V; $I_{OH}$ = –32mA; $V_I$ = $V_{IL}$ or $V_{IH}$ | 2.0 | 2.6 | | 2.0 | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = 4.5V; $I_{OL}$ = 64mA; $V_I$ = $V_{IL}$ or $V_{IH}$ | | 0.42 | 0.55 | | 0.55 | V |
| $V_{RST}$ | Power-up output low voltage[3] | | $V_{CC}$ = 5.5V; $I_O$ = 1mA; $V_I$ = GND or $V_{CC}$ | | 0.13 | 0.55 | | 0.55 | V |
| $I_I$ | Input leakage current | Control pins | $V_{CC}$ = 5.5V; $V_I$ = GND or 5.5V | | ±0.01 | ±1.0 | | ±1.0 | µA |
| | | Data pins | $V_{CC}$ = 5.5V; $V_I$ = GND or 5.5V | | 5 | 100 | | 100 | µA |
| $I_{OFF}$ | Power-off leakage current | | $V_{CC}$ = 0.0V; $V_O$ = 4.5V; $V_I$ = 0.0V or 5.5V | | ±5.0 | ±100 | | ±100 | µA |
| $I_{PU}/I_{PD}$ | Power-up/down 3-State output current[4] | | $V_{CC}$ = 2.1V; $V_O$ = 0.5V; $V_I$ = GND or $V_{CC}$; $V_{OE}$ = Don't care | | ±5.0 | ±50 | | ±50 | µA |
| $I_{OZH}$ | 3-State output High current | | $V_{CC}$ = 5.5V; $V_O$ = 2.7V; $V_I$ = $V_{IL}$ or $V_{IH}$ | | 5.0 | 50 | | 50 | µA |
| $I_{OZL}$ | 3-State output Low current | | $V_{CC}$ = 5.5V; $V_O$ = 0.5V; $V_I$ = $V_{IL}$ or $V_{IH}$ | | –5.0 | –50 | | –50 | µA |
| $I_{CEX}$ | Output High leakage current | | $V_{CC}$ = 5.5V; $V_O$ = 5.5V; $V_I$ = GND or $V_{CC}$ | | 5.0 | 50 | | 50 | µA |
| $I_O$ | Output current[1] | | $V_{CC}$ = 5.5V; $V_O$ = 2.5V | –50 | –80 | –180 | –50 | –180 | mA |
| $I_{CCH}$ | Quiescent supply current | | $V_{CC}$ = 5.5V; Outputs High, $V_I$ = GND or $V_{CC}$ | | 110 | 250 | | 250 | µA |
| $I_{CCL}$ | | | $V_{CC}$ = 5.5V; Outputs Low, $V_I$ = GND or $V_{CC}$ | | 20 | 30 | | 30 | mA |
| $I_{CCZ}$ | | | $V_{CC}$ = 5.5V; Outputs 3-State; $V_I$ = GND or $V_{CC}$ | | 110 | 250 | | 250 | µA |
| $\Delta I_{CC}$ | Additional supply current per input pin[2] | | $V_{CC}$ = 5.5V; one input at 3.4V, other inputs at $V_{CC}$ or GND | | 0.3 | 1.5 | | 1.5 | mA |

**NOTES:**
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any $V_{CC}$ between 0V and 2.1V, with a transition time of up to 10msec. From $V_{CC}$ = 2.1V to $V_{CC}$ = 5V ± 10% a transition time of up to 100µsec is permitted.

## AC CHARACTERISTICS

GND = 0V; $t_R$ = $t_F$ = 2.5ns; $C_L$ = 50pF, $R_L$ = 500Ω

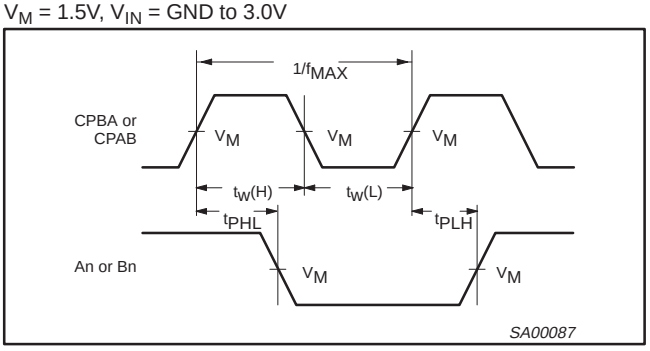
| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $T_{amb}$ = +25°C $V_{CC}$ = +5.0V | | | $T_{amb}$ = –40°C to +85°C $V_{CC}$ = +5.0V ±0.5V | | |
| | | | Min | Typ | Max | Min | Max | |
| $f_{MAX}$ | Maximum clock frequency | 1 | 150 | 250 | | 150 | | MHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>CPBA to An, CPAB to Bn | 1 | 2.0<br>2.5 | 3.2<br>3.8 | 6.6<br>7.2 | 2.0<br>2.5 | 7.6<br>8.2 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output enable time<br>$\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn | 3<br>4 | 1.0<br>2.2 | 3.2<br>4.4 | 4.8<br>6.2 | 1.0<br>2.2 | 5.8<br>7.5 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output disable time<br>$\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn | 3<br>4 | 2.0<br>1.5 | 3.6<br>2.8 | 7.6<br>7.1 | 2.0<br>1.5 | 8.1<br>7.6 | ns |

## AC SETUP REQUIREMENTS

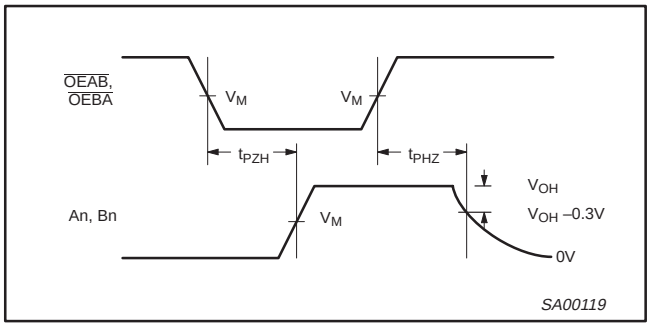
| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | $T_{amb}$ = +25°C<br>$V_{CC}$ = +5.0V | | $T_{amb}$ = –40°C to +85°C<br>$V_{CC}$ = +5.0V ±0.5V | |
| | | | Min | Typ | Min | |
| $t_S(H)$<br>$t_s(L)$ | Setup time<br>An to CPAB or Bn to CPBA | 2 | 4.5<br>3.5 | 2.2<br>1.6 | 4.5<br>3.5 | ns |
| $t_h(H)$<br>$t_h(L)$ | Hold time<br>An to CPAB or Bn to CPBA | 2 | 0.0<br>0.0 | –0.8<br>–1.4 | 0.0<br>0.0 | ns |
| $t_s(H)$<br>$t_s(L)$ | Setup time<br>$\overline{CEAB}$ to CPAB, $\overline{CEBA}$ to CPBA | 2 | 4.0<br>3.0 | 0.8<br>0.8 | 4.0<br>3.0 | ns |
| $t_h(H)$<br>$t_h(L)$ | Hold time<br>$\overline{CEAB}$ to CPAB, $\overline{CEBA}$ to CPBA | 2 | 0.0<br>0.0 | –0.7<br>–0.7 | 0.0<br>0.0 | ns |
| $t_w(H)$<br>$t_w(L)$ | CPAB or CPBA pulse width,<br>High or Low | 1 | 3.0<br>3.5 | 0.8<br>0.9 | 3.0<br>3.5 | ns |

## AC WAVEFORMS

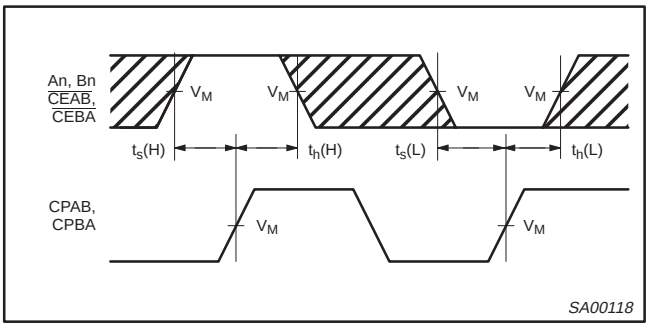
$V_M$ = 1.5V, $V_{IN}$ = GND to 3.0V



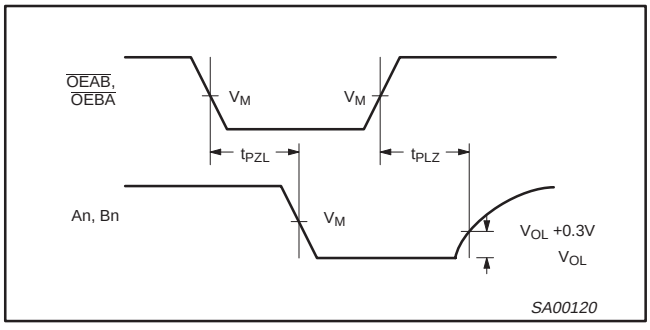

**Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency**




**Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level**

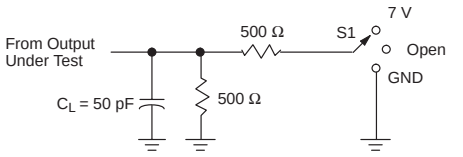



**Waveform 2. Data Setup and Hold Times**




**Waveform 4. 3–State Output Enable Time to Low Level and Output Disable Time from Low Level**

## TEST CIRCUIT AND WAVEFORMS




**Load Circuit**

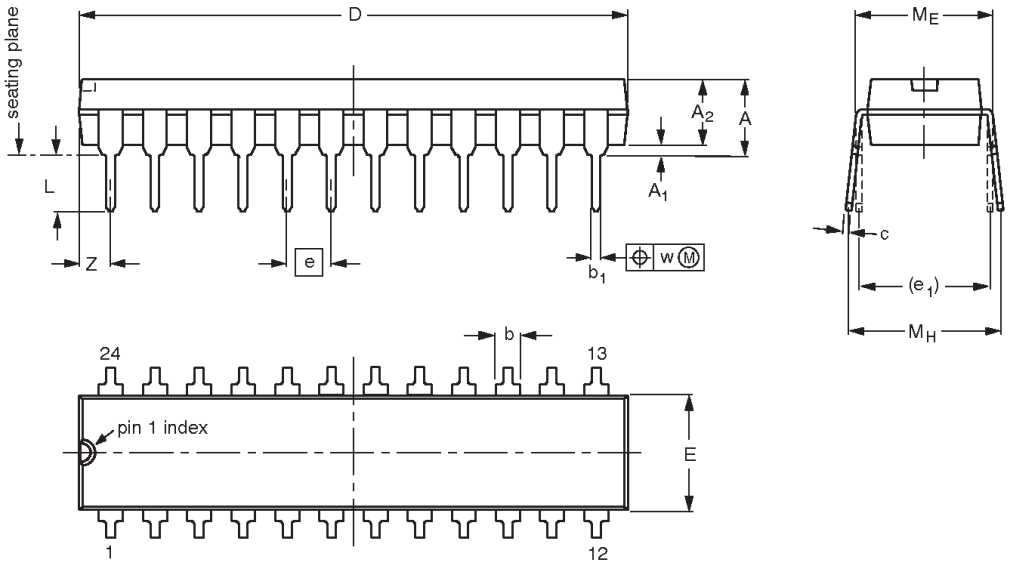
| TEST | S1 |
|---|---|
| $t_{pd}$ | open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | open |

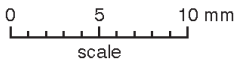
**DEFINITIONS**

$C_L$ = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

*SA00012*

## DIP24: plastic dual in-line package; 24 leads (300 mil) SOT222-1




**DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)**

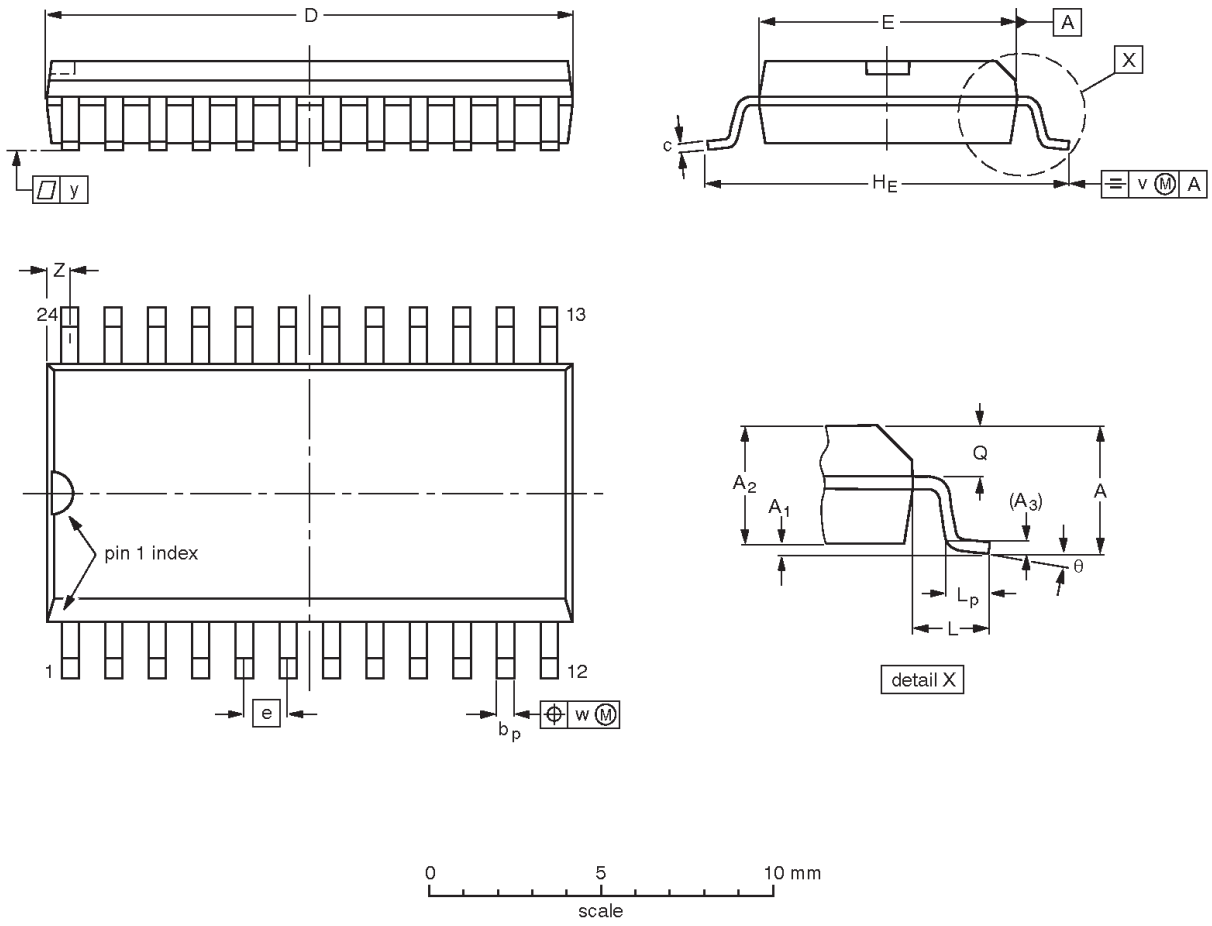
| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $e_1$ | L | $M_E$ | $M_H$ | w | $Z^{(1)}$ max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.70 | 0.38 | 3.94 | 1.63<br>1.14 | 0.56<br>0.43 | 0.36<br>0.25 | 31.9<br>31.5 | 6.73<br>6.48 | 2.54 | 7.62 | 3.51<br>3.05 | 8.13<br>7.62 | 10.03<br>7.62 | 0.25 | 2.05 |
| inches | 0.185 | 0.015 | 0.155 | 0.064<br>0.045 | 0.022<br>0.017 | 0.014<br>0.010 | 1.256<br>1.240 | 0.265<br>0.255 | 0.100 | 0.300 | 0.138<br>0.120 | 0.32<br>0.30 | 0.395<br>0.300 | 0.01 | 0.081 |

**Note**

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT222-1 | | MS-001AF | | | | 95-03-11 |

**SO24: plastic small outline package; 24 leads; body width 7.5 mm** **SOT137-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

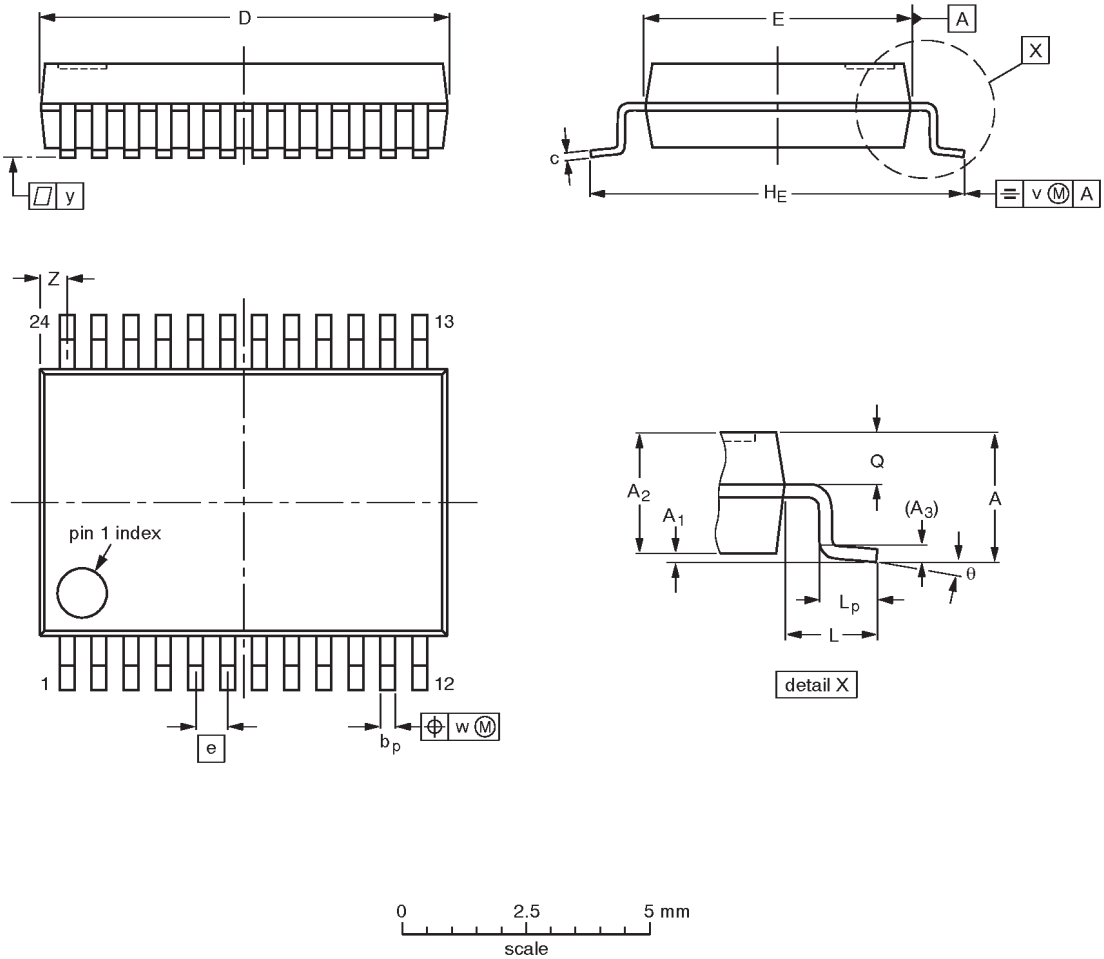
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.65 | 0.30<br>0.10 | 2.45<br>2.25 | 0.25 | 0.49<br>0.36 | 0.32<br>0.23 | 15.6<br>15.2 | 7.6<br>7.4 | 1.27 | 10.65<br>10.00 | 1.4 | 1.1<br>0.4 | 1.1<br>1.0 | 0.25 | 0.25 | 0.1 | 0.9<br>0.4 | $8^o$<br>$0^o$ |
| inches | 0.10 | 0.012<br>0.004 | 0.096<br>0.089 | 0.01 | 0.019<br>0.014 | 0.013<br>0.009 | 0.61<br>0.60 | 0.30<br>0.29 | 0.050 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT137-1 | 075E05 | MS-013AD | | | | ~~95-01-24~~<br>97-05-22 |

**SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm** **SOT340-1**




**DIMENSIONS (mm are the original dimensions)**

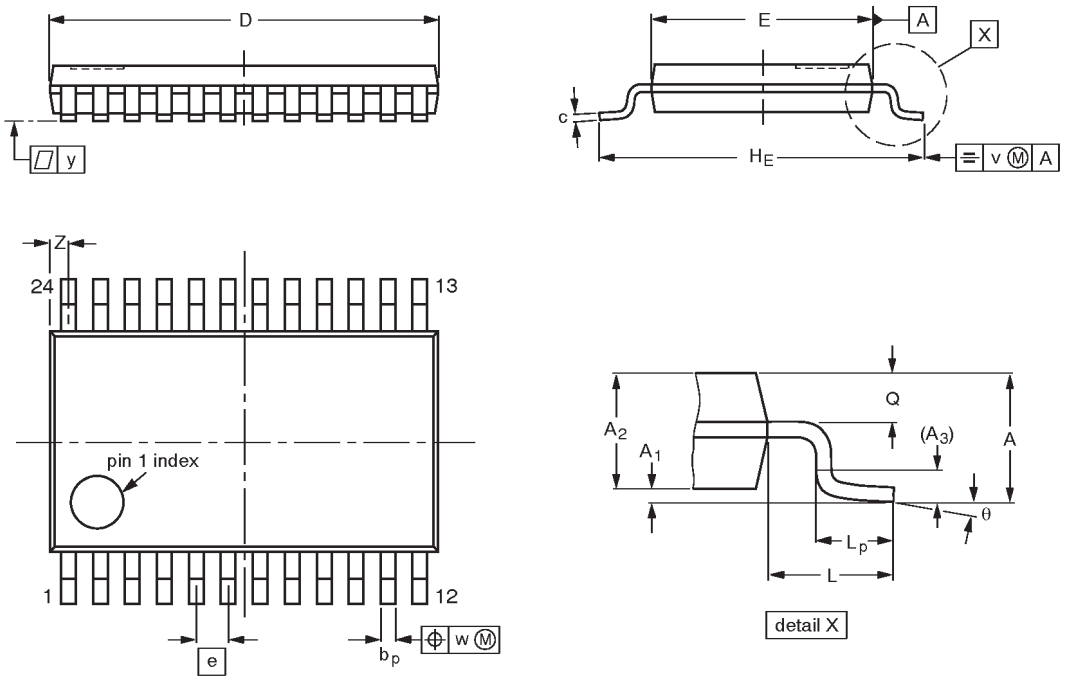
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.0 | 0.21<br>0.05 | 1.80<br>1.65 | 0.25 | 0.38<br>0.25 | 0.20<br>0.09 | 8.4<br>8.0 | 5.4<br>5.2 | 0.65 | 7.9<br>7.6 | 1.25 | 1.03<br>0.63 | 0.9<br>0.7 | 0.2 | 0.13 | 0.1 | 0.8<br>0.4 | 8°<br>0° |

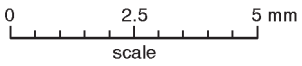
**Note**

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT340-1 | | MO-150AG | | | | ~~93-09-08~~<br>95-02-04 |

**TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm** **SOT355-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.10 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 7.9<br>7.7 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1.0 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.5<br>0.2 | 8°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT355-1 | | MO-153AD | | | | ~~93-06-16~~<br>95-02-04 |

## Data sheet status

| Data sheet status | Product status | Definition [1] |
|---|---|---|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
| Preliminary specification | Qualification | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product. |
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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print code Date of release: 05-96

Document order number: 9397-750-03479

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