Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

74LVC241A

FEATURES

- 5-Volt tolerant inputs/outputs, for interfacing with 5-volt logic.
- Supply voltage range of 1.2 to 3.6 V
- In accordance with JEDEC standard no. 8-1A
- CMOS lower power consumption
- Direct interface with TTL levels
- High impedance when V_{CC} = 0 V

DESCRIPTION

The 74LVC241A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. In 3-State operation, outputs can handle 5 V. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC241A is an octal non-inverting buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs $1\overline{OE}$ and 2OE. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times.

QUICK REFERENCE DATA

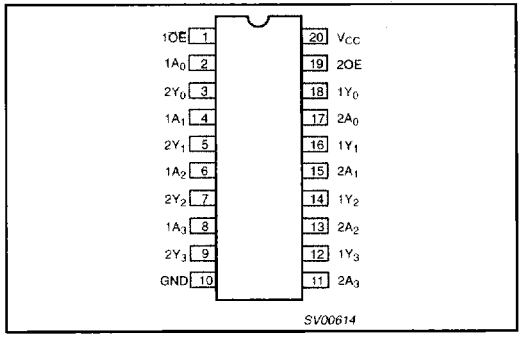
GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 50 pF; V_{CC} = 3.3 V	3.2	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per buffer	V_{CC} = 3.3 V	25	pF

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic SO	–40°C to +85°C	74LVC241A D	74LVC241A D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC241A DB	74LVC241A DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC241A PW	7LVC241APW DH	SOT360-1

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$1\overline{OE}$	Output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	Data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	Bus outputs
10	GND	Ground (0 V)
17, 15, 13, 11	$2A_0$ to $2A_3$	Data inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	Bus outputs
19	2OE	Output enable input (active HIGH)
20	V_{CC}	Positive supply voltage

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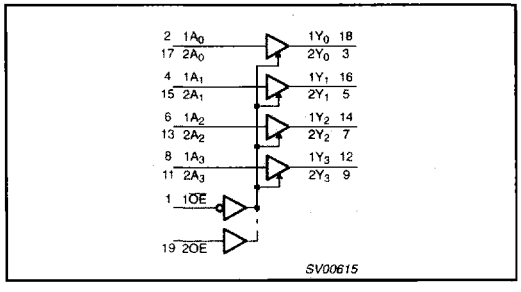
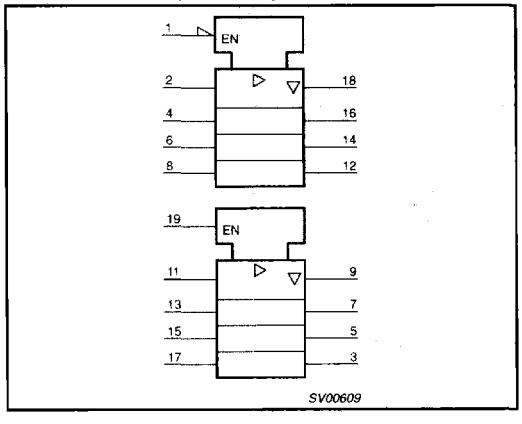
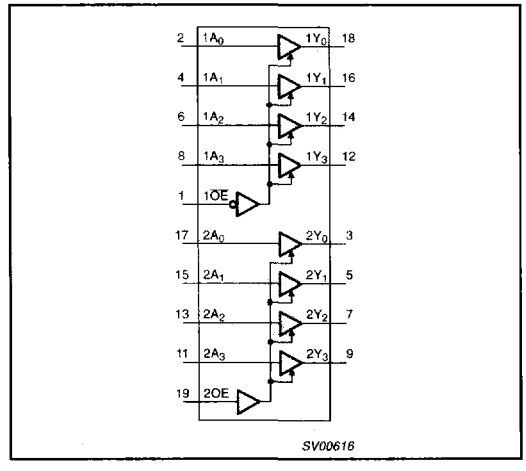
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUT	
$1\overline{OE}$	$1A_n$	2OE	$2A_n$	$1Y_n$	$2Y_n$
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range;output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range;output 3-state		0	5.5	
T_{amb}	Operating ambient temperature range in free-air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	± 50	mA
V_O	DC output voltage;output HIGH or LOW state	Note 2	–0.5 to V_{CC} +0.5	V
	DC output voltage;output 3-state	Note 2	–0.5 to 6.5	
I_O	DC output source or sink current	V_O = 0 to V_{CC}	± 50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		± 100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	*Power dissipation per package* – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = −12mA	V_{CC} − 0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = −100μA	V_{CC} − 0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = −18mA	V_{CC} − 0.6			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = −24mA	V_{CC} − 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100μA			0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	μA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; V_I = V_{IH} or V_{IL}; V_O = 5.5V or GND		0.1	±10	μA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	±10	μA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	10	μA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} −0.6V; I_O = 0		5	500	μA

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; t_r = t_f ≤ 2.5 ns; C_L = 50 pF; R_L = 500Ω; T_{amb} = −40°C to +85°C

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL}/t_{PLH}	Propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	Figures 1, 4	1.5	3.2	6.1	1.5	7.1	11	ns
t_{PZH}/t_{PZL}	3-State output enable time $1\overline{OE}$ to $1Y_n$	Figures 2, 4	1.5	3.8	7.1	1.5	8.1	13	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $1\overline{OE}$ to $1Y_n$	Figures 2, 4	1.5	3.7	6.0	1.5	7.0	8	ns
t_{PZH}/t_{PZL}	3-State output enable time 2OE to $2Y_n$	Figures 3, 4	1.5	3.6	7.1	1.5	8.1	13	ns
t_{PHZ}/t_{PLZ}	3-State output disable time 2OE to $2Y_n$	Figures 3, 4	1.5	3.6	6.0	1.5	7.0	8	ns

NOTE:
1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 × V_{CC} at V_{CC} < 2.7 V
$V_x = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V
$V_x = V_{OL}$ + 0.1 V × V_{CC} at V_{CC} < 2.7 V
$V_Y = V_{OH}$ − 0.3 V at $V_{CC} \geq$ 2.7 V
$V_Y = V_{OH}$ − 0.1 × V_{CC} at V_{CC} < 2.7 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

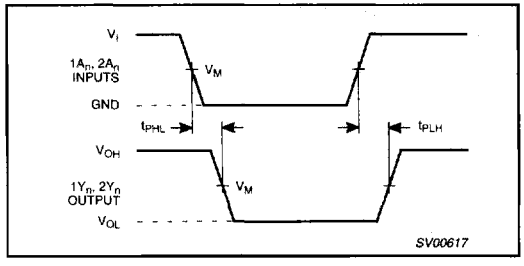


Figure 1. Input ($1A_n$, $2A_n$) to output ($1Y_n$, $2Y_n$) propagation delays.

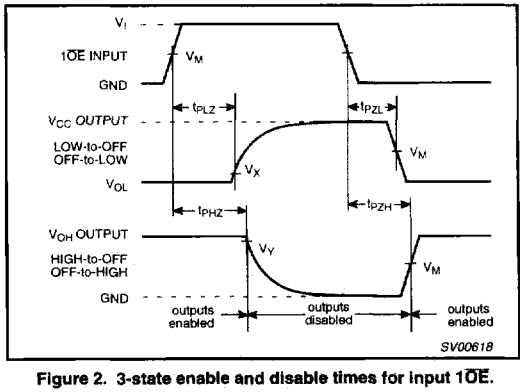


Figure 2. 3-state enable and disable times for input $1\overline{OE}$.

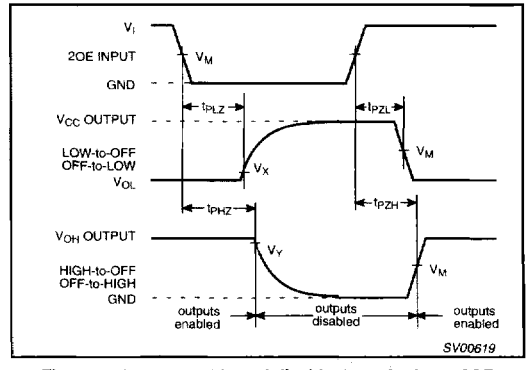
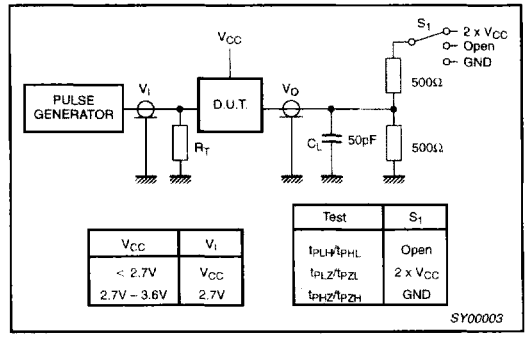


Figure 3. 3-state enable and disable times for input 2OE.

TEST CIRCUIT



V_{CC}	V_I
< 2.7V	V_{CC}
2.7V – 3.6V	2.7V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

Figure 4. Load circuitry for switching times.