T-35-25

TELEDYNE COMPONENTS

SD211A
SD215A

N-CHANNEL ENHANCEMENT-MODE DMOS FET SWITCHES

FEATURES

- **High Input to Output Isolation—120dB typical**
- **Low feedthrough and feedback transients**
- **Low inter-electrode Capacitances**
- **Low Gamma Process**
- **On Resistance Guaranteed in Analog Switch Configuration**

APPLICATIONS

- **+30V Switch Driver—SD211A**
- **±10V Analog Switch—SD215A**
- **±5V Analog Switch—SD211A**

ORDERING INFORMATION

Part No.	Package	Description
SD211ADE	TO-206AF (TO-72) Package	BV_{SD} 10V (min.)
SD211ADE/R	Shorting Rings	BV_{SD} 10V (min.)
SD215ADE	TO-206AF (TO-72) Package	BV_{SD} 20V (min.)
SD215ADE/R	Shorting Rings	BV_{SD} 20V (min.)

ABSOLUTE MAXIMUM RATINGS

Parameter	SD211A	SD215A	Units
V_{DS}	+30	+20	V
V_{SD}	+10	+20	V
V_{DB}	+30	+25	V
V_{SB}	+15	+25	V
V_{GS}	−15	−25	V
	+25	+30	V
V_{GB}	−0.3	−0.3	V
	+25	+30	V
V_{GD}	−30	−25	V
	+25	+30	V

I_D Continuous Drain Current 50mA

P_T Power Dissipation @ or below
T_C = +25°C) 1.2W
Linear Derating Factor ..... 12mW/°C

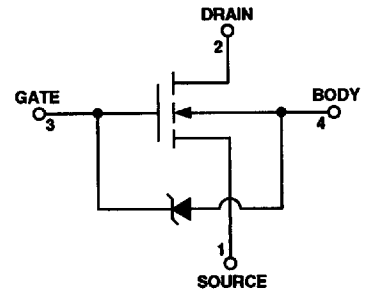
P_D Power Dissipation @ or below
T_A = +25°C 300mW
Linear Derating Factor ..... 3.0mW/°C

T_j Operating Junction Temperature Range ..... −55°C to +125°C

T_s Storage Temperature Range ..... −65°C to +175°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SCHEMATIC DIAGRAM



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N-CHANNEL ENHANCEMENT-MODE DMOS FET SWITCHES

SD211A
SD215A

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ELECTRICAL CHARACTERISTICS: (T_A = +25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	SD211A Min	SD211A Typ	SD211A Max	SD215A Min	SD215A Typ	SD215A Max	Units
Static									
BV_{DS}	Drain-Source Breakdown Voltage	I_D = 10µA, $V_{GS} = V_{BS}$ = 0	30	35	—	—	—	—	V
		ID = 10nA, $V_{GS} = V_{BS}$ = –5V	10	25	—	20	25	—	
BV_{SD}	Source-Drain Breakdown Voltage	I_S = 10nA, $V_{GD} = V_{BD}$ = –5V	10	—	—	20	—	—	V
BV_{DB}	Drain-Substrate Breakdown Voltage	I_D = 10µA, V_{GB} = 0 Source OPEN	15	—	—	25	—	—	V
BV_{SB}	Source-Substrate Breakdown Voltage	I_S = 10µA, V_{GB} = 0 Drain OPEN	15	—	—	25	—	—	V
$I_{D(off)}$	Drain-Source Off Current	V_{DS} = 10V, $V_{GS} = V_{BS}$ = –5V	—	—	10	—	—	—	nA
		V_{DS} = 20V, $V_{GS} = V_{BS}$ = –5V	—	—	—	—	—	10	
$I_{S(off)}$	Source-Drain Off Current	V_{SD} = 10V, $V_{GD} = V_{BD}$ = –5V	—	—	10	—	—	—	nA
		V_{SD} = 20V, $V_{GD} = V_{BD}$ = –5V	—	—	—	—	—	10	
I_{GBS}	Gate-Body Source Leakage Current	V_{GB} = 25V, $V_{DB} = V_{SB}$ = 0	—	—	10	—	—	—	µA
		V_{GB} = 30V, V_{DB}=V_{SB} = 0	—	—	—	—	—	10	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, I_D = 1.0µA, V_{SB} = 0	0.75	1.0	1.5	0.75	1.0	1.5	V
$r_{DS(on)}$	Drain-Source ON Resistance	V_{GS} = 4.5V, I_D = 1mA V_{SB} = 5V	—	—	90	—	—	—	Ω
		V_{GS} = 4.5V, I_D = 1mA V_{SB} = 10V	—	—	—	—	—	90	
		V_{GS} = 10V, I_D = 1mA V_{SB} -=0	—	30	45	—	30	45	
Dynamic									
g_{fs}	Common-Source Forward Transcond.	V_{DS} = 10V, I_D = 20mA f = 1KHz, V_{SB} = 0	10	13	—	10	13	—	mmhos
$C_{(gs+gd+gb)}$	Gate Node Capacitance	V_{DS} = 10V, f = 1MHz $V_{GS} = V_{BS}$ = –15V	—	2.4	3.5	—	2.4	3.5	pF
$C_{(gd+db)}$	Drain Node Capacitance	V_{DS} = 10V, f = 1MHz $V_{GS} = V_{BS}$ = –15V	—	1.3	1.5	—	1.3	1.5	pF
$C_{(gs+sb)}$	Source Node Capacitance	V_{DS} = 10V, f = 1MHz $V_{GS} = V_{BS}$ = –15V	—	3.5	4.0	—	3.5	4.0	pF
C_{dg}	Reverse Transfer Capacitance	V_{DS} = 10V, f = 1MHz $V_{GS} = V_{BS}$ = –15V	—	0.3	0.5	—	0.3	0.5	pF
$T_{D(on)}$	Turn ON Delay Time	V_{DD} = 5V, $V_{G(on)}$ = 10V, R_L = 680Ω, R_G = 51Ω	—	0.7	1.0	—	0.7	1.0	nSec
t_r	Rise Time	V_{DD} = 5V, $V_{G(on)}$ = 10V, R_L = 680Ω, R_G = 51Ω	—	0.8	1.0	—	0.8	1.0	nSec
t_{off}	Turn OFF Time	V_{DD} = 5V, $V_{G(on)}$ = 10V, R_L = 680Ω, R_G = 51Ω	—	10	—	—	10	—	nSec