

# ATT7C108 ATT7C109

# High-Speed CMOS SRAM 1 Mbit (128 Kbit x 8), Common I/O

## Features

- High speed — 15 ns maximum access time
- Automatic powerdown during long cycles
- Easy memory expansion with  $\overline{CE1}$ ,  $\overline{CE2}$ , and  $\overline{OE}$  options
- Advanced CMOS technology
- TTL-compatible inputs and outputs
- Data retention at 2 V for battery backup operation
- Low-power operation
  - Active: 880 mW maximum at 25 ns
  - Standby (typical): 110 mW (TTL inputs); 14 mW (CMOS inputs)
- Package styles available:
  - 32-pin, plastic DIP
  - 32-pin, plastic SOJ

## Description

The ATT7C108 and ATT7C109 devices are high-performance, low-power CMOS static RAMs organized as 131,072 words by 8 bits per word. The eight data-in and data-out signals share I/O pins. The ATT7C108 and 109 differ in that the ATT7C108 has a single chip enable (  $\overline{CE}$  ), while the ATT7C109 has two chip enables (  $\overline{CE1}$  and  $\overline{CE2}$  ). Both devices have an active low output enable (  $\overline{OE}$  ), and are available in three speeds with maximum access times from 15 ns to 25 ns.

Inputs and outputs are TTL compatible. Operation is from a single 5 V power supply. Power

consumption is 880 mW (maximum) at 25 ns. Dissipation drops to 110 mW (typical) for both the ATT7C108 and ATT7C109 when the memory is deselected (enable is high).

Two standby modes are available. Powerdown circuitry reduces power consumption automatically when the memory is deselected, or during read or write cycles that are longer than the access time. In addition, data can be retained in inactive storage with a supply voltage as low as 2 V. The ATT7C108 and ATT7C109 consume only 1.5 mW (typical) at 3 V, allowing effective battery backup operation.

## Pin Information

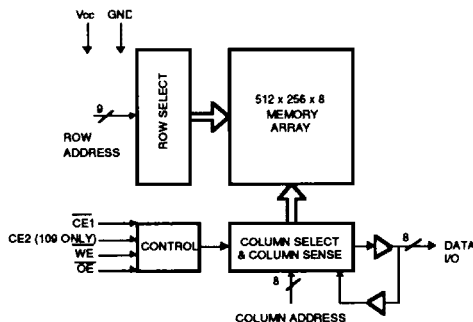


Figure 1. Block Diagram

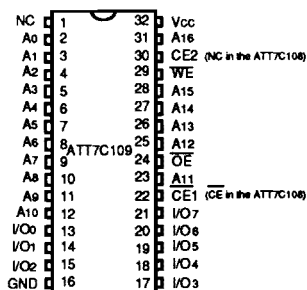


Figure 2. Pin Diagram

Table 1. Pin Descriptions

Pin	Function
A0—A16	Address Inputs
I/O0—I/O7	Data Input/Output
$\overline{CE1}$ , $\overline{CE2}$	Chip Enables
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
GND	Ground
Vcc	+5 V Supply
NC	No Connection

## Functional Description

The ATT7C108 and ATT7C109 devices provide asynchronous (unclocked) operation with matching access and cycle times. One chip enable (active-low) on the ATT7C108 and two chip enables (one active-low and one active-high) on the ATT7C109, plus a 3-state I/O bus with a separate output-enable control, simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A0 through A16. Reading from a designated location is accomplished by presenting an address and driving  $\overline{\text{CE}}1$  and  $\overline{\text{OE}}$  low and CE2 (ATT7C109 only) high while  $\overline{\text{WE}}$  remains high. The data in the addressed memory location then appears on the data I/O pins within one access time.

The eight input/output pins (I/O0 through I/O7) are placed in a high-impedance state when the device is deselected ( $\overline{\text{CE}}1$  high or CE2 low), when the outputs are disabled ( $\overline{\text{OE}}$  high), or during a write operation ( $\overline{\text{CE}}1$  low, CE2 high, and  $\overline{\text{WE}}$  low).

Either one of the CE and  $\overline{\text{WE}}$  signals can be used to terminate a write operation. The data-in and data-out signals have the same polarity.

Latch-up and static discharge protection are provided on-chip. The ATT7C108 and ATT7C109 devices can withstand an injection current of up to 200 mA on any pin without damage.

## Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those indicated in the operational sections of this data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T <sub>stg</sub>	-65	150	°C
Operating Ambient Temperature	T <sub>A</sub>	0	70	°C
Supply Voltage with Respect to Ground	V <sub>CC</sub>	-0.5	7.0	V
Input Signal with Respect to Ground	—	-3.0	7.0	V
Signal Applied to High-impedance Output	—	-3.0	7.0	V
Output Current into Low Outputs	—	—	25	mA
Latch-up Current	—	>200	—	mA

## Truth Table

Table 2. Truth Table for the ATT7C108 and ATT7C109

$\overline{\text{CE}}1$	CE2	$\overline{\text{WE}}$	$\overline{\text{OE}}$	I/O0—I/O7	Mode	Power
H	X	X	X	High Z	Powerdown	Standby (I <sub>CC2</sub> and I <sub>CC3</sub> )
X	L	X	X	High Z	Powerdown	Standby (I <sub>CC2</sub> and I <sub>CC3</sub> )
L	H	H	L	Data Out	Read	Active (I <sub>CC1</sub> )
L	H	L	X	Data In	Write	Active (I <sub>CC1</sub> )
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I <sub>CC1</sub> )

## Handling Precautions

The ATT7C108 and ATT7C109 devices include internal circuitry designed to protect the chips from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use to avoid exposure to excessive electrical stress.

## Recommended Operating Conditions

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0 °C to 70 °C	4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V
Data Retention, Commercial	0 °C to 70 °C	2.0 V ≤ V <sub>CC</sub> ≤ 5.5 V

## Electrical Characteristics

Over all recommended operating conditions.

**Table 3. General Electrical Characteristics**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage:						
High	V <sub>OH</sub>	I <sub>OH</sub> = -4.0 mA, V <sub>CC</sub> = 4.5 V	2.4	—	—	V
Low	V <sub>OL</sub>	I <sub>OL</sub> = 8.0 mA	—	—	0.4	V
Input Voltage:						
High	V <sub>IH</sub>	—	2.2	—	V <sub>CC</sub> + 0.3	V
Low <sup>1</sup>	V <sub>IL</sub>	—	-3.0	—	0.8	V
Input Current	I <sub>IX</sub>	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-10	—	10	μA
Output Leakage Current	I <sub>OZ</sub>	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , CE = V <sub>CC</sub>	-10	—	10	μA
Output Short Current	I <sub>OS</sub>	V <sub>OUT</sub> = GND, V <sub>CC</sub> = Max <sup>2</sup>	—	—	-350	mA
V <sub>CC</sub> Current:						
TTL Inactive <sup>3</sup>	I <sub>CC2</sub>	—	—	20	50	mA
CMOS Standby <sup>4</sup>	I <sub>CC3</sub>	—	—	2.5	30	mA
Data Retention Mode <sup>5</sup>	I <sub>CC4</sub>	V <sub>CC</sub> = 3.0 V	—	5	8	mA
Capacitance (SOJ Package): <sup>6</sup>						
Inputs (A0—A16)	C <sub>I</sub>	Ambient Temp = 25 °C, V <sub>CC</sub> = 5.0 V	—	—	6	pF
Inputs ( $\overline{\text{CE}}1$ , CE2 WE, $\overline{\text{OE}}$ )	C <sub>I</sub>	Test Frequency = 1 MHz <sup>7</sup>	—	—	8	pF
Outputs (I/O0—I/O7)	C <sub>O</sub>		—	—	8	pF

1. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at -0.6 V. A current in excess of 100 mA is required to reach -2 V. The device can withstand indefinite operation with inputs as low as -3 V subject only to power dissipation and bond wire fusing constraints.
2. Duration of the output short circuit should not exceed 30 seconds.
3. Tested with outputs open and all address and data inputs changing at the maximum read cycle. The device is continuously disabled, i.e.,  $\overline{\text{CE}}1 \geq V_{IH}$ , CE2 ≤ V<sub>IL</sub>, max V<sub>CC</sub>.
4. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e.,  $\overline{\text{CE}}1 = V_{CC}$ , CE2 = GND. Input levels are within 0.2 V of V<sub>CC</sub> or ground, max V<sub>CC</sub>.
5. Data retention operation requires that V<sub>CC</sub> never drop below 2.0 V.  $\overline{\text{CE}}1$  must be ≥ V<sub>CC</sub> - 0.2 V. For the ATT7C108 and ATT7C109, all other inputs meet V<sub>IN</sub> ≤ 0.2 V or V<sub>IN</sub> ≥ V<sub>CC</sub> - 0.2 V to ensure full powerdown.
6. Consult AT&T regarding DIP package capacitance.
7. These parameters are not 100% tested.

**Table 4. Electrical Characteristics By Speed**

Parameter	Symbol	Test Condition	Speed			Unit
			25	20	15	
Max V <sub>CC</sub> Current, Active	I <sub>CC1</sub>	*	160	225	270	mA

- \* Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., CE 1 or WE 2 ≤ V<sub>IL</sub>. Input pulse levels are within 0 V to 3 V. Max I<sub>CC</sub> shown applies over the active operating temperature range.

## Timing Characteristics

**Table 5. Read Cycle** <sup>1, 2, 3, 4, 5</sup> (See Figures 3 and 4.)

Over all Recommended Operating Conditions; all measurements in ns.

Symbol	Parameter	Speed					
		25		20		15	
		Min	Max	Min	Max	Min	Max
tADVAX, tCEACEI	Read Cycle Time	25	—	20	—	15	—
tADVDOV	Address Valid to Output Valid <sup>6, 7</sup>	—	25	—	20	—	15
tADVDOX	Address Valid to Output Change	3	—	3	—	3	—
tCEADOV	Chip Enable Active to Output Valid <sup>6, 8</sup>	—	25	—	20	—	15
tCEADOZ	Chip Enable Active to Output Low-Z <sup>9, 10</sup>	3	—	3	—	3	—
tCEIDOZ	Chip Enable Inactive to Data Output High-Z <sup>9, 10</sup>	—	10	—	8	—	8
tOELDOV	Output Enable Low to Data Output Valid	—	12	—	10	—	8
tOELDOZ	Output Enable Low to Low-Z <sup>9, 10</sup>	0	—	0	—	0	—
tOEHDOZ	Output Enable High to Output High-Z <sup>9, 10</sup>	—	10	—	8	—	5
tCEAICH	Chip Enable Active to Powerup <sup>11, 12</sup>	0	—	0	—	0	—
tCHICL	Powerup to Powerdown <sup>11, 12</sup>	—	30	—	25	—	20
tCEIVCL	Chip Enable Inactive to Data Retention <sup>11</sup>	0	—	0	—	0	—
tVCHCEL	End Data Retention to Beginning of Read Cycle <sup>11</sup>	25	—	20	—	15	—

- Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Figure 8), and input pulse levels of 0 to 3.0 V (Figure 9).
- Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, tADVWEH (Table 6) is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.
- All address timings are referenced from the last valid address line to the first transitioning address line.
- CE 1 or CE2 must be inactive or WE must be high during address transitions.
- This product is a very high-speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the Vcc and ground planes directly up to the contactor fingers. A 0.01  $\mu$ F high-frequency capacitor is also required between Vcc and ground. To avoid signal reflections, proper terminations must be used.
- WE is high for the read cycle.
- The chip is continuously selected (CE 1 low and CE2 high).
- All address lines are valid prior to or coincident with the CE 1 and CE2 transition to active.
- At any given temperature and voltage condition, output-disable time is less than output-enable time for any given device.
- Transition is measured  $\pm 200$  mV from steady-state voltage with specified loading in Figure 8. This parameter is sampled and not 100% tested.
- These parameters are not 100% tested.
- Powerup from Icc2 to Icc1 occurs as a result of any of the following conditions: (1) transition of CE 1 and CE2 (ATT7C109 only) to an active state, (2) transition on any address line (CE 1, CE2 active), or (3) transition on any data line (CE 1, CE2 or WE active). The device automatically powers down from Icc2 to Icc1 after tCHICL has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, not on chip-enable pulse width.

## Timing Characteristics (continued)

**Table 6. Write Cycle** <sup>1, 2, 3, 4, 5, 8</sup> (See Figures 6 and 7.)

Over all Recommended Operating Conditions; all measurements in ns.

Symbol	Parameter	Speed					
		25		20		15	
		Min	Max	Min	Max	Min	Max
tADVAX, tCEACEI	Write Cycle Time	20	—	20	—	15	—
tADVCEA	Address Set-up to Write Start	0	—	0	—	0	—
tADVCEI	Address Set-up to End of Write	15	—	15	—	12	—
tCEAWEH, tCEACEI	Chip Enable Active to End of Write	15	—	15	—	12	—
tADVWEX	Address Valid to Beginning of Write	0	—	0	—	0	—
tADVWEH, tADVCEI	Address Valid to End of Write	15	—	15	—	12	—
tWEHADX, tCEIADX	End of Write to Address Change	0	—	0	—	0	—
tWELWEH, tWELCEH	Write Enable Pulse Width	15	—	15	—	12	—
tDIVWEH, tDIVCEI	Data Valid to End of Write	10	—	10	—	7	—
tWEHDIX, tCEIDIX	End of Write to Data Change	0	—	0	—	0	—
tWEHDOZ	Write Enable High to Output Low-Z <sup>6, 7</sup>	0	—	0	—	0	—
tWELDOZ	Write Enable Low to Output High-Z <sup>6, 7</sup>	—	7	—	7	—	5

1. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I<sub>OL</sub> and I<sub>OH</sub> plus 30 pF (see Figure 8), and input pulse levels of 0 V to 3.0 V (see Figure 9).
2. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, tADVWEH is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.
3. All address timings are referenced from the last valid address line to the first transitioning address line.
4.  $\overline{CE} 1$  or  $\overline{CE} 2$  must be inactive or  $\overline{WE}$  must be high during address transitions.
5. This product is a very high-speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V<sub>CC</sub> and ground planes directly up to the contactor fingers. A 0.01 μF high-frequency capacitor is also required between V<sub>CC</sub> and ground. To avoid signal reflections, proper terminations must be used.
6. At any given temperature and voltage condition, output-disable time is less than output-enable time for any given device.
7. Transition is measured ±200 mV from steady state voltage with specified loading in Figure 8. This parameter is sampled and not 100% tested.
8. The internal write cycle of the memory is defined by the overlap of  $\overline{CE} 1$  and  $\overline{CE} 2$  active and  $\overline{WE}$  low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first. If  $\overline{WE}$  goes low before or concurrent with the later of  $\overline{CE} 1$  and  $\overline{CE} 2$  going active, the output remains in a high-impedance state. If  $\overline{CE} 1$  and  $\overline{CE} 2$  go inactive before or concurrent with  $\overline{WE}$  going high, the output remains in a high-impedance state.

Timing Characteristics (continued)

Timing Diagrams

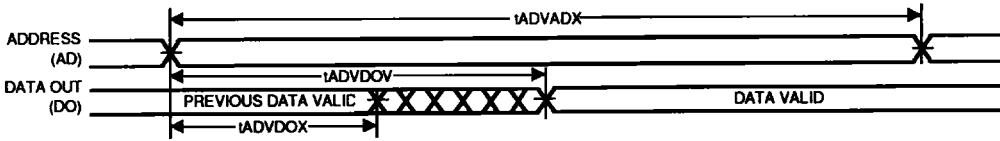


Figure 3. Read Cycle — Address Controlled  
(See Table 4, Notes 6 and 7.)

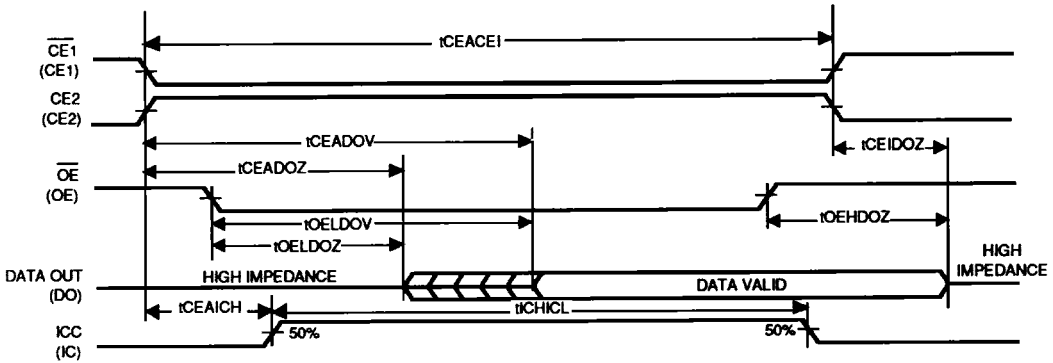


Figure 4. Read Cycle —  $\overline{CE}$  /  $\overline{OE}$  Controlled  
(See Table 4, Notes 6 and 8.)

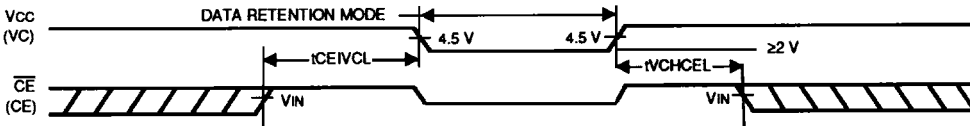


Figure 5. Data Retention

Timing Characteristics (continued)

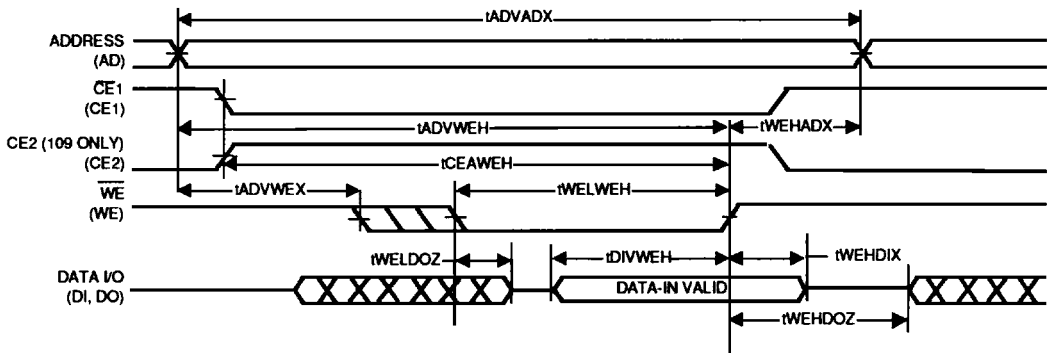


Figure 6. Write Cycle —  $\overline{WE}$  Controlled (  $\overline{OE}$  Low During Write)  
(See Table 5, Note 12; and Table 6.)

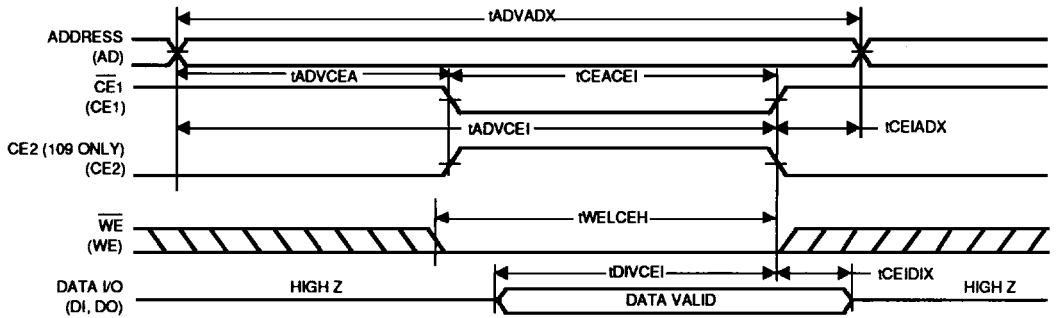
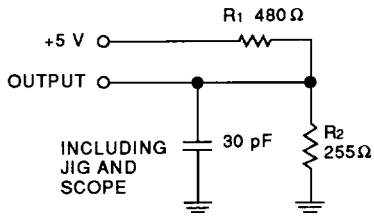
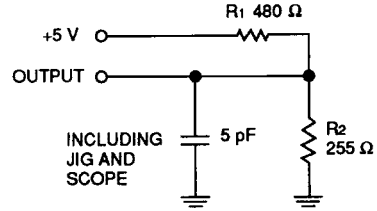


Figure 7. Write Cycle —  $\overline{CE}$  Controlled  
(See Table 5, Note 12; and Table 6.)

Timing Characteristics (continued)



A. Output Loading for loL and loH +30 pF



B. Output Loading for loL and loH +5 pF

Figure 8. Test Loads

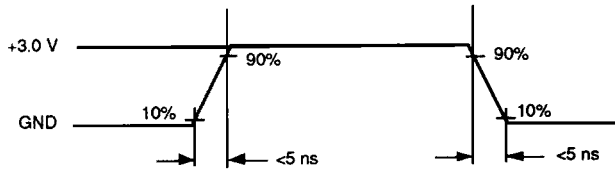
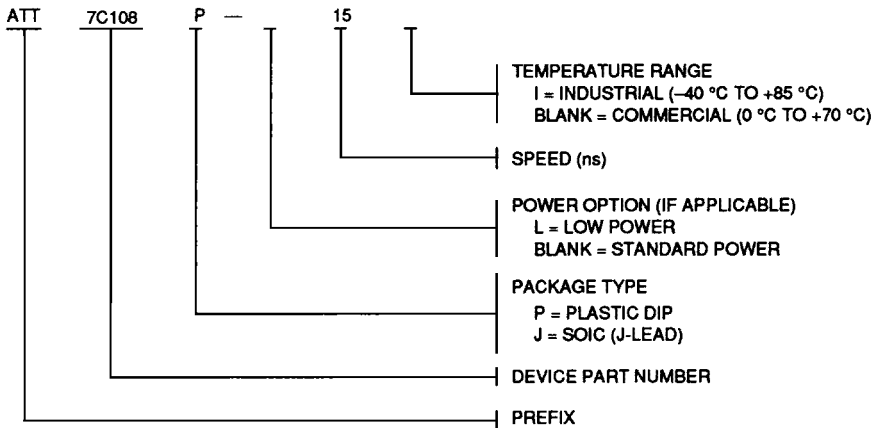


Figure 9. Transition Times



## Ordering Information



### ATT7C108

Operating Range 0 °C to 70 °C

Package Style	Performance Speed		
	25 ns	20 ns	15 ns
32-Pin, Plastic DIP	ATT7C108P-25	ATT7C108P-20	ATT7C108P-15
32-Pin, Plastic SOJ	ATT7C108J-25	ATT7C108J-20	ATT7C108J-15

### ATT7C109

Operating Range 0 °C to 70 °C

Package Style	Performance Speed		
	25 ns	20 ns	15 ns
32-Pin, Plastic DIP	ATT7C109P-25	ATT7C109P-20	ATT7C109P-15
32-Pin, Plastic SOJ	ATT7C109J-25	ATT7C109J-20	ATT7C109J-15