Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 16K (2K x 8-BIT)

IDT7132SA/LA
IDT7142SA/LA

T-46-23-12

FEATURES:

- High-speed access
  - — Military: 25/30/35/45/55/70/90/100/120ns (max.)
  - — Commercial: 20/25/30/35/45/55/70/90/100ns (max.)
- Low-power operation
  - — IDT7132/42SA
    Active: 325mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7132/42LA
    Active: 325mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- MASTER IDT7132 easily expands data bus width to 16-or-more bits using SLAVE IDT7142
- On-chip port arbitration logic (IDT7132 only)
- $\overline{BUSY}$ output flag on IDT7132; $\overline{BUSY}$ input on IDT7142
- Battery backup operation —2V data retention
- TTL-compatible, single 5V ±10% power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD, Class B
- Standard Military Drawing # 5962-87002
- Industrial temperature range (-40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

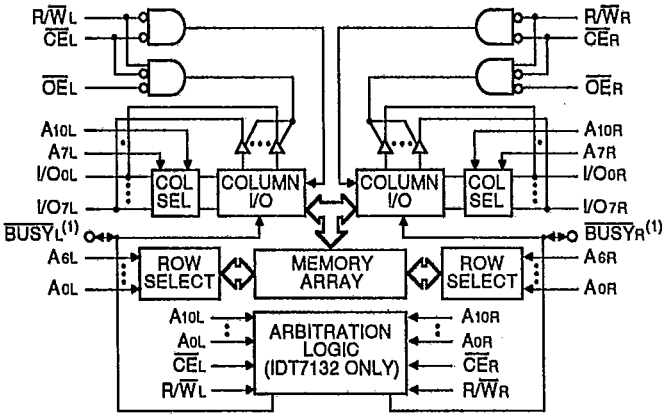
The IDT7132/IDT7142 are high-speed 2K x 8 dual-port static RAMs. The IDT7132 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7142 "SLAVE" dual-port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 325mW of power at maximum access times as fast as 20ns. Low-power (LA) versions offer battery backup data retention capability, with each dual-port typically consuming 200µW from a 2V battery.

The IDT7132/7142 devices are packaged in a 48-pin sidebraze or plastic DIPs, 48- or 52-pin LCCs, 52-pin PLCCs, and a 48-lead flatpacks. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM

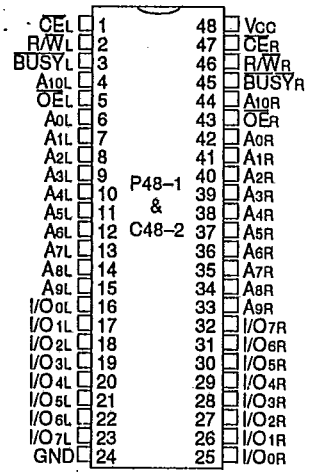


2692 drw 01

NOTE:
1. IDT7132 (MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor.
   IDT7142 (SLAVE): $\overline{BUSY}$ is input.

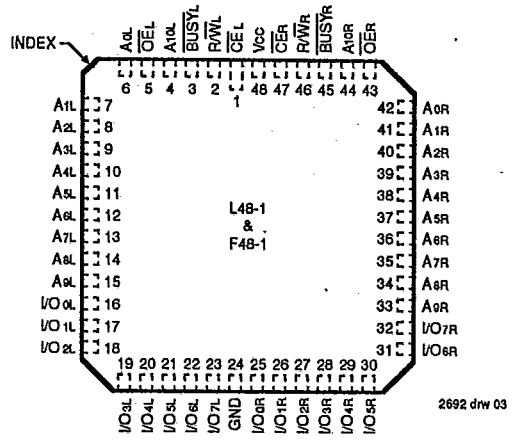
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS

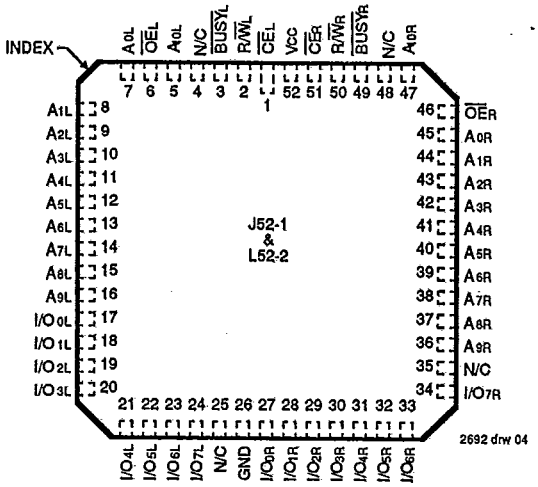


DIP
TOP VIEW

2692 drw 02



48-PIN LCC/FLATPACK
TOP VIEW



52-PIN LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2692 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0(2)	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2692 tbl 02

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2692 tbl 03

T-46-23-12

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ±10%)

Symbol	Parameter	Test Conditions	IDT7132SA IDT7142SA Min.	IDT7132SA IDT7142SA Max.	IDT7132LA IDT7142LA Max.	IDT7132LA IDT7142LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current[9]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O_0-I/O_7)	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2692 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLE VOLTAGE RANGE[1,8] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version	7132 x 20[2,6] 7142 x 20[2,6] Typ.	Max.	7132 x 25[6] 7142 x 25[6] Typ.	Max.	7132 x 30[6] 7142 x 30[6] Typ.	Max.	7132 x 35[7] 7142 x 35[7] Typ.	Max.	7132 x 45 7142 x 45 Typ.	Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	Mil. SA	—	—	125	300	125	295	125	290	75	230	mA
			Mil. LA	—	—	125	240	125	235	125	230	75	185	
			Com'l. SA	125	265	125	260	125	255	75	195	75	190	
			Com'l. LA	125	215	125	210	125	205	75	155	75	145	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE_L}$ and $\overline{CE_R}$ ≥ V_{IH} f = f_{MAX}[4]	Mil. SA	—	—	30	80	30	80	30	80	25	65	mA
			Mil. LA	—	—	30	60	30	60	30	60	25	55	
			Com'l. SA	30	65	30	65	30	65	25	65	25	65	
			Com'l. LA	30	45	30	45	30	45	25	45	25	45	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE_L}$ or $\overline{CE_R}$ ≥ V_{IH} Active Port Outputs Open, f = f_{MAX}[4]	Mil. SA	—	—	80	195	80	190	80	185	40	135	mA
			Mil. LA	—	—	80	160	80	155	80	150	40	110	
			Com'l. SA	80	180	80	175	80	170	40	130	40	120	
			Com'l. LA	80	145	80	140	80	135	40	95	40	85	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs	Both Ports $\overline{CE_L}$ and $\overline{CE_R}$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V, f = 0[5]	Mil. SA	—	—	1.0	30	1.0	30	1.0	30	1.0	30	mA
			Mil. LA	—	—	0.2	10	0.2	10	0.2	10	0.2	10	
			Com'l. SA	1.0	15	1.0	15	1.0	15	1.0	15	1.0	15	
			Com'l. LA	0.2	5	0.2	5	0.2	5	0.2	4	0.2	4	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	One Port $\overline{CE_L}$ or $\overline{CE_R}$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	Mil. SA	—	—	70	185	70	180	70	175	40	125	mA
			Mil. LA	—	—	70	150	70	145	70	140	35	95	
			Com'l. SA	70	175	70	170	70	165	40	115	40	105	
			Com'l. LA	70	140	70	135	70	130	35	90	35	80	

2692 tbl 05

NOTES:
1. x In part numbers indicates power rating (SA or LA).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. At f = f_{Max}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of Input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
6. Not available in DIP packages — see 7032/7042 data sheet.
7. DIP packages for 0°C to +70°C temperature range only — see 7032/7042 data sheet.
8. V_{CC}=5V, T_A=+25°C for Typ.
9. At V_{CC}≤2.0V Input leakages are undefined.

6

T-46-23-12

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (1,8) (Continued) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version	7132 x 55 7142 x 55 Typ.	Max.	7132 x 70 7142 x 70 Typ.	Max.	7132 x90 7142 x 90 Typ.	Max.	7132 x 100 7142 x 100 Typ.	Max.	7132 x 120 (3) 7142 x 120 Typ.	Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}(4)	Mil. SA	65	230	65	225	65	200	65	190	65	190	mA
			Mil. LA	65	185	65	180	65	160	65	155	65	155	
			Com'l. SA	65	180	65	180	65	180	65	180	—	—	
			Com'l. LA	65	140	65	135	65	130	65	130	—	—	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ f = f_{MAX}(4)	Mil. SA	25	65	25	65	25	65	25	65	25	65	mA
			Mil. LA	25	55	25	55	25	45	25	45	25	45	
			Com'l. SA	25	65	25	60	25	55	25	55	—	—	
			Com'l. LA	25	45	25	40	25	35	25	35	—	—	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open, f = f_{MAX}(4)	Mil. SA	40	135	40	135	40	125	40	125	40	125	mA
			Mil. LA	40	110	40	110	40	100	40	100	40	100	
			Com'l. SA	40	115	40	110	40	110	40	110	—	—	
			Com'l. LA	40	85	40	85	40	75	40	75	—	—	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V, f = 0(5)	Mil. SA	1.0	30	1.0	30	1.0	30	1.0	30	1.0	30	mA
			Mil. LA	0.2	10	0.2	10	0.2	10	0.2	10	0.2	10	
			Com'l. SA	1.0	15	1.0	15	1.0	15	1.0	15	—	—	
			Com'l. LA	0.2	4	0.2	4	0.2	4	0.2	4	—	—	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open, f = f_{MAX}(4)	Mil. SA	40	120	40	115	40	110	40	110	40	110	mA
			Mil. LA	35	90	35	85	35	80	35	80	35	80	
			Com'l. SA	40	100	40	100	40	95	40	95	—	—	
			Com'l. LA	35	75	35	75	35	70	35	70	—	—	

2692 tbl 06

NOTES:
1. x in part numbers indicates power rating (SA or LA).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
6. Not available in DIP packages — see 7032/7042 data sheet.
7. DIP packages for 0°C to +70°C temperature range only — see 7032/7042 data sheet.
8. V_{CC}=5V, T_A=+25°C for Typ.

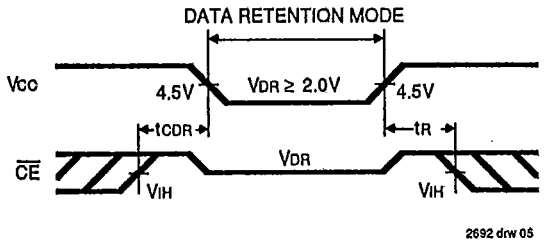
DATA RETENTION CHARACTERISTICS (LA Version Only)

Symbol	Parameter	Test Conditions		IDT7132LA/IDT7142LA Min.	Typ.	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V		2.0	—	0	V
I_{CCDR}	Data Retention Current		Mil.	—	100	4000	µA
			Com'l.	—	100	1500	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	ns

2692 tbl 07

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM



2692 drw 05

AC TEST CONDITIONS

T-46-23-12

Input Pulse Levels	GND TO 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2, & 3

2692 tbl 08

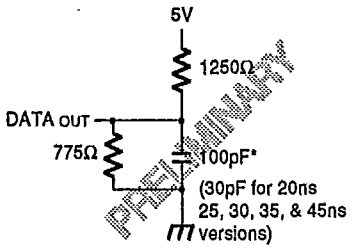


Figure 1. Output Load

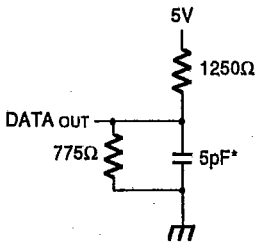


Figure 2. Output Load
(for tHV, tLZ, tWZ, and tOW)

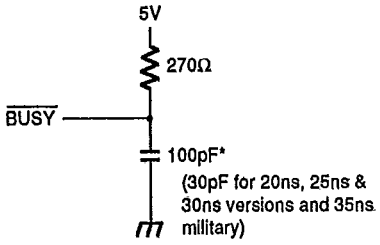


Figure 3. Busy Output Load
(IDT7132 only)

* Including scope and jig

2692 drw 06

6

T-46-23-12

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[5]

Symbol	Parameter	7132 x 20[2,6] 7142 x 20[2,6] Min.	Max.	7132 x 25[6] 7142 x 25[6] Min.	Max.	7132 x 30[6] 7142 x 30[6] Min.	Max.	7132 x 35[7] 7142 x 35[7] Min.	Max.	7132 x 45 7142 x 45 Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tAA	Address Access Time	—	20	—	25	—	30	—	35	—	45	ns
tACE	Chip Enable Access Time	—	20	—	25	—	30	—	35	—	45	ns
tAOE	Output Enable Access Time	—	10	—	12	—	15	—	25	—	30	ns
tOH	Output Hold From Address Change	0	—	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time[1,4]	0	—	0	—	0	—	5	—	5	—	ns
tHZ	Output High Z Time[1,4]	—	8	—	10	—	12	—	15	—	20	ns
tPU	Chip Enable to Power Up Time[4]	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[4]	—	50	—	50	—	50	—	50	—	50	ns

2692 tbl 09

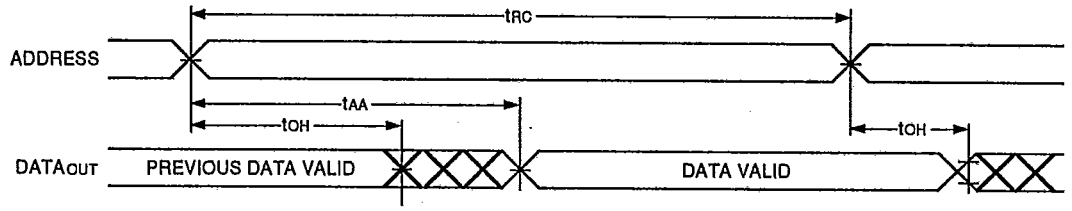
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[5] (Continued)

Symbol	Parameter	7132 x 55 7142 x 55 Min.	Max.	7132 x 70 7142 x 70 Min.	Max.	7132 x 90 7142 x 90 Min.	Max.	7132 x 100 7142 x 100 Min.	Max.	7132 x 120[3] 7142 x 120[3] Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	55	—	70	—	90	—	100	—	120	—	ns
tAA	Address Access Time	—	55	—	70	—	90	—	100	—	120	ns
tACE	Chip Enable Access Time	—	55	—	70	—	90	—	100	—	120	ns
tAOE	Output Enable Access Time	—	35	—	40	—	40	—	40	—	60	ns
tOH	Output Hold From Address Change	0	—	0	—	10	—	10	—	10	—	ns
tLZ	Output Low Z Time[1,4]	5	—	5	—	5	—	5	—	5	—	ns
tHZ	Output High Z Time[1,4]	—	30	—	35	—	40	—	40	—	40	ns
tPU	Chip Enable to Power Up Time[4]	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[4]	—	50	—	50	—	50	—	50	—	50	ns

2692 tbl 10

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. "X" in part numbers indicates power rating (SA or LA).
6. Not available in DIP packages — see 7032/7042 data sheet.
7. DIP packages for 0°C to +70°C temperature range only — see 7032/7042 data sheet.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1,2,4]

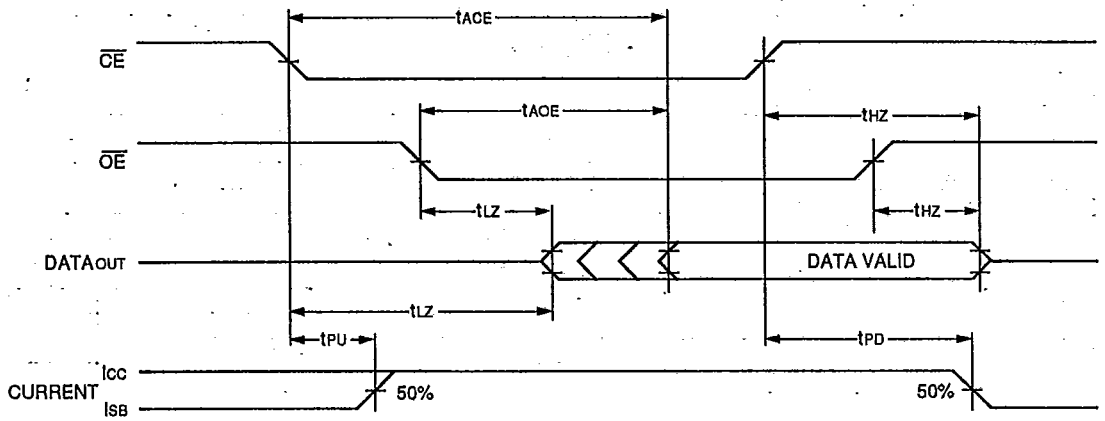


2692 drw 07

NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.

T-46-23-12

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1,3)



2692 drw 08

NOTES:
1. R/W is high for Read Cycles.
2. Device is continuously enabled, CE = VIL.
3. Addresses valid prior to or coincident with CE transition low.
4. OE = VIL.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(7)

Symbol	Parameter	7132 x 20(2,8) 7142 x 20(2,8) Min.	Max.	7132 x 25(8) 7142 x 25(8) Min.	Max.	7132 x 30(8) 7142 x 30(8) Min.	Max.	7132 x 35(9) 7142 x 35(9) Min.	Max.	7132 x 45 7142 x 45 Min.	Max.	Unit
Write Cycle												
tWC	Write Cycle Time(5)	20	—	25	—	30	—	35	—	45	—	ns
tEW	Chip Enable to End of Write	15	—	20	—	25	—	30	—	35	—	ns
tAW	Address Valid to End of Write	15	—	20	—	25	—	30	—	35	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width(6)	15	—	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	10	—	12	—	15	—	20	—	20	—	ns
tHZ	Output High Z Time(1,4)	—	8	—	10	—	12	—	15	—	20	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z(1,4)	—	8	—	10	—	12	—	15	—	20	ns
tOW	Output Active From End of Write(1,4)	0	—	0	—	0	—	0	—	0	—	ns

2692 tbl 11

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2, and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, tWC = tBAA + tWP.
6. Specified for OE at high (Refer to "Timing Waveform of Write Cycle", Note 7)
7. "x" in part numbers indicates power rating (SA or LA).
8. Not available in DIP packages — see 7032/7042 data sheet.
9. DIP packages for 0°C to +70°C temperature range only — see 7032/7042 data sheet.

T-46-23-12

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[7] (Continued)

Symbol	Parameter	7132 x 55 / 7142 x 55 Min.	7132 x 55 / 7142 x 55 Max.	7132 x 70 / 7142 x 70 Min.	7132 x 70 / 7142 x 70 Max.	7132 x 90 / 7142 x 90 Min.	7132 x 90 / 7142 x 90 Max.	7132 x 100 / 7142 x 100 Min.	7132 x 100 / 7142 x 100 Max.	7132 x 120[3] / 7142 x 120[3] Min.	7132 x 120[3] / 7142 x 120[3] Max.	Unit
Write Cycle												
tWC	Write Cycle Time (5)	55	—	70	—	90	—	100	—	120	—	ns
tEW	Chip Enable to End of Write	40	—	50	—	85	—	90	—	100	—	ns
tAW	Address Valid to End of Write	40	—	50	—	85	—	90	—	100	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width (6)	40	—	50	—	55	—	55	—	65	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	20	—	30	—	40	—	40	—	40	—	ns
tHZ	Output High Z Time (1,4)	—	30	—	35	—	40	—	40	—	40	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z(1,4)	—	30	—	35	—	40	—	40	—	50	ns
tOW	Output Active From End of Write(1,4)	0	—	0	—	0	—	0	—	0	—	ns

NOTES: 2692 tbl 12

1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, $t_{WC} = t_{BAA} + t_{WP}$.
6. Specified for $\overline{OE}$ at high (Refer to "Timing Waveform of Write Cycle", Note 7)
7. "x" in part numbers indicates power rating (SA or LA).

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

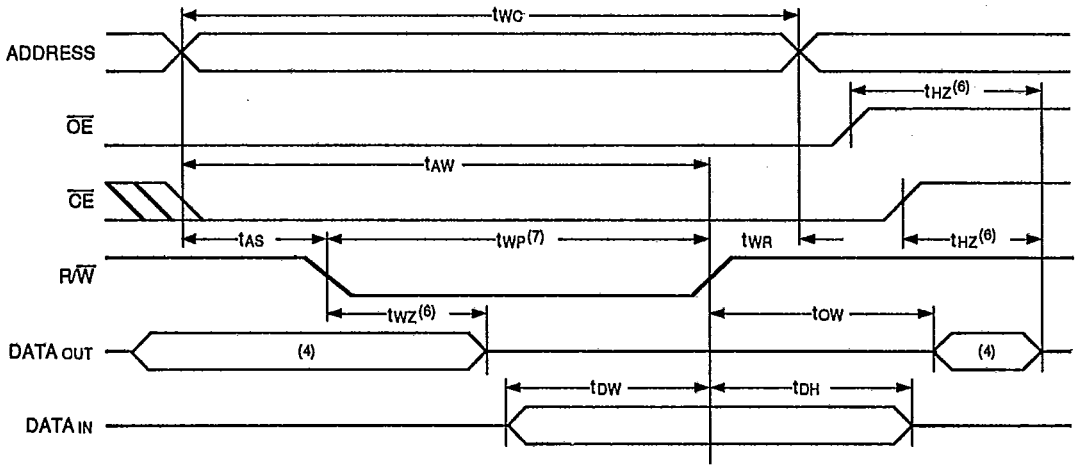
Symbol	Parameter (1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{IN} = 0V	11	pF

NOTE: 2692 tbl 13

1. This parameter is sampled and not 100% tested.

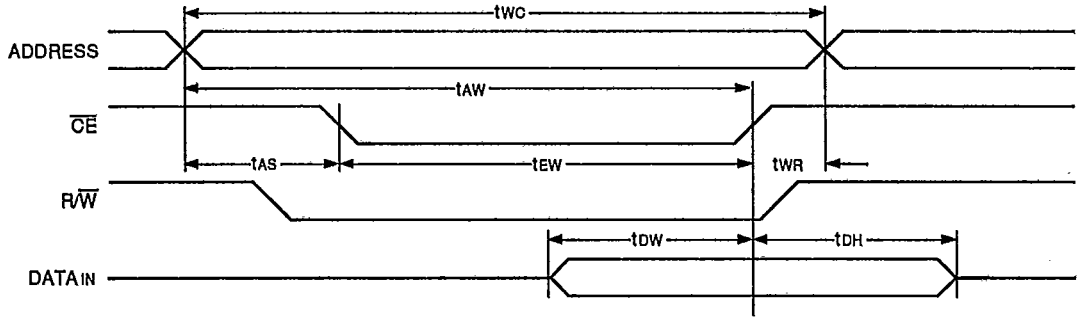
T-46-23-12

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/$\overline{W}$ CONTROLLED TIMING)(1,2,3,7)



2692 drw 09

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING)(1,2,3,5)



2692 drw 10

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

T-46-23-12

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[8]

Symbol	Parameter	7132 x 20 [1,10] 7142 x 20 [1,10] Min.	Max.	7132 x 25 [10] 7142 x 25 [10] Min.	Max.	7132 x 30 [10] 7142 x 30 [10] Min.	Max.	7132 x 35 [11] 7142 x 35 [11] Min.	Max.	7132 x 45 7142 x 45 Min.	Max.	Unit
Busy Timing (For Master IDT7132 Only)												
tBAA	$\overline{BUSY}$ Access Time to Address	—	20	—	25	—	30	—	35	—	35	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	20	—	20	—	25	—	30	—	35	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable	—	20	—	20	—	25	—	30	—	30	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable	—	20	—	20	—	25	—	25	—	25	ns
tWDD	Write Pulse to Data Delay [3]	—	50	—	50	—	50	—	60	—	70	ns
tDDD	Write Data Valid to Read Data Delay [3]	—	35	—	35	—	35	—	35	—	45	ns
tAPS	Arbitration Priority Set-up Time [4]	5	—	5	—	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data [5]	—	Note 5	—	Note 5	—	Note 5	—	Note 5	—	Note 5	ns
Busy Input Timing (For Slave IDT7142 Only)												
tWB	Write to $\overline{BUSY}$ Input [6]	0	—	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$ [7]	12	—	15	—	20	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay [9]	—	50	—	50	—	50	—	60	—	70	ns
tDDD	Write Data Valid to Read Data Delay [9]	—	35	—	35	—	35	—	35	—	45	ns

2692 tbl 14

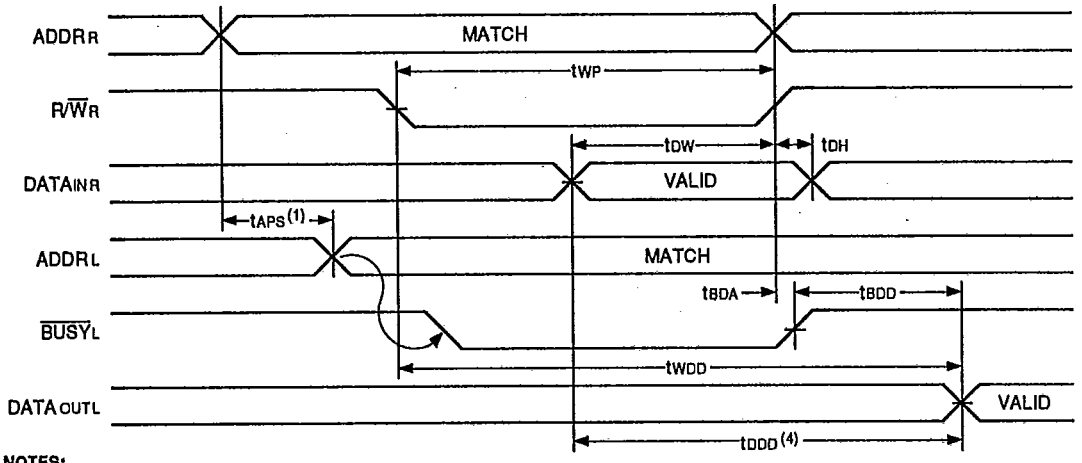
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[8]

Symbol	Parameter	7132 x 55 7142 x 55 Min.	Max.	7132 x 70 7142 x 70 Min.	Max.	7132 x 90 7142 x 90 Min.	Max.	7132 x 100 7142 x 100 Min.	Max.	7132 x 120 [2] 7142 x 120 [2] Min.	Max.	Unit
Busy Timing (For Master IDT7132 Only)												
tBAA	$\overline{BUSY}$ Access Time to Address	—	45	—	45	—	45	—	50	—	60	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	40	—	40	—	45	—	50	—	60	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable	—	35	—	35	—	45	—	50	—	60	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable	—	30	—	30	—	45	—	50	—	60	ns
tWDD	Write Pulse to Data Delay [3]	—	80	—	90	—	100	—	120	—	140	ns
tDDD	Write Data Valid to Read Data Delay [3]	—	55	—	70	—	90	—	100	—	120	ns
tAPS	Arbitration Priority Set-up Time [4]	5	—	5	—	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data [5]	—	Note 5	—	Note 5	—	Note 5	—	Note 5	—	Note 5	ns
Busy Input Timing (For Slave IDT7142 Only)												
tWB	Write to $\overline{BUSY}$ Input [6]	0	—	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$ [7]	20	—	20	—	20	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay [9]	—	80	—	90	—	100	—	120	—	140	ns
tDDD	Write Data Valid to Read Data Delay [9]	—	55	—	70	—	90	—	100	—	120	ns

2692 tbl 15

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (For Master IDT7132 only)".
4. To ensure that the earlier of the two ports wins.
5. tBDD is a calculated parameter and is the greater of 0, tWDD-tWP (actual) or tDDD - tDW (actual)
6. To ensure that the write cycle is inhibited during contention.
7. To ensure that a write cycle is completed after contention.
8. "x" in part numbers indicates power rating (SA or LA).
9. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With Port-to-Port Delay (For Slave IDT7142 Only)".
10. Not available in DIP packages — see 7032/7042 data sheet.
11. DIP packages for 0°C to +70°C temperature range only — see 7032/7042 data sheet.

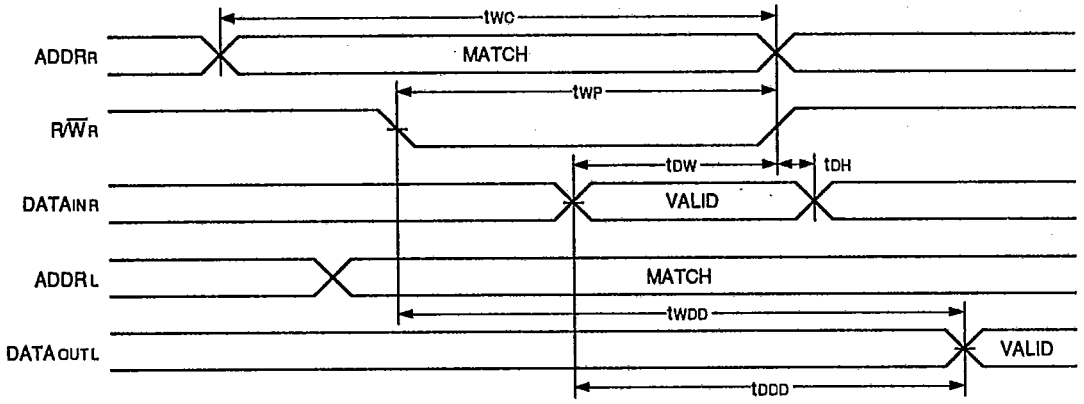
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$ (1,2,3) (FOR MASTER IDT7132 ONLY)



2692 drw 11

NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continously enabled for both ports.
4. $\overline{OE}$ at LO for the reading port.

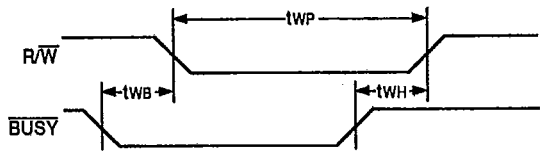
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY (1,2,3) (FOR SLAVE IDT7142 ONLY)



2692 drw 12

NOTES:
1. Assume $\overline{BUSY}$ input at HI for the writing port, and $\overline{OE}$ at LO for the reading port.
2. Write Cycle parameters should be adhered to in order to ensure proper writing.
3. Device is continuously enabled for both ports.

TIMING WAVEFORM OF WRITE WITH BUSY INPUT (FOR SLAVE IDT7142 ONLY)

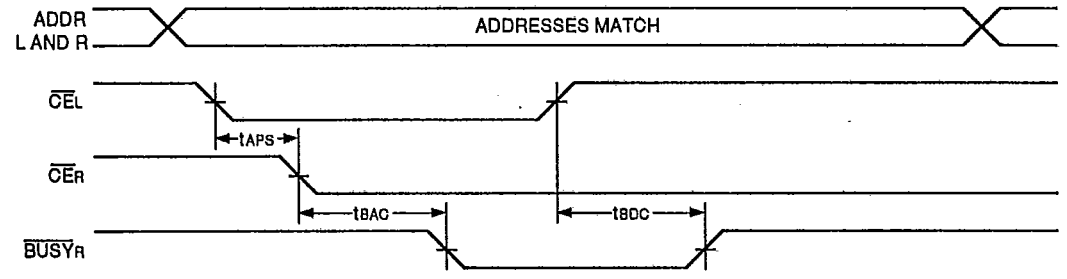


2692 drw 13

T-46-23-12

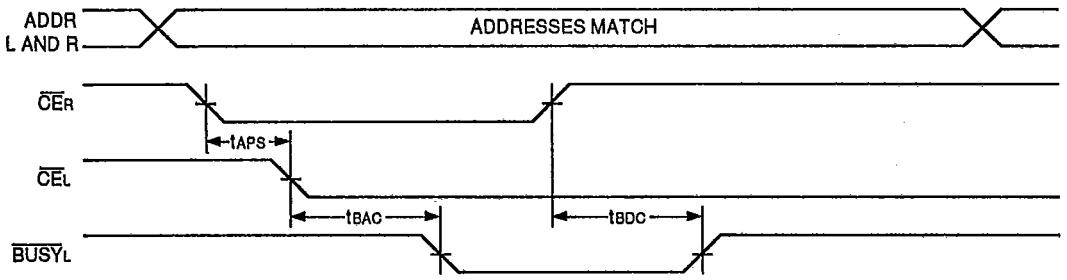
TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION (FOR MASTER IDT7132 ONLY)

$\overline{CE}_L$ VALID FIRST:



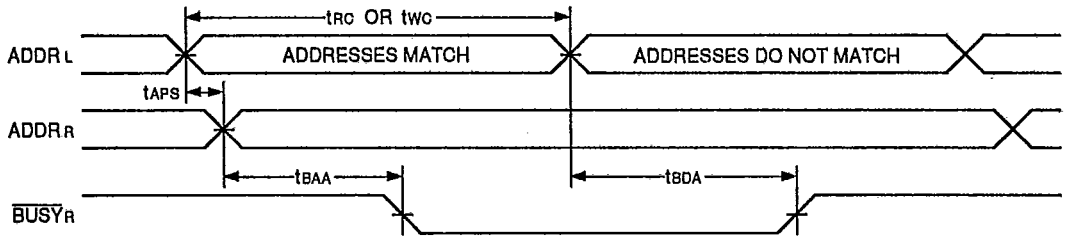
2692 drw 14

$\overline{CE}_R$ VALID FIRST:



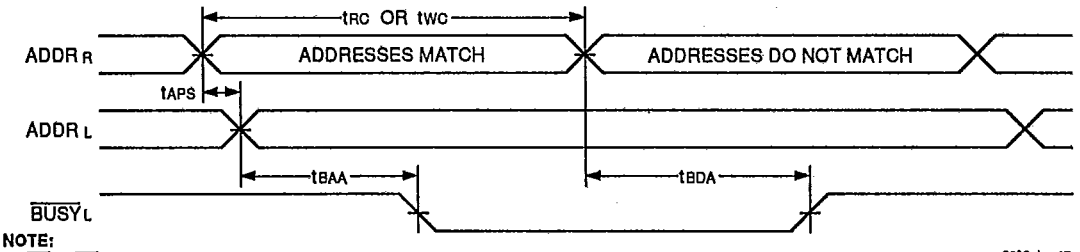
2692 drw 15

TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION(1) (FOR MASTER IDT7132 ONLY)



2692 drw 16

RIGHT ADDRESS VALID FIRST:

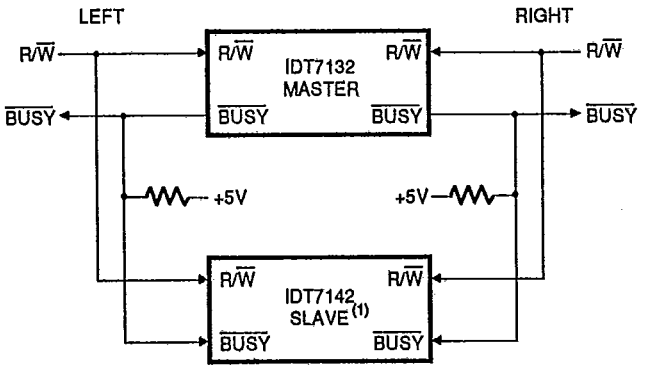


NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$

2692 drw 17

T-46-23-12

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



2692 drw 18

NOTE:
1. No arbitration in IDT7142 (SLAVE). $\overline{BUSY}$-IN inhibits write in IDT7142 (SLAVE).

FUNCTIONAL DESCRIPTION:

The IDT7132/42 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any locations in memory. These devices have an automatic power-down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power-down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table 1.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION:

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address data. It is important to note that the write operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table II). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION:

Expanding the data bus width to sixteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another acitivates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one arbitrator, in the MASTER, is used. The SLAVE has BUSY inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed, until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than on chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

6

TRUTH TABLES

T-46-23-12

TABLE I – NON-CONTENTION READ/WRITE CONTROL(4)

Left Or Right Port (1)				Function
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	
X	H	X	Z	Port Disabled and in Power Down Mode I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	$DATA_{IN}$	Data on Port Written into Memory(2)
H	L	L	$DATA_{OUT}$	Data in Memory Output on Port(3)
H	L	H	Z	High Impedance

2692 tbl 16

NOTES:
1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$
2. If $\overline{BUSY}$ = L, data is not written
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

TABLE II – ARBITRATION(1,2)

Left Port		Right Port		Flags		Function
$\overline{CE}_L$	$A_{0L} - A_{10L}$	$\overline{CE}_R$	$A_{0R} - A_{10R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R} - A_{10R}$	L	$\neq A_{0L} - A_{10L}$	H	H	No Contention
Address Arbitration With $\overline{CE}$ Low Before Address Match						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ Arbitration With Address Match Before $\overline{CE}$						
LL5R	$= A_{0R} - A_{10R}$	LL5R	$= A_{0L} - A_{10L}$	H	L	L-Port Wins
RL5L	$= A_{0R} - A_{10R}$	RL5L	$= A_{0L} - A_{10L}$	L	H	R-Port Wins
LW5R	$= A_{0R} - A_{10R}$	LW5R	$= A_{0L} - A_{10L}$	H	L	Arbitration Resolved
LW5R	$= A_{0R} - A_{10R}$	LW5R	$= A_{0L} - A_{10L}$	L	H	Arbitration Resolved

2692 tbl 17

NOTES:
1. X = DON'T CARE, L = LOW, H = HIGH
2. LV5R = Left Address Valid ≥ 5ns before right address.
   RV5L = Right Address Valid ≥ 5ns before left address.
   Same = Left and Right Addresses match within 5ns of each other.
   LL5R = Left $\overline{CE}$ = LOW ≥ 5ns before Right $\overline{CE}$.
   RL5L = Right $\overline{CE}$ = LOW ≥ 5ns before Left $\overline{CE}$.
   LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other.