PRELIMINARY

32Kx8 Static RAM
CMOS, Monolithic

The EDI8833C/LP/P is a high speed, high performance, low power, 262,144bit CMOS Static RAM organized as 32Kx8.

Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

Two low power versions are available for military applications, LP and P.

The LP version offers battery back-up data retention capability at VDD equal to 2V and operates from a 5V supply.

Military product compliant to MIL-STD-883, paragraph 1.2.1 is available.

Features

32Kx8 bit CMOS Static
Random Access Memory, Monolithic

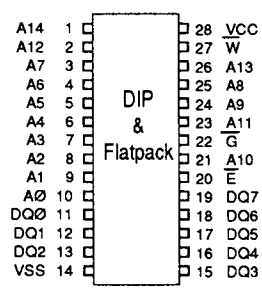
- Access Times 35, 45, and 55
- Data Retention Function (LP)
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

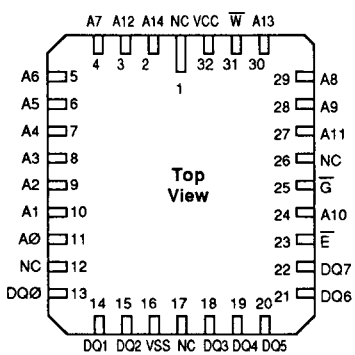
Jedec Approved Pinouts

- 28 Pin Sidebrazed DIP, 600 mils wide (No. 8)
- 32 Pad Leadless Chip Carrier (No. 12)
- 28 Lead Flatpack (No. 79)

Single +5V (±10%) Supply Operation

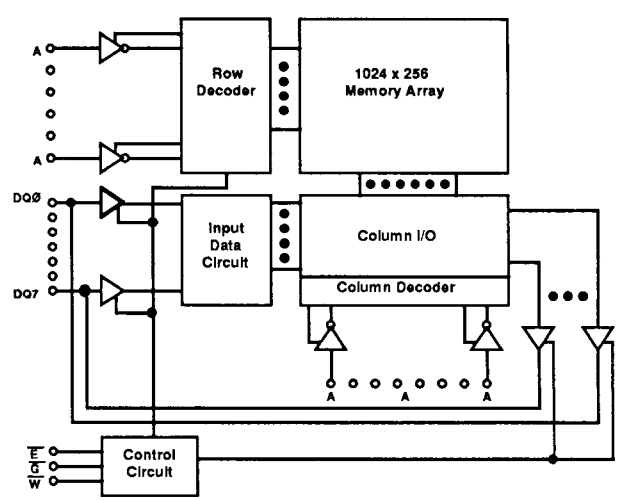
Pin Configuration and Block Diagram





Pin Names

AØ-A14	Address Inputs
E	Chip Enable
W	Write Enable
G	Output Enable
DQØ-DQ7	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection



Absolute Maximum Ratings*

Voltage on any pin relative to VSS ..... -0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial ..... 0°C to +70°C
Industrial ..... -40C to +85°C
Military. ..... -55°C to +125°C
Storage Temperature, Ceramic. ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Output Current. ..... 20 mA
Junction Temperature (TJ) ..... 175°C

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels ..... VSS to 3.0V
Input Rise and Fall Times 5ns
Input and Output Timing Levels 1.5V
Output Load . ..... 1TTL, CL =30pF
(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions		Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{E}$ = VIL, II/O = 0mA, Min Cycle		--		125	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH, VIN ≤ VIL or ≥ VIH		--	--	20	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$≥ VCC-0.2V	C	--	--	3	mA
		VIN ≥VCC-0.2V or VIN≤0.2V	LP/P		--	900	µA
Input Leakage Current	ILI	VIN = 0V to VCC		--	--	±5	µA
Output Leakage Current	ILO	V I/O = 0V to VCC		--	--	±10	µA
Output High Voltage	VOH	IOH= -4.0mA		2.4	--	--	V
Output Low Voltage	VOL	IOL= 8.0mA		--	--	0.4	V

*Typical = TA = 25°C, VCC = 5.0V

Truth Table

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2,1CC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max			Unit
		LCC	FP	DIP	
Input Capacitance (Except DQ Pins)	CI	6	10	10	pF
Capacitance Control (DQ Pins)	CD/Q	8	12	12	pF

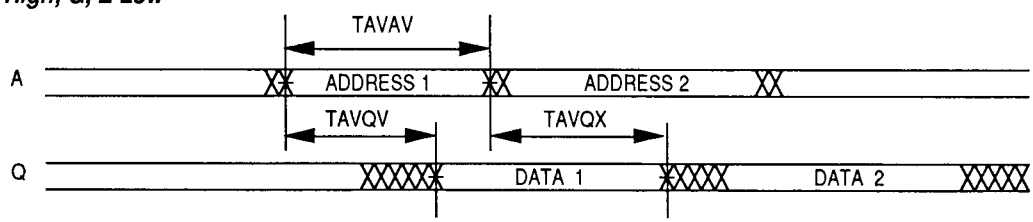
These parameters are sampled, not 100% tested.

AC Characteristics
Read Cycle

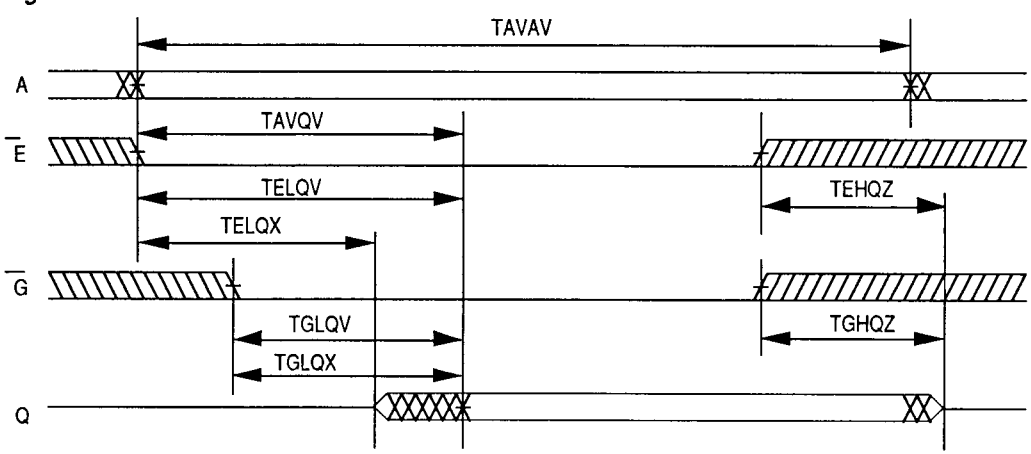
Parameter	Symbol	35ns		45ns		55ns		
		Min	Max	Min	Max	Min	Max	Units
Read Cycle Time	TAVAV	35		45		55		ns
Address Access Time	TAVQV		35		45		55	ns
Chip EnableAccess Time	TELQV		35		45		55	ns
Chip Enable to Output Low Z (1)	TELQX	3		3		3		ns
Output Enable to Output Valid	TGLQV		15		20		25	ns
Output Enable to Output in Low Z (1)	TGLQX	3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ		15		20		25	ns
Output Disable to Output in High Z (1)	TGHQZ		15		20		25	ns
Output Hold from Address Change	TAVQX	3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
$\overline{W}$ High; $\overline{G}$, $\overline{E}$ Low



Read Cycle 2
$\overline{W}$ High

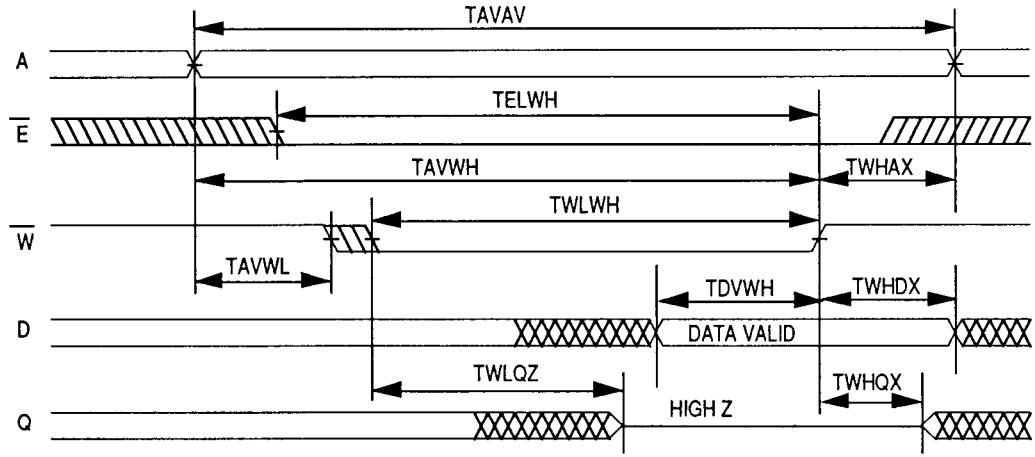


AC Characteristics
Write Cycle

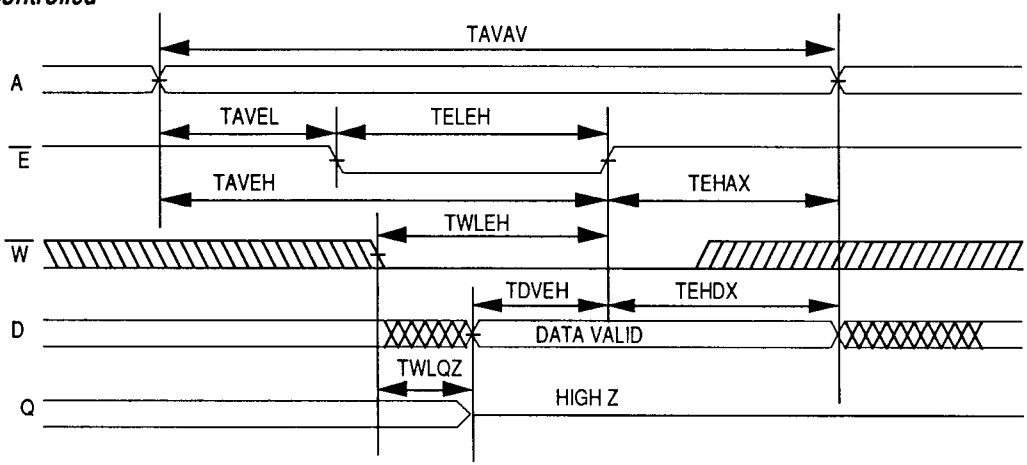
Parameter	Symbol		35ns		45ns		55ns		Units
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		35		45		55		ns
Chip Enable to	TELWH	$\overline{W}$	30		40		50		ns
End of Write	TELEH	$\overline{E}$	30		40		50		ns
Address Setup Time	TAVWL	$\overline{W}$	0		0		0		ns
	TAVEL	$\overline{E}$	0		0		0		ns
Address Valid to	TAVWH	$\overline{W}$	30		40		50		ns
End of Write	TAVEH	$\overline{E}$	30		40		50		ns
Write Pulse Width	TWLWH	$\overline{W}$	25		25		25		ns
	TWLEH	$\overline{E}$	25		25		25		ns
Write Recovery Time	TWHAX	$\overline{W}$	0		0		0		ns
	TEHAX	$\overline{E}$	0		0		0		ns
Data Hold Time	TWHDX	$\overline{W}$	0		0		0		ns
	TEHDX	$\overline{E}$	0		0		0		ns
Write to Output in High Z (1)	TWLQZ			20		20		25	ns
Data to Write Time	TDVWH	$\overline{W}$	15		20		25		ns
	TDVEH	$\overline{E}$	15		20		25		ns
Output Active from End of Write (1)	TWHQX		0		0		0		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled



Characteristic	Sym	Test Conditions	Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 2.0V	2	--	--	V
Data Retention Quiescent Current	ICCDR	$\overline{E}$≥ VDD -0.2V			350	µA
Chip Disable to Data Retention Time	TCDR	VIN ≥VDD -0.2V	0	--	--	ns
Operation Recovery Time	TR	or VIN ≤0.2V	TAVAV*	--	--	ns

*Read Cycle Time

Data Retention $\overline{E}$ Controlled