

74ABT162244 16-Bit Buffer/Line Driver with 25 Ω Series Resistors in the Outputs

General Description

The 'ABT162244 contains sixteen non-inverting buffers with TRI-STATE® outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Individual TRI-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors.

Features

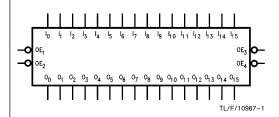
- Separate control logic for each nibble
- 16-bit version of the 'ABT2244
- Guaranteed latch protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability

Commercial	Package Number	Package Description
74ABT162244CSSC (Note 1)	MS48A	48-Lead (0.300" Wide) Molded Shrink Small Outline, JEDEC (SSOP)
74ABT162244CMTD (Notes 1, 2)	MTD48	48-Lead Molded Thin Shrink Small Outline, JEDEC (TSSOP)

Note 1: Devices also available in 13" reel. Use suffix = SSCX and MTDX.

Note 2: Contact factory for package availability.

Logic Symbol



Pin Description

Pin Names	Description	
ŌĒn	Output Enable Input (Active Low)	
l ₀ -l ₁₅	Inputs	
O ₀ -O ₁₅	Outputs	

Connection Diagram

Pin Assignment for SSOP



TL/F/10987-2

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Functional Description

The 'ABT162244 contains sixteen non-inverting buffers with TRI-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but indepen-

dent of the other. The control pins can be shorted together to obtain full 16-bit operation.

I₄-I₇

L

Н

Χ

I₁₂-I₁₅

L

Н

Χ

Inputs

Inputs

 $\overline{\text{OE}}_2$

L

L

Н

 $\overline{\text{OE}}_4$

L

L

Н

Outputs

04-07

L

Н

Z

Outputs

012-015

L

Н Z

Truth Tables

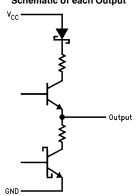
Inp	Outputs		
ŌE ₁	I ₀ -I ₃	O ₀ -O ₃	
L	L	L	
L	Н	Н	
Н	X	Z	

Inp	Inputs		
ŌE ₃	I ₈ -I ₁₁	O ₈ -O ₁₁	
L	L	L	
L	Н	Н	
Н	X	Z	

Z = High Impedance

ı	=	I ow \	/oltane	Level

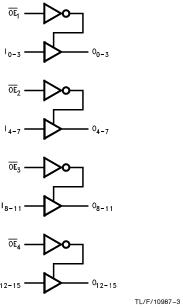
Schematic of each Output



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H = High Voltage Level
L = Low Voltage Level
X = Immaterial

Logic Diagrams



Absolute Maximum Ratings (Note 1)

 $\begin{array}{ll} {\rm Storage\ Temperature} & -65^{\circ}{\rm C\ to}\ +150^{\circ}{\rm C} \\ {\rm Ambient\ Temperature\ under\ Bias} & -55^{\circ}{\rm C\ to}\ +125^{\circ}{\rm C} \end{array}$

Junction Temperature under Bias

Plastic -55°C to +150°C

 $V_{\mbox{\footnotesize CC}}$ Pin Potential to

Ground Pin -0.5V to +7.0V
Input Voltage (Note 2) -0.5V to +7.0V
Input Current (Note 2) -30 mA to +5.0 mA

Voltage Applied to Any Output

in the Disabled or

Power-off State -0.5V to 5.5V in the HIGH State -0.5V to V_{CC}

Current Applied to Output

in LOW State (Max) twice the rated I_{OL} (mA)

DC Latchup Source Current -500 mA
Over Voltage Latchup (I/O) 10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature

Commercial -40°C to +85°C

Supply Voltage

DC Electrical Characteristics

Symbol	Parameter		ABT162244		Units	V _{CC}	Conditions		
Symbol	Faiai	iletei	Min	Тур	Max	Ullits	VCC	Conditions	
V _{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal	
V _{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal	
V _{CD}	Input Clamp Diode Vo	Itage			-1.2	V	Min	$I_{IN} = -18 \text{ mA}$	
V _{OH}	Output HIGH Voltage	74ABT	2.5			V	Min	$I_{OH} = -3 \text{ mA}$	
		74ABT	2.0			V	Min	$I_{OH} = -32 \text{ mA}$	
V _{OL}	Output LOW Voltage	74ABT			0.8	٧	Min	I _{OL} = 12 mA	
I _{IH}	Input HIGH Current				5 5	μΑ	Max	V _{IN} = 2.7V (Note 1) V _{IN} = V _{CC}	
I _{BVI}	Input HIGH Current Breakdown Test				7	μΑ	Max	V _{IN} = 7.0V	
I _{IL}	Input LOW Current				-5 -5	μΑ	Max	$V_{IN} = 0.5V$ (Note 1) $V_{IN} = 0.0V$	
V _{ID}	Input Leakage Test		4.75			٧	0.0	$I_{\text{ID}} = 1.9 \mu\text{A}$ All Other Pins Grounded	
lozh	Output Leakage Curre	nt			50	μΑ	0 - 5.5V	$V_{OUT} = 2.7V; \overline{OE}_n = 2.0V$	
l _{OZL}	Output Leakage Curre	nt			-50	μΑ	0 - 5.5V	$V_{OUT} = 0.5V; \overline{OE}_n = 2.0V$	
los	Output Short-Circuit C	urrent	-100		-275	mA	Max	$V_{OUT} = 0.0V$	
I _{CEX}	Output High Leakage	Current			50	μΑ	Max	$V_{OUT} = V_{CC}$	
I _{ZZ}	Bus Drainage Test				100	μΑ	0.0	V _{OUT} = 5.5V; All Others GND	
I _{CCH}	Power Supply Current				2.0	mA	Max	All Outputs HIGH	
I _{CCL}	Power Supply Current				60	mA	Max	All Outputs LOW	
I _{CCZ}	Power Supply Current				2.0	mA	Max	$\overline{\text{OE}}_{n} = V_{CC}$ All Others at V_{CC} or GND	
Ісст	Additional I _{CC} /Input	Outputs Enabled Outputs TRI-STATE Outputs TRI-STATE			3.0 3.0 50	mA mA μA	Max	$\begin{split} &V_{l}=V_{CC}-2.1V\\ &\text{Enable Input }V_{l}=V_{CC}-2.1V\\ &\text{Data Input }V_{l}=V_{CC}-2.1V\\ &\text{All Others at }V_{CC}\text{ or GND} \end{split}$	
I _{CCD}	Dynamic I _{CC} (Note 1)	No Load			0.1	mA/ MHz	Max	$\label{eq:outputsOpen} \begin{split} & \frac{\text{Outputs Open}}{\text{OE}_n} = & \text{GND} \\ & \text{One Bit Toggling, 50\% Duty Cycle} \end{split}$	

Note 1: Guaranteed, but not tested.

AC Electrical Characteristics

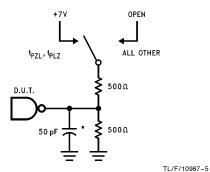
Symbol	Parameter		$74ABT$ $T_A = +25^{\circ}0$ $V_{CC} = +50$ $C_L = 50 \text{ pF}$	<i>l</i>	$74ABT$ $T_A = -40^{\circ}C \text{ to } +85^{\circ}C$ $V_{CC} = 4.5V -5.5V$ $C_L = 50 \text{ pF}$		to +85°C /-5.5V Units	
		Min	Тур	Max	Min	Max		
t _{PLH}	Propagation	1.0	2.4	3.9	1.0	3.9		
t _{PHL}	Delay Data to Outputs	1.0	3.2	4.7	1.0	4.7	ns	
t _{PZH}	Output	1.5	3.5	6.3	1.5	6.3	ns	
t_{PZL}	Enable Time	1.5	4.2	6.9	1.5	6.9	115	
t _{PHZ}	Output	1.0	4.2	6.7	1.0	6.7	ns	
t _{PLZ}	Disable Time	1.0	3.8	6.7	1.0	6.7	113	

Capacitance

Symbol	Parameter	Тур	Units	Conditions, T _A = 25°C	
C _{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0.0V$	
C _{OUT} (Note 1)	Output Capacitance	9.0	pF	V _{CC} = 5.0V	

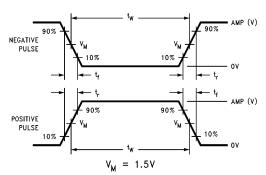
Note 1: C_{OUT} is measured at frequency f=1 MHz per MIL-STD-883B, Method 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load



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FIGURE 2a. Input Pulse Requirements

Amplitude	Rep. Rate	t _w	t _r	t _f	
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns	

FIGURE 2b. Test Input Signal Requirements

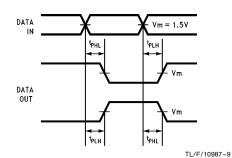


FIGURE 3. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

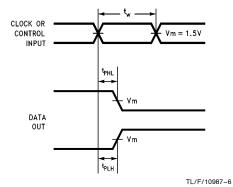


FIGURE 4. Propagation Delay, Pulse Width Waveforms

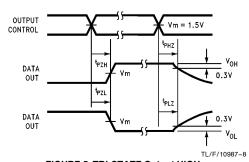


FIGURE 5. TRI-STATE Output HIGH and LOW Enable and Disable Times

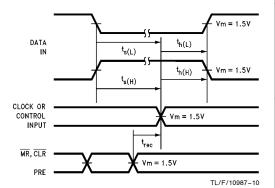
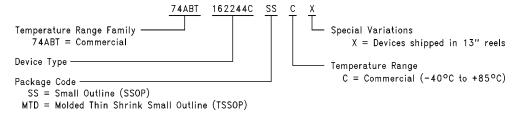


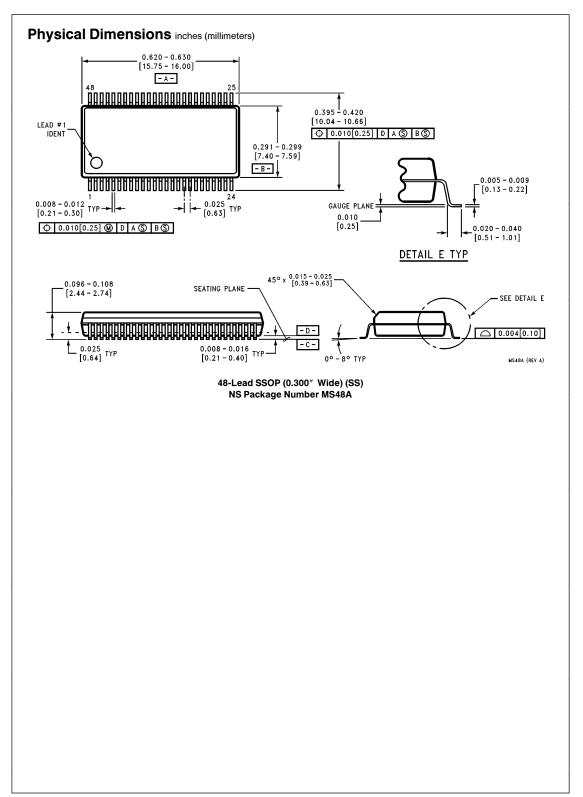
FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



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Physical Dimensions millimeters (Continued) 12.5 ± 0.1 -A-GAGE PLANE 0.25 8.1 6.1 ± 0.1 -B-SEATING PLANE 4.05 $0.60^{\,+0.15}_{\,-0.10}$ DETAIL A △ 0.2 C B A TYPICAL ALL LEAD TIPS -□0.1 C ALL LEAD TIPS SEE DETAIL A (0.90)1.1 -C-0.09-0.20 TYP 0.5 TYP 0.10 ± 0.05 TYP - 0 17 - 0 27 TYP ⊕ 0.13 M A B S C S MTD48 (REV A)

48-Lead Molded Thin Shrink Small Outline Package, JEDEC **NS Package Number MTD48**

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