# HARRIS 82C84A/883

June 1989

## CMOS Clock Generator Driver

### Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Generates the System Clock For CMOS or NMOS Microprocessors
- Up to 25MHz Operation
- Uses a Parallel Mode Crystal Circuit or External Frequency Source
- Provides Ready Synchronization
- Generates System Reset Output From Schmitt Trigger Input
- TTL Compatible Inputs/Outputs
- Very Low Power Consumption
- Single 5V Power Supply
- Military Operating Temperature Range ............ -55°C to +125°C

### Description

The Harris 82C84A/883 is a high performance CMOS Clock Generator-driver which is designed to service the requirements of both CMOS and NMOS microprocessors such as the 80C86, 80C88, 8086 and the 8088. The chip contains a crystal controlled oscillator, a divide-by-three counter and complete "Ready" sychronization and reset logic.

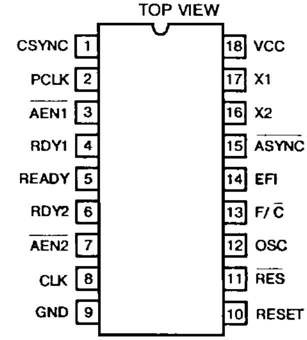
Static CMOS circuit design permits operation with an external frequency source from DC to 25MHz. Crystal controlled operation to 25MHz is guaranteed with the use of a parallel, fundamental mode crystal and two small load capacitors.

All inputs (except X1 and $\overline{RES}$) are TTL compatible over temperature and voltage ranges.

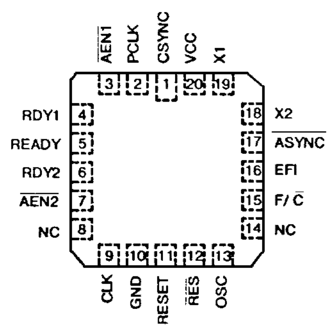
Power consumption is a fraction of that of the equivalent bipolar circuits. This speed-power characteristic of CMOS permits the designer to custom tailor his system design with respect to power and/or speed requirements.

### Pinouts

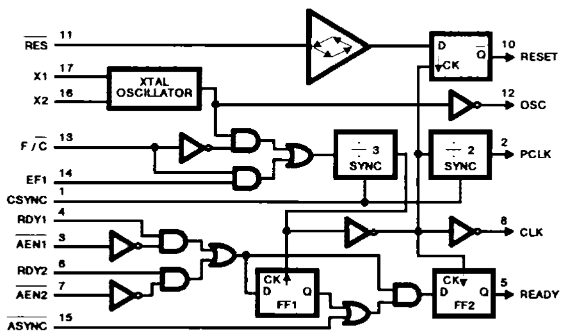
82C84A/883 (CERAMIC DIP)
TOP VIEW




82C84A/883 (CERAMIC LCC)
TOP VIEW




### Functional Diagram




| CONTROL PIN | LOGICAL 1 | LOGICAL 0 |
|---|---|---|
| F/$\overline{C}$ | External Clock | Crystal Drive |
| $\overline{RES}$ | Normal | Reset |
| RDY1<br>RDY2 | Bus Ready | Bus Not Ready |
| $\overline{AEN1}$<br>$\overline{AEN2}$ | Address Disabled | Address Enable |
| $\overline{ASYNC}$ | 1 Stage Ready Synchronization | 2 Stage Ready Synchronization |

## Pin Description

| SYMBOL | DIP PIN NUMBER | TYPE | DESCRIPTION |
|---|---|---|---|
| $\overline{\text{AEN1}}$, $\overline{\text{AEN2}}$ | 3, 7 | I | ADDRESS ENABLE: $\overline{\text{AEN}}$ is an active LOW signal. $\overline{\text{AEN}}$ serves to qualify its respective Bus Ready Signal (RDY1 or RDY2). $\overline{\text{AEN1}}$ validates RDY1 while $\overline{\text{AEN2}}$ validates RDY2 Two $\overline{\text{AEN}}$ signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Busses. In non-Multi-Master configurations, the $\overline{\text{AEN}}$ signal inputs are tied true (LOW). |
| RDY1, RDY2 | 4, 6 | I | BUS READY (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available RDY1 is qualified by $\overline{\text{AEN1}}$ while RDY2 is qualified by $\overline{\text{AEN2}}$. |
| $\overline{\text{ASYNC}}$ | 15 | I | READY SYNCHRONIZATION SELECT: $\overline{\text{ASYNC}}$ is an input which defines the synchronization mode of the READY logic. When $\overline{\text{ASYNC}}$ is low, two stages of READY synchronization are provided. When $\overline{\text{ASYNC}}$ is left open or HIGH a single stage of READY synchronization is provided. |
| READY | 5 | O | READY: READY is an active HIGH signal which is the synchronized RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met. |
| X1, X2 | 17, 16 | I O | CRYSTAL IN: X1 and X2 are the pins to which a crystal is attached. The crystal frequency is 3 times the desired processor clock frequency.* |
| F/$\overline{\text{C}}$ | 13 | I | FREQUENCY/CRYSTAL SELECT: F/$\overline{\text{C}}$ is a strapping option. When strapped LOW. F/$\overline{\text{C}}$ permits the processor's clock to be generated by the crystal. When F/$\overline{\text{C}}$ is strapped HIGH, CLK is generated for the EFI input. |
| EFI | 14 | I | EXTERNAL FREQUENCY IN: When F/$\overline{\text{C}}$ is strapped HIGH, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output. |
| CLK | 8 | O | PROCESSOR CLOCK: CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus. CLK has an output frequency which is 1/3 of the crystal or EFI input frequency and a 1/3 duty cycle. |
| PCLK | 2 | O | PERIPHERAL CLOCK: PCLK is a peripheral clock signal whose output frequency is 1/2 that of CLK and has a 50% duty cycle. |
| OSC | 12 | O | OSCILLATOR OUTPUT: OSC is the output of the internal oscillator circuitry. Its frequency is equal to that of the crystal. |
| $\overline{\text{RES}}$ | 11 | I | RESET IN: $\overline{\text{RES}}$ is an active LOW signal which is used to generate RESET. The 82C84A/883 provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration. |
| RESET | 10 | O | RESET: RESET is an active HIGH signal which is used to reset the 80C86 family processors. Its timing characteristics are determined by $\overline{\text{RES}}$. |
| CSYNC | 1 | I | CLOCK SYNCHRONIZATION: CSYNC is an active HIGH signal which allows multiple 82C84As to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC needs to be externally synchronized to EFI. When using the internal oscillator CSYNC should be hardwired to ground. |
| GND | 9 | | Ground |
| VCC | 18 | | VCC: the +5V power supply pin. A 0.1µF capacitor between VCC and GND is recommended for decoupling. |

* If the crystal inputs are not used X1 must be tied to VCC or GND and X2 should be left open.

## Absolute Maximum Ratings

Supply Voltage .................................... +8.0V
Input, Output or I/O Voltage Applied ..... GND-0.5V to VCC+0.5V
Storage Temperature Range ................. -65°C to +150°C
Junction Temperature ............................... +175°C
Lead Temperature (Soldering 10 sec) .................. +300°C
ESD Classification .................................. Class 1

## Reliability Information

| Thermal Resistance | $\theta_{ja}$ | $\theta_{jc}$ |
|---|---|---|
| Ceramic DIP Package | 86°C/W | 24°C/W |
| Ceramic LCC Package | 73°C/W | 20°C/W |

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package ............................. 580mW
Ceramic LCC Package ............................. 532mW
Gate Count ........................................ 50 Gates

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

## Operating Conditions

Operating Temperature Range ............... -55°C to +125°C
Operating Voltage Range ....................... +4.5V to +5.5V

**TABLE 1. 82C84A/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS**

Device Guaranteed and 100% Tested

| PARAMETER | SYMBOL | CONDITIONS | GROUP A SUBGROUPS | TEMPERATURE | LIMITS | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | | | MIN | MAX | |
| Logical One Input Voltage | VIH | VCC = 5.5V (Notes 1, 2) | 1, 2, 3 | -55°C ≤ $T_A$ ≤ +125°C | 2.2 | - | V |
| Logical Zero Input Voltage | VIL | VCC = 4.5V (Notes 1, 2, 3) | 1, 2, 3 | -55°C ≤ $T_A$ ≤ +125°C | - | 0.8 | V |
| Reset Input High Voltage | VIHR | VCC = 5.5V | 1, 2, 3 | -55°C ≤ $T_A$ ≤ +125°C | VCC-0.8 | - | V |
| Reset Input Low Voltage | VILR | VCC = 4.5V | 1, 2, 3 | -55°C ≤ $T_A$ ≤ +125°C | - | 0.5 | V |
| Reset Input Hysteresis | VT+ VT- | VCC = 5.5V | 1, 2, 3 | -55°C ≤ $T_A$ ≤ +125°C | 0.2VCC | - | V |
| Output High Voltage | VOH | VCC = 4.5V, (Note 4) IOH = -4.0mA for CLK Output, IOH = -2.5mA for all others | 1, 2, 3 | -55°C ≤ $T_A$ ≤ +125°C | VCC-0.4 | - | V |
| Output Low Voltage | VOL | VCC = 4.5V, (Note 4) IOL = +4.0mA for CLK Output, IOL = +2.5mA for all others | 1, 2, 3 | -55°C ≤ $T_A$ ≤ +125°C | - | 0.4 | V |
| Input Leakage Current | II | VCC = 5.5V, VIN = GND or VCC except $\overline{\text{ASYNC}}$, X1 (Note 5) | 1, 2, 3 | -55°C ≤ $T_A$ ≤ +125°C | -1.0 | +1.0 | µA |
| Operating Power Supply Current | ICCOP | VCC = 5.5V, Ouputs Open, Crystal Frequency = 25MHz, (Note 6) | 1, 2, 3 | -55°C ≤ $T_A$ ≤ +125°C | - | 40 | mA |

NOTES:
1. F/$\overline{\text{C}}$ is a strap option and should be held either ≤ 0.8V or ≥ 2.2V. Does not apply to X1 or X2 pins.
2. Due to test equipment limitations related to noise, the actual tested value may differ from that specified, but the specified limit is guaranteed.
3. CSYNC pin is tested with VIL ≤ 0.8V.
4. Interchanging of force and sense conditions is permitted.
5. $\overline{\text{ASYNC}}$ pin includes an internal 17.5kΩ nominal pull-up resistor. For $\overline{\text{ASYNC}}$ input at GND, $\overline{\text{ASYNC}}$ input leakage current = 300µA nominal. X1 - crystal feedback input.
6. f = 25MHz may be tested using the extrapolated value based on measurements taken at f = 2MHz and f = 10MHz.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

**TABLE 2. 82C84A/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS**

Device Guaranteed and 100% Tested

| PARAMETER | SYMBOL | (NOTE 1) CONDITIONS | GROUP A SUBGROUPS | TEMPERATURE | LIMITS MIN | LIMITS MAX | UNITS |
|---|---|---|---|---|---|---|---|
| TIMING REQUIREMENTS | | | | | | | |
| External Frequency High Time | TEHEL(1) | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 13 | - | ns |
| External Frequency Low Time | TELEH(2) | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 13 | - | ns |
| EFI Period | TELEL(3) | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 36 | - | ns |
| RDY1, RDY2 Active Setup to CLK, $\overline{ASYNC}$ = HIGH | TR1VCL(4) | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 35 | - | ns |
| XTAL Frequency | | (Note 2) | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 2.4 | 25 | MHz |
| RDY1, RDY2 Active Setup Time to CLK, $\overline{ASYNC}$ = LOW | TR1VCH(5) | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 35 | - | ns |
| RDY1, RDY2 Inactive Setup Time to CLK | TR1VCH(6) | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 35 | - | ns |
| RDY1, RDY2 Hold to CLK | TCLR1X(7) | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 0 | - | ns |
| $\overline{ASYNC}$ Setup to CLK | TAYVCL(8) | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 50 | - | ns |
| $\overline{ASYNC}$ Hold to CLK | TCLAYX(9) | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 0 | - | ns |
| $\overline{AEN1}$, $\overline{AEN2}$ Setup to RDY1, RDY2 | TA1VR1V(10) | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 15 | - | ns |
| $\overline{AEN1}$, $\overline{AEN2}$ Hold to CLK | TCLA1X(11) | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 0 | - | ns |
| CSYNC Setup to EFI | TYHEH(12) | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 20 | - | ns |
| CSYNC Hold to EFI | TEHYL(13) | | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 20 | - | ns |
| RES Setup to CLK | TI1HCL(15) | (Note 3) | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 65 | - | ns |
| TIMING RESPONSES | | | | | | | |
| RES Hold to CLK | TCLI1H(16) | (Note 3) | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 20 | - | ns |
| CLK Cycle Period | TCLCL(17) | (Note 6) | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | 125 | - | ns |
| CLK High Time | TCHCL(18) | (Note 6) | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | (1/3* TCLCL) +2.0 | - | ns |
| CLK Low Time | TCLCH(19) | (Note 6) | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | (2/3* TCLCL) -15.0 | - | ns |
| CLK Rise or Fall time | TCH1CH2(20) TCL2CL1(21) | From 1.0V to 3.0V | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | - | 10 | ns |
| PCLK High Time | TPHPL(22) | (Note 6) | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | TCLCL -20 | - | ns |
| PCLK Low Time | TPLPH(23) | (Note 6) | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | TCLCL -20 | - | ns |
| Ready Inactive to CLK | TRYLCL(24) | (Note 4) | 9, 10, 11 | $-55^oC \le T_A \le +125^oC$ | -8 | - | ns |
| Ready Active to CLK | TRYHCH(25) | (Note 5) | 9, 10,11 | $-55^oC \le T_A \le +125^oC$ | (2/3* TCLCL) -15.0 | - | ns |

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

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CMOS PERIPHERALS

**TABLE 2. 82C84A/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (CONTINUED)**

Device Guaranteed and 100% Tested

| PARAMETER | SYMBOL | (NOTE 1) CONDITIONS | GROUP A SUBGROUPS | TEMPERATURE | LIMITS MIN | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| TIMINIG RESPONSES (Continued) | | | | | | | |
| CLK to Reset Delay | TCLIL(26) | | 9, 10, 11 | $-55^oC \leq T_A \leq +125^oC$ | - | 40 | ns |
| CLK to PCLK High Delay | TCLPH(27) | | 9, 10, 11 | $-55^oC \leq T_A \leq +125^oC$ | - | 22 | ns |
| CLK to PCLK Low Delay | TCLPL(28) | | 9, 10, 11 | $-55^oC \leq T_A \leq +125^oC$ | - | 22 | ns |
| OSC to CLK High Delay | TOLCH(29) | | 9, 10, 11 | $-55^oC \leq T_A \leq +125^oC$ | - | 22 | ns |
| OSC to CLK Low Delay | TOLCL(30) | | 9, 10, 11 | $-55^oC \leq T_A \leq +125^oC$ | - | 35 | ns |

NOTES:
1. Tested as follows: f = 2.4MHz, VIH = 2.6V, VIL = 0.4V, CL = 50pF, VOH = ≥ 1.5V, VOL ≤ 1.5V, unless otherwise specified. $\overline{RES}$ and F/$\overline{C}$ must switch between 0.4V and VCC-0.4V. Input rise and fall times driven at 1 ns/V. VIL ≤ VIL (max) - 0.4V for CSYNC pin. VCC = 4.5V and 5.5V.
2. Tested using EFI or X1 input pin.
3. Setup and hold necessary only to guarantee recognition at next clock.
4. Applies only to T2 states.
5. Applies only to T3 TW states.
6. Tested with EFI input frequency = 4.2MHz.

**TABLE 3. 82C84A/883 ELECTRICAL PERFORMANCE CHARACTERISTICS**

| PARAMETER | SYMBOL | CONDITIONS | NOTES | TEMPERATURE | LIMITS MIN | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Input Capacitance | CIN | VCC = OPEN, f = 1MHz, All Measurements Referenced to Device GND | 1 | $T_A = +25^oC$ | - | 10 | pF |
| Output Capacitance | COUT | VCC = OPEN, f = 1MHz, All Measurements Referenced to Device GND | 1 | $T_A = +25^oC$ | - | 15 | pF |
| CSYNC Width | TYHYL(14) | | 1, 2 | $-55^oC \leq T_A \leq +125^oC$ | 2* TELEL | - | ns |
| OSC to CLK High Delay | TOLCH(29) | | 1, 2 | $-55^oC \leq T_A \leq +125^oC$ | -5 | - | ns |
| OSC to CLK Low Delay | TOHCL(30) | | 1, 2 | $-55^oC \leq T_A \leq +125^oC$ | 2 | - | ns |

NOTES:
1. The parameters listed in table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. Input test signals must switch between VIL (max) - 0.4V and VIH (min) + 0.4V. $\overline{RES}$ and F/$\overline{C}$ must switch between 0.4V and VCC-0.4V. Input rise and fall times driven at 1 ns/V. VIL ≤ VIL (max) - 0.4 V for CSYNC pin. VCC = 4.5V and 5.5V.

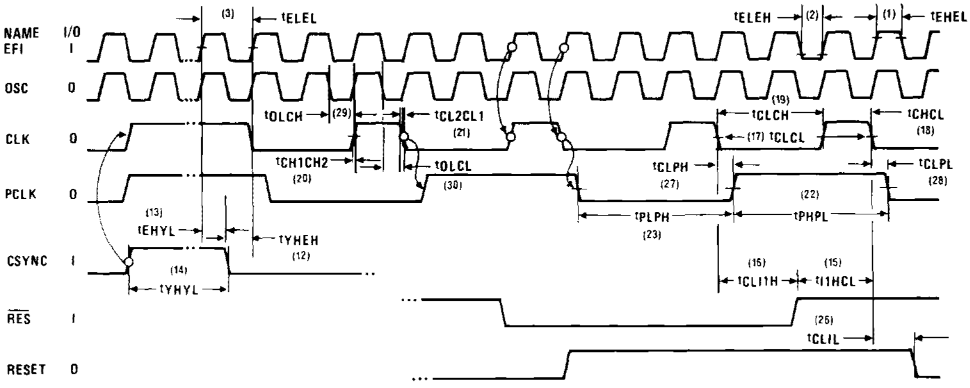
**TABLE 4. APPLICABLE SUBGROUPS**

| CONFORMANCE GROUPS | METHOD | SUBGROUPS |
|---|---|---|
| Initial Test | 100%/5004 | - |
| Interim Test | 100%/5004 | 1, 7, 9 |
| PDA | 100% | 1 |
| Final Test | 100% | 2, 3, 8A, 8B, 10, 11 |
| Group A | - | 1, 2, 3, 7, 8A, 8B, 9, 10, 11 |
| Groups C & D | Samples/5005 | 1, 7, 9 |

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

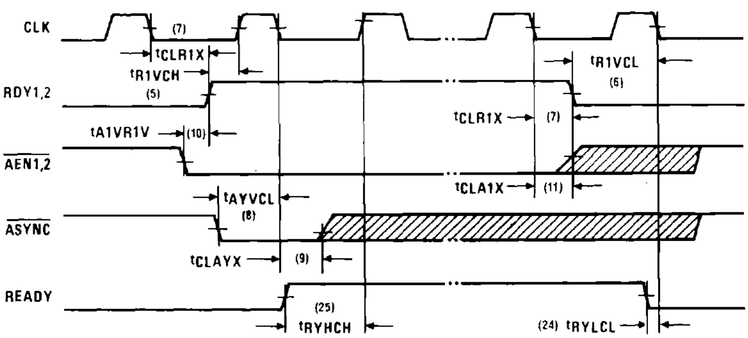
## Timing Waveforms

### WAVEFORMS FOR CLOCKS AND RESET SIGNALS

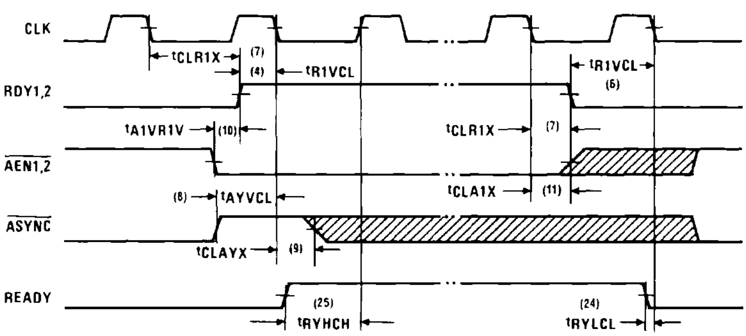



NOTE: All timing measurements are made at 1.5 Volts, unless otherwise noted.

### WAVEFORMS FOR READY SIGNALS (FOR ASYNCHRONOUS DEVICES)




### WAVEFORMS FOR READY SIGNALS (FOR SYNCHRONOUS DEVICES)

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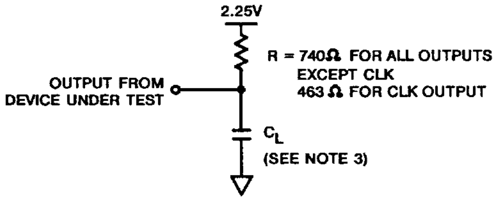
CMOS PERIPHERALS

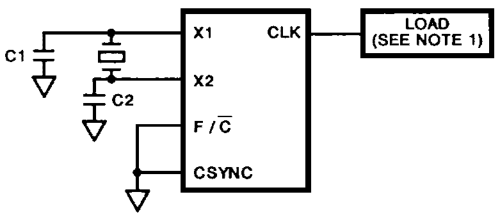
## Test Load Circuits

**TEST LOAD MEASUREMENT CONDITIONS**

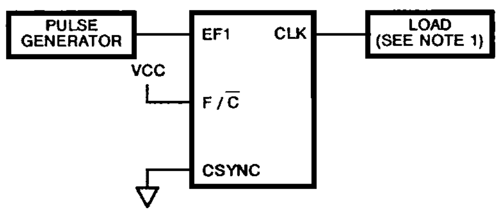



NOTES: 1. $C_L$ =100pF for CLK output
2. $C_L$ = 50pF for all outputs except CLK
3. $C_L$ = Includes probe and jig capacitance

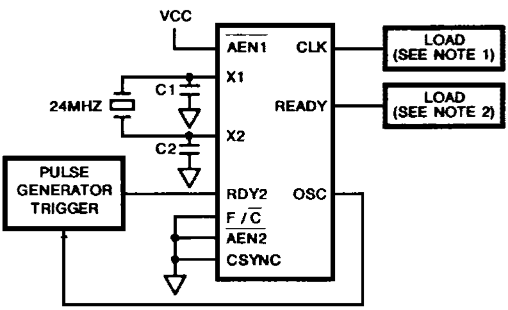
**TCHCL, TCLCH LOAD CIRCUIT**



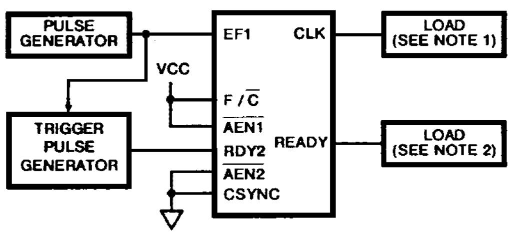

**TCHCL, TCLCH LOAD CIRCUIT**



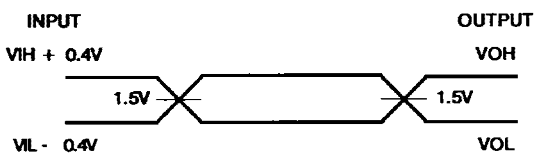

**TRYLCL, TRYHCH LOAD CIRCUIT**




**TRYLCL, TRYHCH LOAD CIRCUIT**



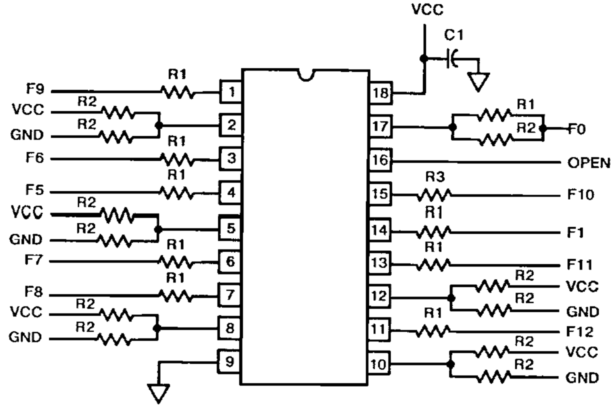

## A.C. Testing Input, Output Waveform



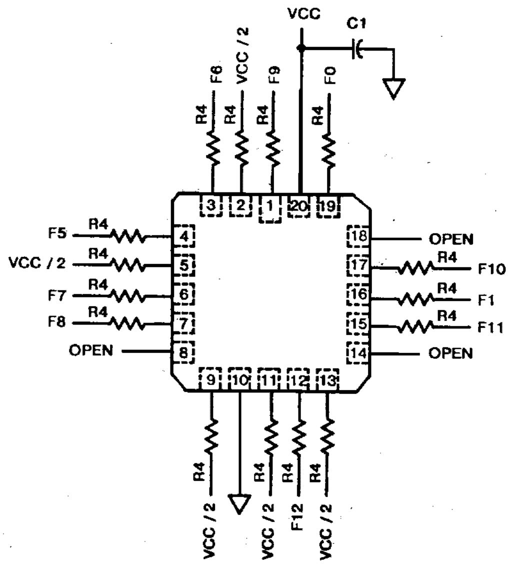

NOTE: Input test signals must switch between VIL (maximum) -0.4V and VIH (minimum) +0.4V. $\overline{RES}$ and F/$\overline{C}$ must switch between 0.4V and VCC -0.4V. Input rise and fall times driven at 1ns/V. VIL ≤ VIL (max) -0.4V for CSYNC pin. VCC -4.5V and 5.5V.

## Burn-In Circuits

82C84A/883 CERAMIC DIP




82C84A/883 CERAMIC LCC




NOTES:

VCC = 5.5V ±0.5V, GND = 0V
VIH =4.5V ±10%
VIL = -0.2 to 0.4V
R1 = 47kΩ, ±5%,
R2 = 10kΩ, ±5%,
R3 = 2.2kΩ, ±5%,
R4 = 1.2kΩ, ±5%,
C1 = 0.01μF (minimum)
F0 = 100kHz ±10%
F1 = F0/2, F2 = F1/2, . . . F12 = F11/2

## Metallization Topology

**DIE DIMENSIONS:**
66.1 x 70.5 x 19 ± 1 mils

**METALLIZATION:**
Type: Silicon - Aluminum
Thickness: 11kÅ ± 1kÅ

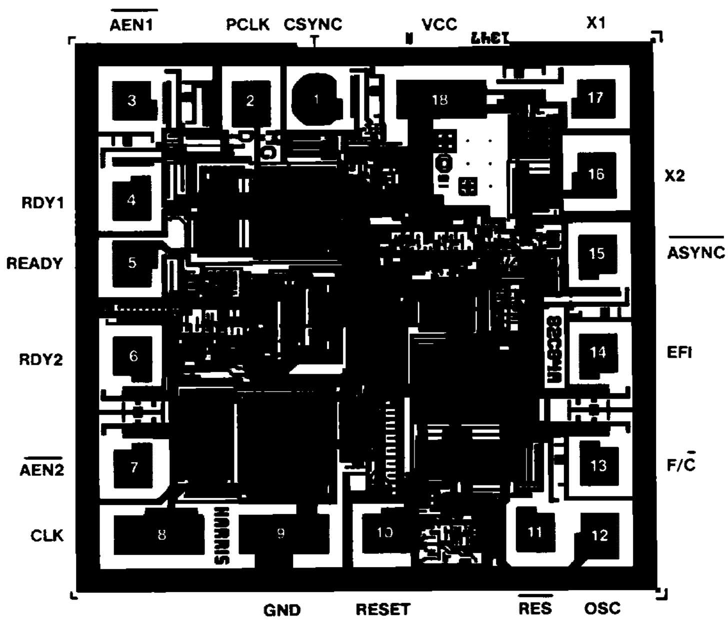
**GLASSIVATION:**
Type: $SiO_2$
Thickness: 8kÅ ± 1kÅ

**DIE ATTACH:**
Material: Gold - Silicon Eutectic Alloy (LCC has Gold Preform)
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

**WORST CASE CURRENT DENSITY:**
$1.42 \times 10^5$ A/cm$^2$

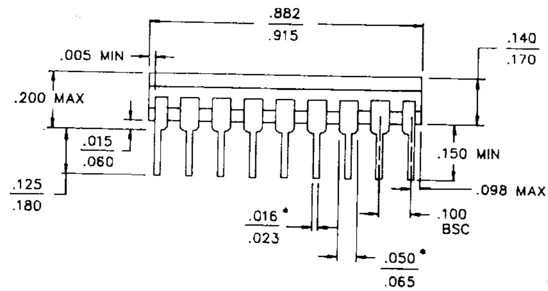
## Metallization Mask Layout

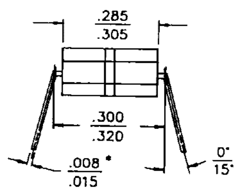
**82C84A/883**



## Packaging†

**18 PIN CERAMIC DIP**



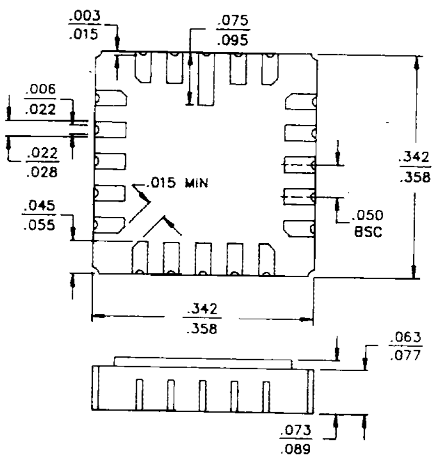




* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

**LEAD MATERIAL:** Type B
**LEAD FINISH:** Type A
**PACKAGE MATERIAL:** Ceramic 90% Alumina
**PACKAGE SEAL:**
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

**INTERNAL LEAD WIRE:**
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
**COMPLIANT OUTLINE:** 38510 D-6

**20 PAD CERAMIC LCC**
BOTTOM VIEW




**PAD MATERIAL:** Type C
**PAD FINISH:** Type A
**FINISH DIMENSION:** Type A
**PACKAGE MATERIAL:** Multilayer Ceramic, 90% Alumina
**PACKAGE SEAL:**
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

**INTERNAL LEAD WIRE:**
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
**COMPLIANT OUTLINE:** 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

*The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.*

## Functional Description

### Oscillator

The oscillator circuit of the 82C84A is designed primarily for use with an external parallel resonant, fundamental mode crystal from which the basic operating frequency is derived.

The crystal frequency should be selected at three times the required CPU clock. X1 and X2 are the two crystal input crystal connections. For the most stable operation of the oscillator (OSC) output circuit, two capacitors (C1 = C2) as shown in the waveform figures are recommended. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

TABLE A. CRYSTAL SPECIFICATIONS

| PARAMETER | TYPICAL CRYSTAL SPEC |
|---|---|
| Frequency | 2.4 - 25MHz, Fundamental, "AT" cut |
| Type of Operation | Parallel |
| Unwanted Modes | -6dB (Minimum) |
| Load Capacitance | 18 - 32pF |

See Harris Publication TB-47 for recommended crystal specifications

Capacitors C1, C2 are chosen such that their combined capacitance

$$CT = \frac{C1 \times C2}{C1 + C2} \text{ (Including stray capacitance)}$$

matches the load capacitance as specified by the crystal manufacturer. This insures operation within the frequency tolerance specified by the crystal manufacturer.

### Clock Generator

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input (CSYNC) allows the output clock to be synchronized with an external event (such as another 82C84A clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the 82C84A. This is accomplished with two flip-flops. (See Figure 1). The counter output is a 33% duty cycle clock at one-third the input frequency.

* The F/$\overline{C}$ input is a strapping pin that selects either the crystal oscillator or the EFI input as the clock for the ÷ 3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source. Output is taken from OSC.

### Clock Oututs

The CLK output is a 33% duty cycle clock driver designed to drive the 80C86, 80C88 processors directly. PCLK is a peripheral clock signal whose output frequency is 1/2 that of CLK. PCLK has a 50% duty cycle.

### Reset Logic

The reset logic provides a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate the reset timing. the reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the 82C84A.

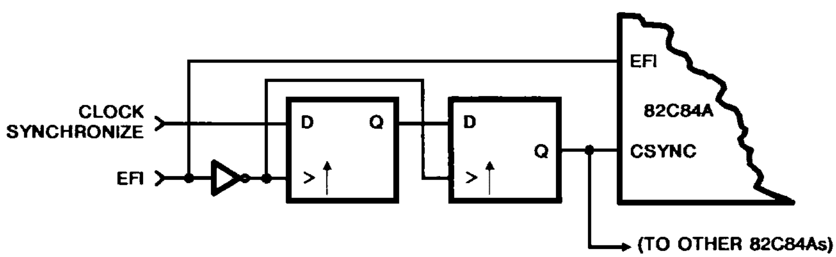



FIGURE 1. CSYNC SYNCHRONIZATION

* NOTE: If EFI input is used, then cyrstal input X1 must be tied to VCC or GND and X2 should be left open. If the cyrstal inputs are used, then EFI should be tied to VCC or GND.

## DESIGN INFORMATION (Continued)

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**READY Synchronization**

Two READY input (RDY1, RDY2) are provided to accommodate two system busses. Each input has a qualifier ($\overline{AEN1}$ and $\overline{AEN2}$, respectively). The $\overline{AEN}$ signals validate their respective RDY signals. If a Multi-Master system is not being used the $\overline{AEN}$ pin should be tied LOW.

Synchronization is required for all asynchronous active-going edges of either RDY input to guarantee that the RDY setup and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

The $\overline{ASYNC}$ input defines two modes of READY synchronization operation.

When $\overline{ASYNC}$ is LOW, two stages of synchronization are provided for active READY input signals. Positive-going asynchronous READY inputs will first be synchronized to flip-flop one a the rising edge of CLK (requiring a setup time tR1VCH) and the synchronized to flip-flop two at the next falling edge of CLK, after which time the READY output will go active (HIGH). Negative-going asynchronous READY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which the READY output will go inactive. This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing, tR1VCL, on each bus cycle.

When $\overline{ASYNC}$ is high or left open, the first READY flip-flop is bypassed in the READY synchronization logic. READY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time.

$\overline{ASYNC}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.