

## Signetics

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FAST Products	

# FAST 74F132 Schmitt Trigger

Quad 2-Input NAND Schmitt Trigger

## DESCRIPTION

The 74F132 contains four 2-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates. Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as three inputs remain at a more positive voltage than  $V_{T+MAX}$ , the gate will respond in the transition of the other input as shown in Waveform 1.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F132	6.3 ns	13 mA

## ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$
14-Pin Plastic DIP	N74F132N
14-Pin Plastic SO	N74F132D

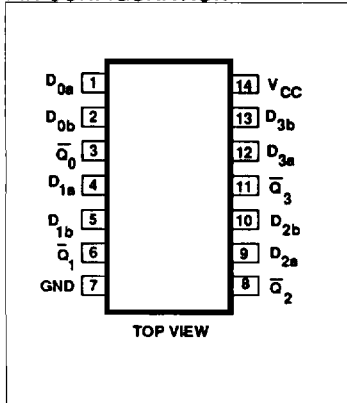
## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_{na}, D_{nb}$	Data inputs	1.0/1.0	20 $\mu$ A/0.6mA
$\bar{Q}_n$	Data output	50/33	1.0mA/20mA

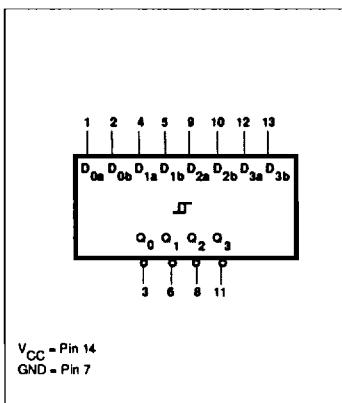
### NOTE:

One (1.0) FAST Unit Load is defined as: 20 $\mu$ A in the High state and 0.6mA in the Low state.

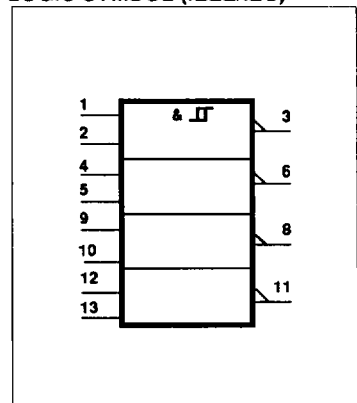
## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



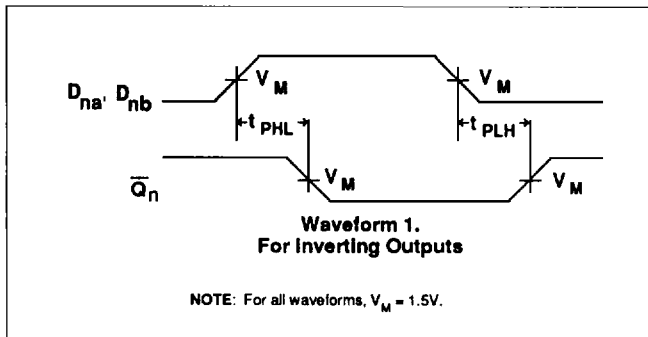
# Schmitt Trigger

FAST 74F132

## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25^\circ\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_{PLH}$ $t_{PHL}$	Propagation delay $D_{na}, D_{nb}$ to $\bar{Q}_n$	Waveform 1	3.5	5.5	7.0	3.0	8.5	ns

## AC WAVEFORMS



## TEST CIRCUIT AND WAVEFORMS

**Test Circuit For Totem-Pole Outputs**

**DEFINITIONS**

$R_L$  = Load resistor; see AC CHARACTERISTICS for value.

$C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

$V_M = 1.5\text{V}$   
**Input Pulse Definition**

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1MHz	500ns	2.5ns	2.5ns