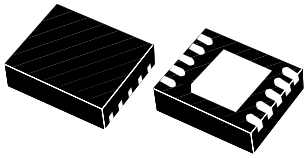
L6728AH

High frequency single phase PWM controller with Power Good

Datasheet - production data



VFDFPN 10

Features

- Flexible power supply from 5 V to 12 V
- Power conversion input as low as 1.5 V
- 0.8 V internal reference
- 0.8% output voltage accuracy
- High-current integrated drivers
- Power Good output
- Sensorless and programmable OCP across low-side $R_{DS(on)}$
- OV / UV protections
- VSEN disconnection protection
- Oscillator internally fixed at 600 kHz
- LS-less to manage pre-bias startup
- Adjustable output voltage
- Disable function
- Internal soft-start
- VFDFPN 10 package

Applications

- Memory and termination supply
- Subsystem power supply (MCH, IOCH, PCI)
- CPU and DSP power supply
- Distributed power supply
- General DC / DC converters

Description

The L6728AH is a single phase step-down controller with integrated high-current drivers, that provides complete control logic and protection to realize in a simple way general DC-DC converters by using a compact VFDFPN 10 package.

Device flexibility allows managing conversions with power input V_{IN} as low as 1.5 V and device supply voltage ranging from 5 V to 12 V.

The L6728AH device provides a simple control loop with the voltage mode EA. The integrated 0.8 V reference allows regulating output voltages with ± 0.8% accuracy over line and temperature variations. The oscillator is internally fixed to 600 kHz.

The L6728AH provides programmable dual level overcurrent protection as well as over and undervoltage protection. Current information is monitored across the low-side MOSFET $R_{DS(on)}$ saving the use of expensive and space-consuming sense resistors.

The PGOOD output easily provides real-time information on output voltage status, through VSEN dedicated output monitor.

Table 1. Device summary

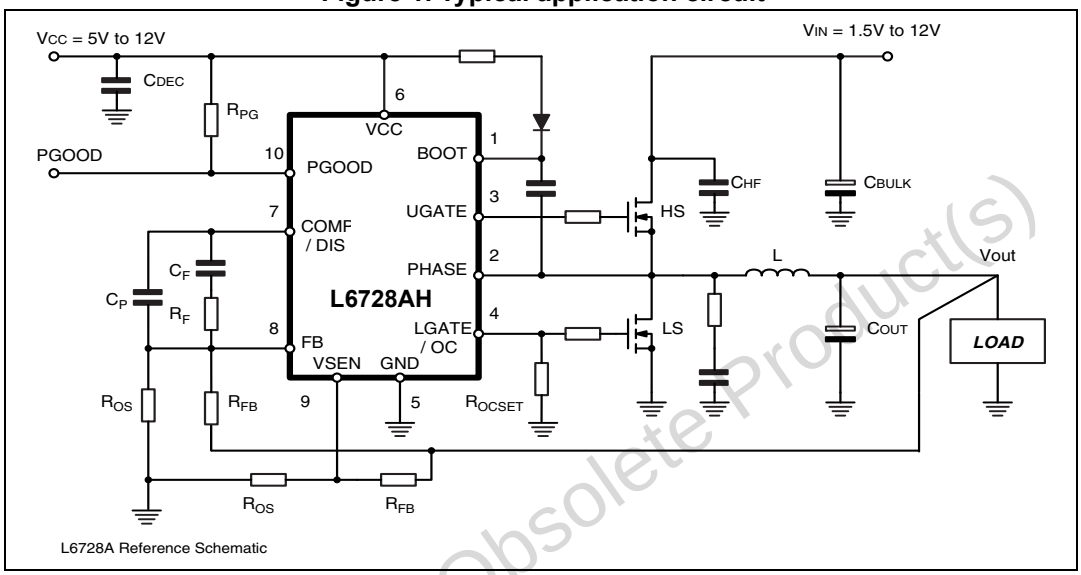
Order codes	Package	Packing
L6728AH	VFDFPN 10	Tube
L6728AHTR		Tape and reel

Contents

1 Typical application circuit and block diagram

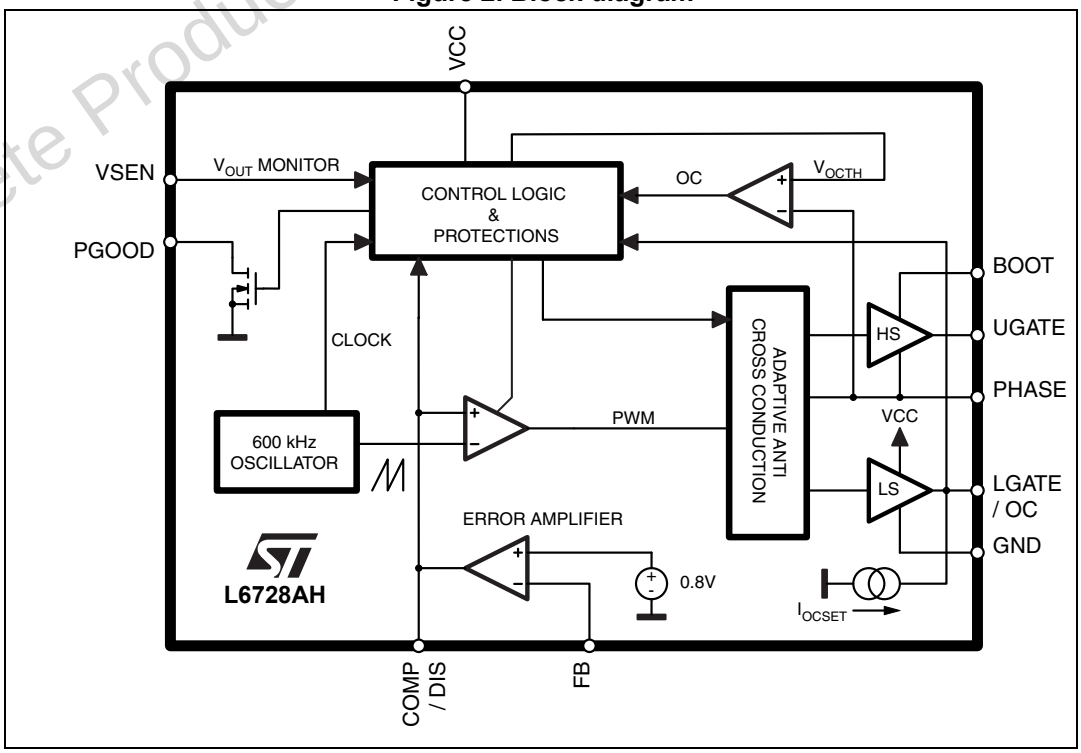
1.1 Application circuit

Figure 1. Typical application circuit



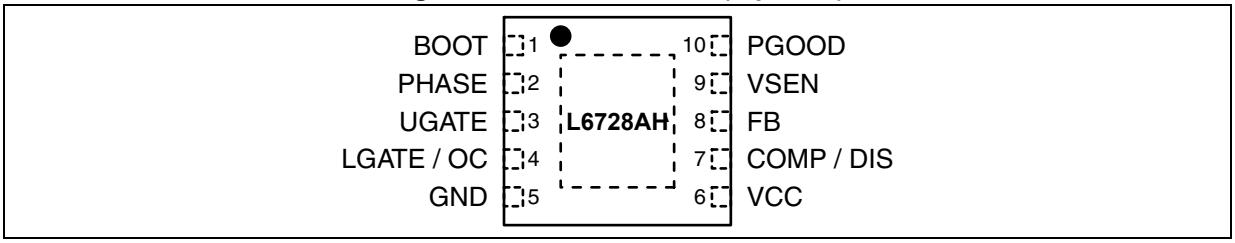
1.2 Block diagram

Figure 2. Block diagram



2 Pins description and connection diagrams

Figure 3. Pins connection (top view)



2.1 Pin descriptions

Table 2.Pin description

Pin #	Name	Function
1	BOOT	HS driver supply. Connect through a capacitor (100 nF) to the floating node (LS-drain) pin and provide a necessary bootstrap diode from V_{CC}.
2	PHASE	HS driver return path, current-reading and adaptive deadtime monitor. Connect to the LS drain to sense $R_{DS(on)}$ drop to measure the output current. This pin is also used by the adaptive deadtime control circuitry to monitor when the HS MOSFET is OFF.
3	UGATE	HS driver output. Connect directly to the HS MOSFET gate.
4	LGATE / OC	*LGATE*. LS driver output. Connect directly to the LS MOSFET gate. *OC* overcurrent threshold set. During a short period of time following V_{CC} rising over the UVLO threshold, a 10 µA current is sourced from this pin. Connect to GND with an R_{OCSET} resistor greater than 5 kΩ to program the OC threshold. The resulting voltage at this pin is sampled and held internally as the OC set point. A maximum programmable OC threshold is 0.55 V. A voltage greater than 0.6 V activates an internal clamp and causes the OC threshold to be set at the maximum value.
5	GND	All internal references, logic and drivers are connected to this pin. Connect to the PCB ground plane.
6	VCC	Device and drivers power supply. Operative range from 5 V to 12 V. Filter with at least 1 µF MLCC to GND.
7	COMP / DIS	*COMP.* Error amplifier output. Connect with an R_F - C_F // C_P to FB to compensate the device control loop. *DIS.* The device can be disabled by pushing this pin lower than 0.75 V (typ.). Setting free the pin, the device enables again.
8	FB	Error amplifier inverting input. Connect with a resistor R_{FB} to the output regulated voltage. Output resistor divider may be used to regulate voltages higher than the reference.
9	VSEN	Regulated voltage sense pin for OVP and UVP protections and PGOOD. Connect to the output regulated voltage, or to the output resistor divider if the regulated voltage is higher than the reference.
10	PGOOD	Open drain output set free after SS has finished and pulled low when VSEN is outside the relative window. Pull up to a voltage equal or lower than V_{CC}. If not used it can be left floating.

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{TH(JA)}$	Thermal resistance junction to ambient (Device soldered on 2s2p, 67 mm x 69 mm board)	45	°C/W
$R_{TH(JC)}$	Thermal resistance junction to case	5	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction temperature range	-40 to 125	°C
P_{TOT}	Maximum power dissipation at T_A = 25 °C	2.25	W

3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	To GND	-0.3 to 15	V
V_{BOOT}, V_{UGATE}	To PHASE to GND to GND; t < 200 ns	15 33 45	V
V_{PHASE}	To GND to GND; t < 200 ns	-5 to 18 -8 to 30	V
V_{LGATE}	To GND	-0.3 to V_{CC}+0.3	V
	FB, COMP, VSEN to GND	-0.3 to 3.6	V
	PGOOD to GND	-0.3 to V_{CC}+0.3	V

3.2 Electrical characteristics

V_{CC} = 5 V to 12 V; T_J = 0 °C to 70 °C, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current and power-on						
I_{CC}	V_{CC} supply current	UGATE and LGATE = OPEN		6		mA
I_{BOOT}	BOOT supply current	UGATE = OPEN; PHASE to GND		0.7		mA
UVLO	V_{CC} turn-ON	V_{CC} rising			4.1	V
	Hysteresis			0.2		V
Oscillator						
F_{SW}	Main oscillator accuracy		540	600	660	kHz
ΔV_{OSC}	PWM ramp amplitude			1.4		V
d_{MAX}	Maximum duty-cycle		67			%
Reference and error amplifier						
	Output voltage accuracy		-0.8	-	0.8	%
A_0	DC gain(1)			120		dB
GBWP	Gain-bandwidth product(1)			15		MHz
SR	Slew-rate(1)			8		V/µs
DIS	Disable threshold	COMP falling	0.70		0.85	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Gate drivers						
I_{UGATE}	HS source current	BOOT - PHASE = 5 V		1.5		A
R_{UGATE}	HS sink resistance	BOOT - PHASE = 5 V		1.1		Ω
I_{LGATE}	LS source current	V_{CC} = 5 V		1.5		A
R_{LGATE}	LS sink resistance	V_{CC} = 5 V		0.65		Ω
Overcurrent protection						
I_{OCSET}	OCSET current source	Sourced from LGATE pin, during OC setting phase	9	10	11	µA
V_{OC_SW}	OC switchover threshold	$V_{LGATE/OC}$ rising		600		mV
Over and undervoltage protections						
OVP	OVP threshold	VSEN rising	0.90	1.00	1.10	V
		unlatch, VSEN falling	0.35	0.40	0.45	V
UVP	UVP threshold	VSEN falling	0.50	0.60	0.70	V
VSEN	VSEN bias current	Sourced from VSEN		100		nA
PGOOD						
PGOOD	Upper threshold	VSEN rising	0.860	0.890	0.920	V
	Lower threshold	VSEN falling	0.680	0.710	0.740	V
V_{PGOODL}	PGOOD voltage low	I_{PGOOD} = -4 mA			0.4	V

1. Guaranteed by design, not subject to test.

4 Device description

The L6728AH is a single phase PWM controller with embedded high-current drivers, that provides complete control logic and protections to realize in an easy and simple way a general DC-DC step-down converter. Designed to drive the N-channel MOSFETs in a synchronous buck topology, with its high level of integration this 10-pin device allows reducing the cost and size of the power supply solution also providing real-time PGOOD in a compact VFDFPN 0 3 x 3 mm package.

The L6728AH device is designed to operate from a 5 V or 12 V supply. The output voltage can be precisely regulated to as low as 0.8 V with ± 1% accuracy over line and temperature variations. The switching frequency is internally set to 600 kHz.

This device provides a simple control loop with a voltage-mode error-amplifier. The error-amplifier features a 15 MHz gain-bandwidth product and an 8 V/µs slew rate, allowing a high regulator bandwidth for fast transient response.

To avoid load damages, the L6728AH provides overcurrent protection as well as overvoltage, under voltage and feedback disconnection protection. The overcurrent trip threshold is programmable by a simple resistor connected from the Lgate to GND. Output current is monitored across the low-side MOSFET $R_{DS(on)}$, saving the use of an expensive and space-consuming sense resistor. Output voltage is monitored through the dedicated VSEN pin.

The L6728AH device implements the soft-start increasing the internal reference in the closed loop regulation. The low-side-less feature allows the device to perform the soft-start over pre-biased output avoiding the high-current return through the output inductor and a dangerous negative spike at the load side.

The L6728AH device is available in a compact VFDFN10 3 x 3 mm package with an exposed pad.

5 Driver section

The integrated high-current drivers allow using different types of the power MOSFET (also multiple MOSFETs to reduce the equivalent $R_{DS(on)}$), maintaining fast switching transition.

The driver for the high-side MOSFET uses the BOOT pin for the supply and the PHASE pin for the return. The driver for the low-side MOSFET uses the V_{CC} pin for the supply and the GND pin for the return.

The controller embodies an anti-shoot-through and adaptive deadtime control to minimize low-side body diode conduction time, maintaining good efficiency while saving the use of the Schottky diode:

- To check the high-side MOSFET turn-off, the PHASE pin is sensed. When the voltage at the PHASE pin drops down, the low-side MOSFET gate drive is suddenly applied.
- To check the low-side MOSFET turn off, the LGATE pin is sensed. When the voltage at the LGATE has fallen, the high-side MOSFET gate drive is suddenly applied.

If the current flowing in the inductor is negative, voltage on the PHASE pin will never drop. To allow the low-side MOSFET to turn-on even in this case, a watchdog controller is enabled: if the source of the high-side MOSFET doesn't drop, the low-side MOSFET is switched on so allowing the negative current of the inductor to recirculate. This mechanism allows the system to regulate even if the current is negative.

Power conversion input is flexible: a 5 V, 12 V bus or any bus that allows the conversion (see maximum duty-cycle limitations in *Table 5 on page 7*) can be chosen freely.

Power dissipation

The L6728AH embeds high-current MOSFET drivers for both high-side and low-side MOSFETs: it is then important to consider the power that the device is going to dissipate in driving them in order to avoid overcoming the maximum junction operative temperature.

Two main terms contribute in the device power dissipation: bias power and drivers' power.

- Device bias power (P_{DC}) depends on the static consumption of the device through the supply pins and it is simply quantifiable as follow (assuming to supply HS and LS drivers with the same V_{CC} of the device):

Equation 1

$$P_{DC} = V_{CC} \cdot (I_{CC} + I_{BOOT})$$

- Drivers power is the power needed by the driver to continuously switch on and off the external MOSFETs; it is a function of the switching frequency and total gate charge of the selected MOSFETs. It can be quantified considering that the total power P_{SW} dissipated to switch the MOSFETs (easy calculable) is dissipated by three main factors: external gate resistance (when present), intrinsic MOSFET resistance and intrinsic driver resistance. This last term is the important one to be determined to calculate the device power dissipation. The total power dissipated to switch the MOSFETs results:

Equation 2

$$P_{SW} = F_{SW} \cdot (Q_{gHS} \cdot V_{BOOT} + Q_{gLS} \cdot V_{CC})$$

External gate resistors helps the device to dissipate the switching power since the same power P_{SW} will be shared between the internal driver impedance and the external resistor resulting in a general cooling of the device.

6 Soft-start

The L6728AH implements a soft-start to smoothly charge the output filter avoiding high inrush currents to be required from the input power supply. The device gradually increases the internal reference from 0 V to 0.8 V in 4.5 msec (typ.), in the closed loop regulation, linearly charging the output capacitors to the final regulation voltage. A pre-charged output voltage will affect the soft-start duration, resulting in a reduction of this period of time (< 4 msec).

During the soft-start process all the protections but the UVP are active: the UVP becomes active as soon as the soft-start ends up.

The device begins the soft-start phase only when the V_{CC} power supply is above the UVLO threshold and the overcurrent threshold setting phase has been completed.

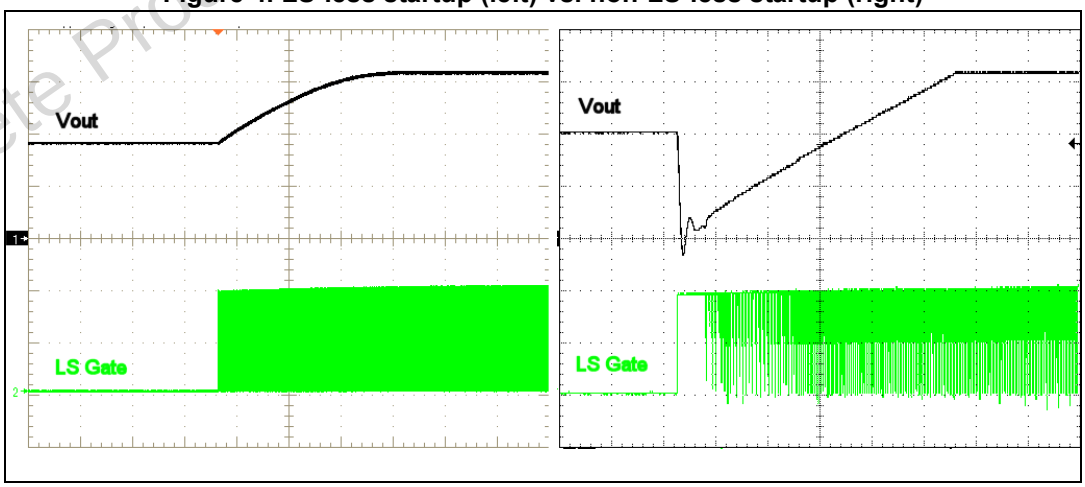
Low-side-less start up (LS-less)

In order to avoid any kind of the negative undershoot and dangerous return from the load the during the start-up, the L6728AH performs a special sequence in enabling the LS driver to switch: during the soft-start phase, the LS driver results disabled (LS = OFF) until the HS starts to switch. This avoids the dangerous negative spike on the output voltage that can happen if starting over a pre-biased output.

If the output voltage is pre-biased to a voltage higher than the final one, the HS would never start to switch. In this case, at the end of soft-start time, the LS is enabled and discharges the output to the final regulation value.

This particular feature of the device masks the LS turn-on only from the control loop point of view: protections bypass this turning ON the LS MOSFET in case of need.

Figure 4. LS-less startup (left) vs. non-LS-less startup (right)



7 Overcurrent protection

The overcurrent function protects the converter from a shorted output or overload, by sensing the output current information across the low-side MOSFET drain-source on-resistance, $R_{DS(on)}$. This method reduces the cost and enhances converter efficiency by avoiding the use of expensive and space-consuming sense resistors.

The low-side $R_{DS(on)}$ current sense is implemented by comparing the voltage at the PHASE node when the LS MOSFET is turned on with the programmed OCP thresholds voltages, internally held. If the monitored voltage is bigger than these thresholds, an overcurrent event is detected.

For maximum safety and load protection, the L6728AH implements a dual level overcurrent protection system:

- **1st level threshold**: it is the user externally set threshold. If the monitored voltage on the PHASE exceeds this threshold, a 1st level overcurrent is detected. If four 1st level OC events are detected in four consecutive switching cycles, overcurrent protection will be triggered.
- **2nd level threshold**: it is an internal threshold whose value is equal to the 1st level threshold multiplied by a factor 1.5. If the monitored voltage on the PHASE exceeds this threshold, overcurrent protection will be triggered immediately.

When overcurrent protection is triggered, the device turns off both LS and HS MOSFETs in a latched condition. To recover from overcurrent protection triggered condition, the V_{CC} power supply must be cycled.

Overcurrent threshold setting

The L6728AH allows to easily program a 1st level overcurrent threshold ranging from 50 mV to 550 mV, simply by adding a resistor (R_{OCSET}) between the LGATE and GND. The 2nd level threshold will be automatically set accordingly.

During a short period of time (about 5 ms) following V_{CC} rising over the UVLO threshold, an internal 10 µA current (I_{OCSET}) is sourced from the LGATE pin, determining a voltage drop across the R_{OCSET}. This voltage drop will be sampled and internally held by the device as the 1st level overcurrent threshold. The OC setting procedure overall time length is about 5 ms.

Connecting a R_{OCSET} resistor between the LGATE and GND, the programmed 1st level threshold will be:

Equation 3

$$I_{OCth1} = \frac{I_{OCSET} \cdot R_{OCSET}}{R_{dsON}}$$

the programmed 2nd level threshold will be:

Equation 4

$$I_{OCth2} = 1.5 \cdot \frac{I_{OCSET} \cdot R_{OCSET}}{R_{dsON}}$$

In case the R_{OCSET} is not connected, the device sets the OCP thresholds to the maximum values: an internal safety clamp on the LGATE is triggered as soon as LGATE voltage reaches 600 mV, setting the maximum threshold and suddenly ending the OC setting phase.

8 Output voltage setting and protections

The L6728AH is capable to precisely regulate an output voltage as low as 0.8 V. In fact, the device comes with a fixed 0.8 V internal reference that guarantee the output regulated voltage to be within ± 1% tolerance over line and temperature variations (excluding output resistor divider tolerance, when present).

Output voltage higher than 0.8 V can be easily achieved by adding a resistor R_{OS} between the FB pin and ground. Referring to *Figure 1 on page 4*, the steady state DC output voltage will be:

Equation 5

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R_{FB}}{R_{OS}}\right)$$

where V_{REF} is 0.8 V.

The L6728AH monitors the voltage at the VSEN pin and compares it to internal reference voltage in order to provide undervoltage and overvoltage protections as well as the PGOOD signal. According to the level of the VSEN, different actions are performed from the controller:

- PGOOD

  If the voltage monitored through the VSEN exits from the PGOOD window limits, the device deasserts the PGOOD signal still continuing switching and regulating. The PGOOD is asserted at the end of the soft-start phase.
- Undervoltage protection

  If the voltage at the VSEN pin drops below the UV threshold, the device turns off both HS and LS MOSFETs, latching the condition. Cycle V_{CC} to recover.
- Overvoltage protection

  If the voltage at the VSEN pin rises over the OV threshold (1 V typ.), overvoltage protection turns off the HS MOSFET and turns on the LS MOSFET. The LS MOSFET will be turned off as soon as the VSEN goes below $V_{REF}/2$ (0.4 V). The condition is latched, the cycle V_{CC} to recover. Notice that, even if the device is latched, the device still controls the LS MOSFET and can switch it on whenever the VSEN rises above 0.4 V.
- Feedback disconnection protection

  In order to provide load protection even if the VSEN pin is not connected, a 100 nA bias current is always sourced from this pin. If the VSEN pin is not connected, this current will permanently pull it up causing the device to detect an OV: thus the LS will be latched on preventing output voltage from rising out of control.

9 Application details

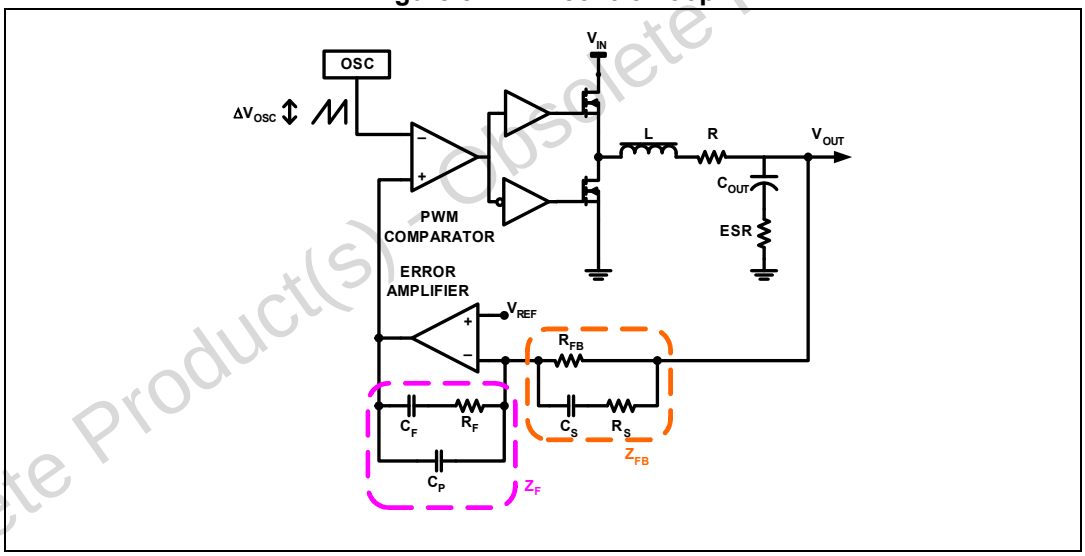
9.1 Compensation network

The control loop showed in *Figure 5* is a voltage mode control loop. The output voltage is regulated to the internal reference (when present, the offset resistor between the FB node and GND can be neglected in control loop calculation).

Error amplifier output is compared to the oscillator saw-tooth waveform to provide the PWM signal to the driver section. The PWM signal is then transferred to the switching node with V_{IN} amplitude. This waveform is filtered by the output filter.

The converter transfer function is the small signal transfer function between the output of the EA and V_{OUT}. This function has a double pole at frequency F_{LC} depending on the L-C output filter and a zero at F_{ESR} depending on the output capacitor ESR. The DC gain of the modulator is simply the input voltage V_{IN} divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

Figure 5. PWM control loop



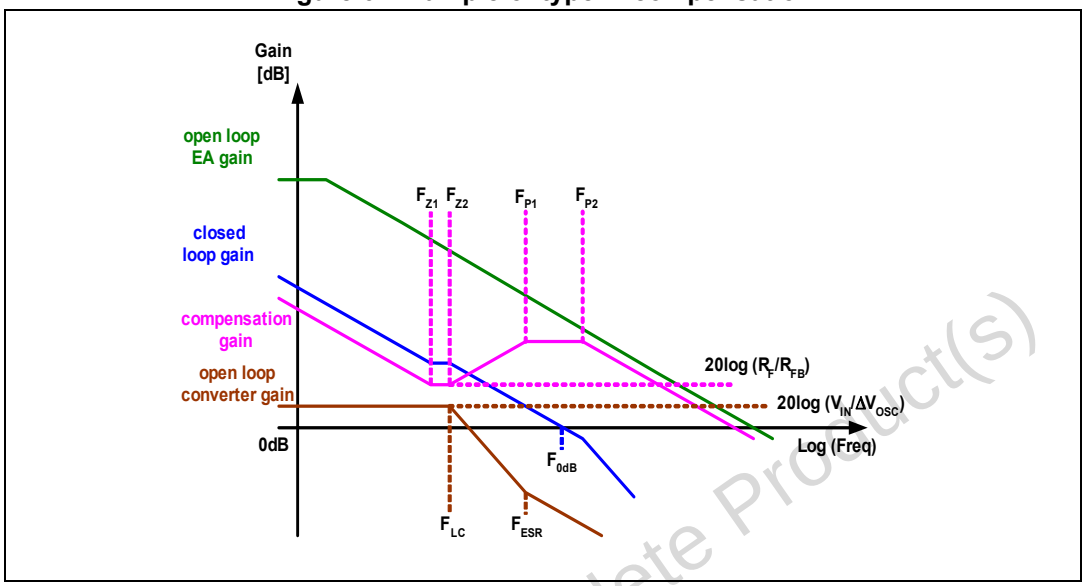
The compensation network closes the loop joining V_{OUT} and EA output with transfer function ideally equal to $-Z_F/Z_{FB}$.

The compensation goal is to close the control loop assuring high DC regulation accuracy, good dynamic performances and stability. To achieve this, the overall loop needs the high DC gain, high bandwidth and good phase margin.

The high DC gain is achieved giving an integrator shape to compensation network transfer function. The loop bandwidth (F_{0dB}) can be fixed choosing the right R_F/R_{FB} ratio, however, for stability, it should not exceed $F_{SW}/2\pi$. To achieve a good phase margin, the control loop gain has to cross 0 dB axis with a -20 dB/decade slope.

As an example, *Figure 6* shows an asymptotic bode plot of a type III compensation.

Figure 6. Example of type III compensation



- Open loop converter singularities:

  a) $F_{LC} = \frac{1}{2\pi\sqrt{L \cdot C_{OUT}}}$

  b) $F_{ESR} = \frac{1}{2\pi \cdot C_{OUT} \cdot ESR}$

- Compensation network singularities frequencies:

  a) $F_{Z1} = \frac{1}{2\pi \cdot R_F \cdot C_F}$

  b) $F_{Z2} = \frac{1}{2\pi \cdot (R_{FB} + R_S) \cdot C_S}$

  c) $F_{P1} = \frac{1}{2\pi \cdot R_F \cdot \left(\frac{C_F \cdot C_P}{C_F + C_P}\right)}$

  d) $F_{P2} = \frac{1}{2\pi \cdot R_S \cdot C_S}$

To place the poles and zeroes of the compensation network, the following suggestions may be followed:

a) Set the gain R_F/R_{FB} in order to obtain the desired closed loop regulator bandwidth according to the approximated formula (suggested values for the R_{FB} is in the range of some kΩ):

$$\frac{R_F}{R_{FB}} = \frac{F_{0dB}}{F_{LC}} \cdot \frac{\Delta V_{OSC}}{V_{IN}}$$

b) Place F_{Z1} below F_{LC} (typically 0.5 * F_{LC}):

$$C_F = \frac{1}{\pi \cdot R_F \cdot F_{LC}}$$

c) Place F_{P1} at F_{ESR}:

$$C_P = \frac{C_F}{2\pi \cdot R_F \cdot C_F \cdot F_{ESR} - 1}$$

d) Place F_{Z2} at F_{LC} and F_{P2} at the half of the switching frequency:

$$R_S = \frac{R_{FB}}{\frac{F_{SW}}{2 \cdot F_{LC}} - 1}$$

$$C_S = \frac{1}{\pi \cdot R_S \cdot F_{SW}}$$

e) Check that the compensation network gain is lower than the open loop EA gain before F_{0dB};

f) Check the phase margin obtained (it should be greater than 45°) and repeat if necessary.

9.2 Layout guidelines

The L6728AH provides control functions and high-current integrated drivers to implement high-current step-down DC-DC converters. In this kind of application, a good layout is very important.

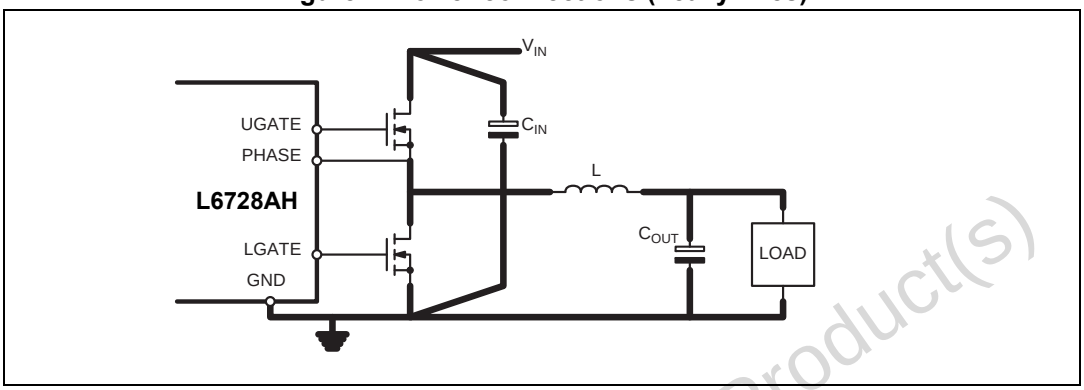
The first priority when placing components for these applications has to be reserved to the power section, minimizing the length of the each connection and loop as much as possible. To minimize noise and voltage spikes (EMI and losses) power connections (highlighted in *Figure 7*) must be a part of a power plane and anyway realized by wide and thick copper traces: the loop must be anyway minimized. The critical components, i.e. the power MOSFETs, must be close one to the other. The use of the multi-layer printed circuit board is recommended.

The input capacitance (C_{IN}), or at least a portion of the total capacitance needed, has to be placed close to the power section in order to eliminate the stray inductance generated by the copper traces. Low ESR and ESL capacitors are preferred, MLCC are suggested to be connected near the HS drain.

Use a proper VIAs number when power traces have to move between different planes on the PCB in order to reduce both parasitic resistance and inductance. Moreover, reproducing the same high-current trace on more than one PCB layer will reduce the parasitic resistance associated to that connection.

Connect output bulk capacitors (C_{OUT}) as near as possible to the load, minimizing parasitic inductance and resistance associated to the copper trace, also adding extra decoupling capacitors along the way to the load when this results in being far from the bulk capacitors bank.

Figure 7. Power connections (heavy lines)

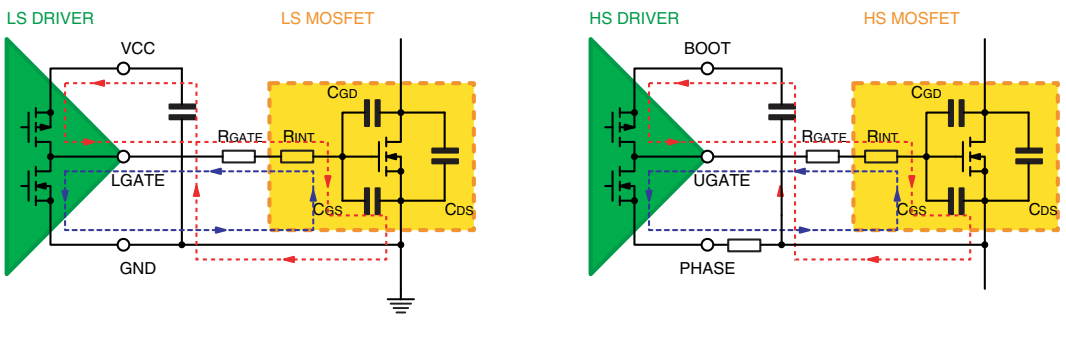


The gate traces and phase trace must be sized according to the driver RMS current delivered to the power MOSFET. The device robustness allows managing applications with the power section far from the controller without losing performances. Anyway, when possible, it is recommended to minimize the distance between the controller and power section.

Small signal components and connections to critical nodes of the application, as well as bypass capacitors for the device supply, are also important. Locate the bypass capacitor (V_{CC} and bootstrap capacitor) and feedback compensation components as close to the device as practical. For over current programmability, place the R_{OCSET} close to the device and avoid leakage current paths on the COMP/OC pin, since the internal current source is only 60 µA.

Systems that do not use the Schottky diode in parallel to the low-side MOSFET might show big negative spikes on the phase pin. This spike must be limited within the absolute maximum ratings (for example, adding a gate resistor in series to the HS MOSFET gate), as well as the positive spike, but has an additional consequence: it causes the bootstrap capacitor to be overcharged. This extra-charge can cause, in the worst case condition of maximum input voltage and during particular transients, that boot-to-phase voltage overcomes the absolute maximum ratings also causing device failures. It is then suggested in this cases to limit this extra-charge by adding a small resistor in series to the boot capacitor (one resistor in series to the BOOT).

Figure 8. Drivers turn-on and turn-off paths



10 Application information

10.1 Inductor design

The inductance value is defined by a compromise between the dynamic response time, the efficiency, the cost and the size. The inductor has to be calculated to maintain the ripple current (ΔI_L) between 20% and 30% of the maximum output current (typ.). The inductance value can be calculated with the following relationship:

Equation 6

$$L = \frac{V_{IN} - V_{OUT}}{F_{SW} \cdot \Delta I_L} \cdot \frac{V_{OUT}}{V_{IN}}$$

where F_{SW} is the switching frequency, V_{IN} is the input voltage and V_{OUT} is the output voltage.

Increasing the value of the inductance reduces the current ripple but, at the same time, increases the converter response time to a dynamic load change. The response time is the time required by the inductor to change its current from initial to final value. Until the inductor has not finished its charging time, the output current is supplied by the output capacitors. Minimizing the response time can minimize the output capacitance required. If the compensation network is well designed, during a load variation the device is able to set a duty-cycle value very different (0% or 80%) from the steady state one. When this condition is reached, the response time is limited by the time required to change the inductor current.

10.2 Output capacitor(s)

The output capacitors are basic components to define the ripple voltage across the output and for the fast transient response of the power supply. They depend on the output voltage ripple requirements, as well as any output voltage deviation requirement during a load transient.

During steady-state conditions, the output voltage ripple is influenced by both the ESR and capacitive value of the output capacitors as follow:

Equation 7

$$\Delta V_{OUT\_ESR} = \Delta I_L \cdot ESR$$

Equation 8

$$\Delta V_{OUT\_C} = \Delta I_L \cdot \frac{1}{8 \cdot C_{OUT} \cdot F_{SW}}$$

Where ΔI_L is the inductor current ripple. In particular, the expression that defines ΔV_{OUT_C} takes in consideration the output capacitor charge and discharge as a consequence of the inductor current ripple.

During a load variation, the output capacitors supply the current to the load or absorb the current stored into the inductor until the converter reacts. In fact, even if the controller recognizes immediately the load transient and sets the duty-cycle at 80% or 0%, the current slope is limited by the inductor value. The output voltage has a drop that also in this case depends on the ESR and capacitive charge/discharge as follow:

Equation 9

$$\Delta V_{OUT\_ESR} = \Delta I_{OUT} \cdot ESR$$

Equation 10

$$\Delta V_{OUT\_C} = \Delta I_{OUT} \cdot \frac{L \cdot \Delta I_{OUT}}{2 \cdot C_{OUT} \cdot \Delta V_L}$$

Where ΔV_L is the voltage applied to the inductor during the transient response ($D_{MAX} \cdot V_{IN} - V_{OUT}$ for the load appliance or V_{OUT} for the load removal).

MLCC capacitors have typically low ESR to minimize the ripple but also have low capacitance that do not minimize the voltage deviation during dynamic load variations. On the contrary, electrolytic capacitors have big capacitance to minimize voltage deviation during load transients while they do not show the same ESR values of the MLCC resulting then in higher ripple voltages. For these reasons, a mix between the electrolytic and MLCC capacitor is suggested to minimize the ripple as well as reducing voltage deviation in the dynamic mode.

10.3 Input capacitors

The input capacitor bank is designed considering mainly the input RMS current that depends on the output deliverable current (I_{OUT}) and the duty-cycle (D) for the regulation as follow:

Equation 11

$$I_{rms} = I_{OUT} \cdot \sqrt{D \cdot (1 - D)}$$

The equation reaches its maximum value, $I_{OUT}/2$, with D = 0.5. The losses depend on the input capacitor ESR and, in worst case, are:

Equation 12

$$P = ESR \cdot (I_{OUT}/2)^2$$

11 20 A demonstration board

The L6728AH 20 A demonstration board realizes, in a two-layer PCB, a step-down DC/DC converter and shows the operation of the device in a general-purpose high-current application. Different output voltage rails have been considered: 8 V, 5 V, 3.3 V, 2.5 V, 1.25 V and 0.8 V. The input voltage can range from a bottom value that depends on the chosen rail up to 15 V buses (absolute maximum). The application can deliver an output current up to the value fixed by R_{OCSET} (~27 A).

Figure 9. 20 A demonstration board (left) and components placement (right)

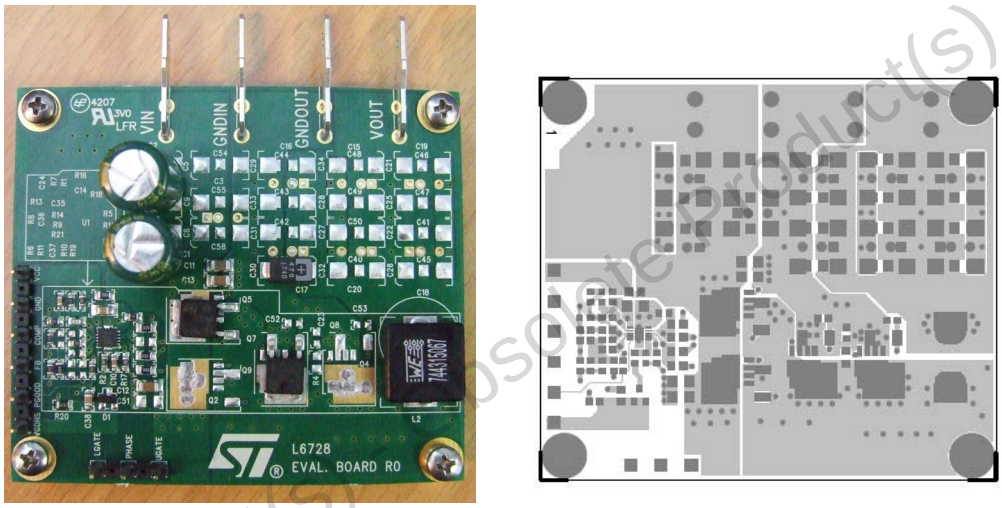


Figure 10. 20 A demonstration board's top (left) and bottom (right) layers

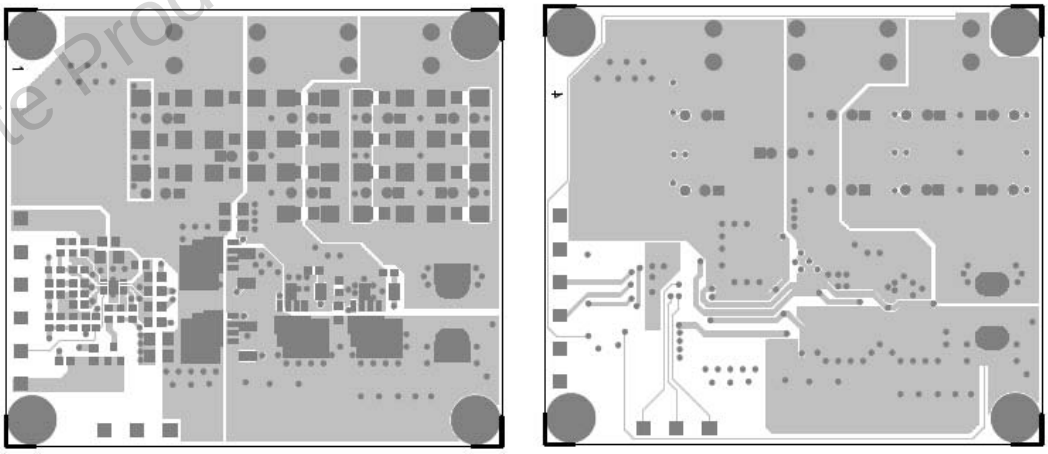


Figure 11. 20 A demonstration board schematic

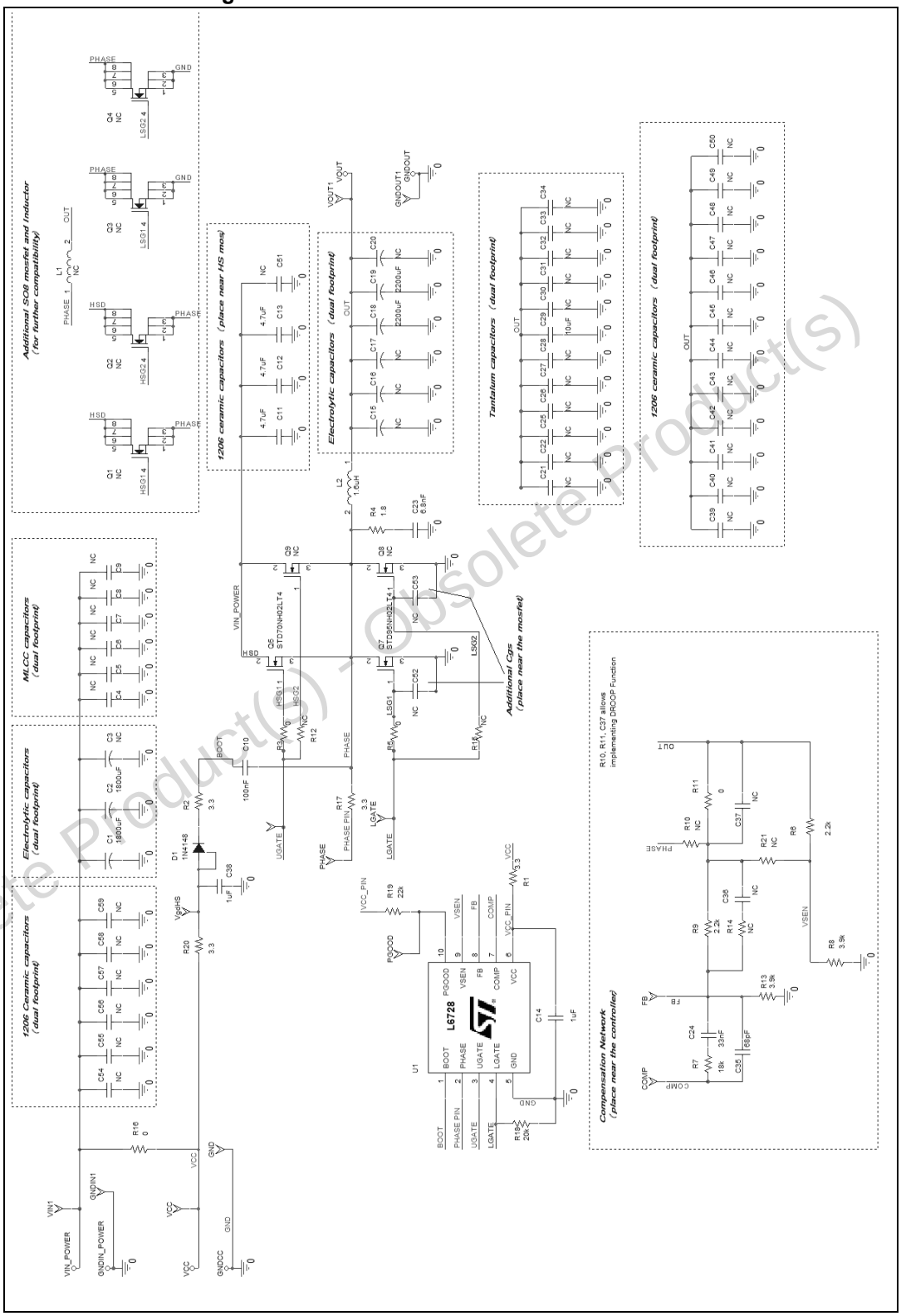


Table 6. 20A demonstration board - bill of material (common components)

Qty.	Reference	Description	Package
Capacitors			
2	C1, C2	Electrolytic capacitor 1800 µF 16 V Sanyo P/N 16ME1800WG	Radial 10 x 23 mm
1	C10	MLCC, 100 nF, 50 V, X7R Murata GRM188R71H104K	SMD0603
3	C11 to C13	MLCC, 4.7 µF, 16 V, X7R Murata GRM31CR71C475K	SMD1206
2	C14, C38	MLCC, 1 µF, 16 V, X7R Murata GRM21BR71C105K	SMD0805
48	C3 to C9, C15 to C20, C39 to C59, C36, C37, C21 to C23, C25 to C29, C31 to C34	Not mounted	N.A.
1	C30	POSCAP 470 µF, 6.3 V, 10 mΩ Sanyo P/N 6TPD470M	SMD1206
1	C24	MLCC, 47 nF, 50 V, X7R Murata GRM188R71H473K	SMD0603
1	C35	MLCC, 100 pF, 50 V, X7R Murata GRM188R71H101K	
Resistors			
4	R1, R2, R20, R17	Resistor, 2R2, 1/16W, 1%	SMD0603
5	R3, R5, R11, R12, R16	Resistor, 0R, 1/8W, 1%	SMD0805
5	R4, R10, R14, R15, R21	Not mounted	N.A.
1	R19	Resistor, 22 K, 1/16W, 1%	SMD0603
1	R18	Resistor, 18 K, 1/16W, 1%	
Inductor			
1	L1	Wurth SMD power inductor 670 nH - 1.75 mΩ - 40 A P/N 744-315-067	N.A.
1	L2	Not mounted	
Active components			
1	D1	Diode, 1N4148	SOT23
5	Q1 to Q4, Q8	Not mounted	N.A.
1	Q5	STD70NH02L	DPACK
1	Q7	STD95NH02L	
1	U1	Controller, L6728AH	VFDFPN 10, 3 x 3 mm

11.1 Demonstration board description

11.1.1 Power input (V_{IN})

This is the input voltage for the power conversion. The high-side drain is connected to this input. This voltage can range from 1.5 V to 12 V bus.

If the voltage is between 5 V and 12 V it can supply also the device (through the V_{CC} pin) and in this case the R16 (0 Ω) resistor must be present.

11.1.2 Output (V_{OUT})

Different output voltage rails have been tested. For each rail a few components need to be changed: these components are used to program the desiderated output voltage and to compensate the system. The overcurrent-protection limit is set to ~27 A but it can be changed by replacing the resistors R18.

Table 7. Rail dependent components

Ref.	8 V rail	5 V rail	3.3 V rail	2.5 V rail	1.25 V rail	0.8 V rail
Q9	Mounted		Not mounted			
R7	3.6 kΩ	3.6 kΩ	3.6 kΩ	3.6 kΩ	11 kΩ	11 kΩ
R6, R9	3.6 kΩ	3.6 kΩ	4.7 kΩ	4.7 kΩ	22 kΩ	22 kΩ
R8, R13	390 Ω	680 Ω	1.5 kΩ	2.2 kΩ	39 kΩ	Open

Note: All the previous resistors are the SMD 0603 package, 1/16 W, 1% tolerance.

11.1.3 Signal input (V_{CC})

Using the input voltage V_{IN} to supply the controller no power is required at this input. However the controller can be supplied separately from the power stage through the V_{CC} input and, in this case, the R16 (0 Ω) resistor must be unsoldered.

11.1.4 Test points

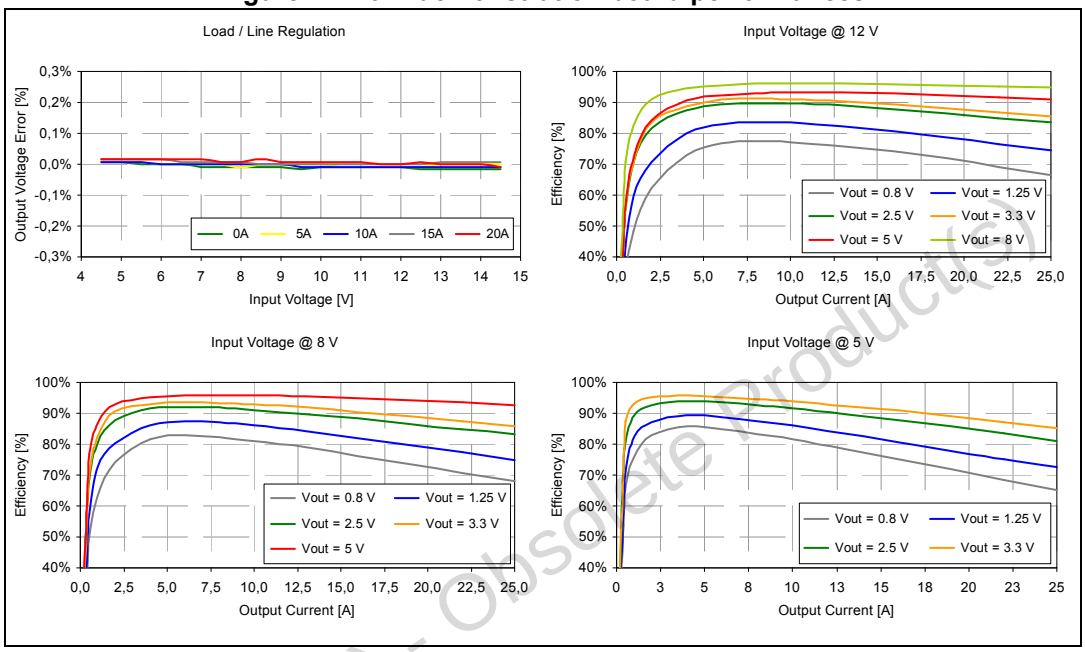
Several test points are provided to have easy access at the all important signal characterizing the device:

- COMP: the output of the error amplifier
- FB: the inverting input of the error amplifier
- PGOOD: signaling the regular functioning (active high)
- VGDHS: the bootstrap diode anode
- PHASE: the phase node
- LGATE: the low-side gate pin of the device
- HGATE: the high-side gate pin of the device.

11.2 Demonstration board characterization

Figure 12 and *Figure 17* show the electrical performances of the tamboured in terms of accuracy and efficiency.

Figure 12. 20 A demonstration board performances



12 5 A demonstration board

The L6728AH 5 A demonstration board realizes, in a two-layer PCB, a step-down DC/DC converter and shows the operation of the device in a general-purpose high-current application. Different output voltage rails have been considered: 8 V, 5 V, 3.3 V, 2.5 V, 1.25 V and 0.8 V. The input voltage can range from a bottom value that depends on the chosen rail up to 15 V buses (absolute maximum). The application can deliver an output current up to the value fixed by R_{OCSET} (~6 A).

Figure 13. 5 A demonstration board (left) and components placement (right)

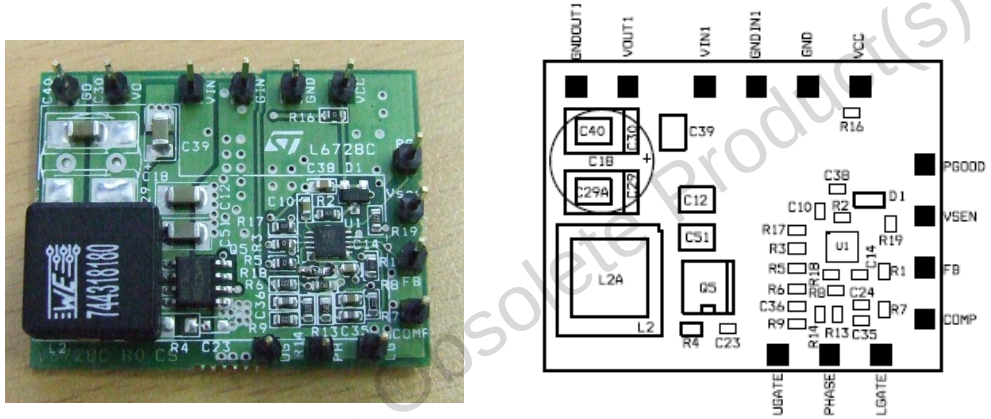


Figure 14. 5 A demonstration board's top (left) and bottom (right) layers

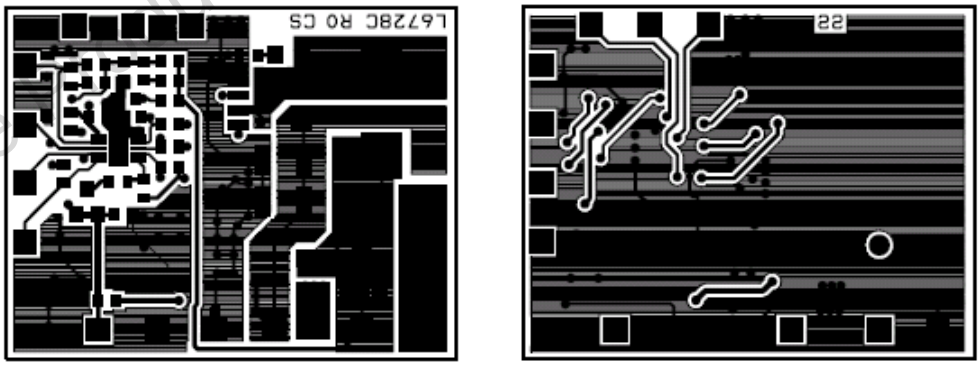


Figure 15. 5 A demonstration board schematic

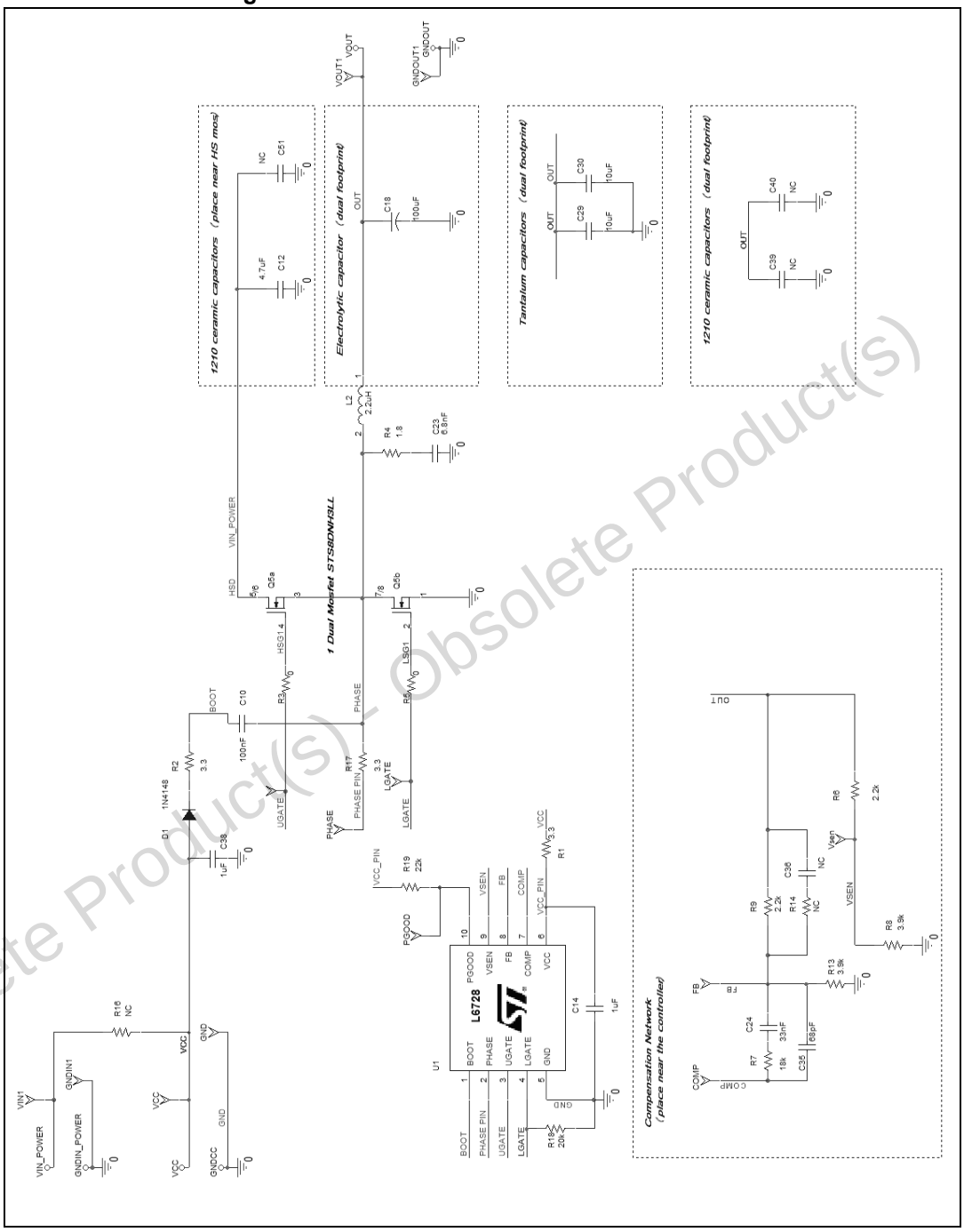


Table 8. 5 A demonstration board - bill of material

Qty.	Reference	Description	Package
Capacitors			
2	C12, C51	MLCC, 10 µF, 16 V, X5R Murata GRM31CR61C106K	SMD1206
1	C10	MLCC, 100 nF, 50 V, X7R Murata GRM188R71H104K	SMD0603
2	C14, C38	MLCC, 1 µF, 16 V, X7R Murata GRM21BR71C105K	SMD0805
2	C39, C40	MLCC, 22 µF, 6.3 V, X5R Murata GRM31CR60J226K	SMD1206
2	C36	MLCC, 10 nF, 50 V, X7R Murata GRM188R71H103K	SMD0603
1	C24	MLCC, 47 nF, 50 V, X7R Murata GRM188R71H223K	
1	C35	MLCC, 1 nF, 50 V, X7R Murata GRM188R71H102K	
Resistors			
3	R1, R2, R17	Resistor, 3R3, 1/16 W, 1%	SMD0603
3	R3, R5, R16	Resistor, 0R, 1/8 W, 1%	
1	R14	Resistor, 51R, 1/8 W, 1%	
2	R6, R9	Resistor, 2K2, 1/16 W, 1%	
2	R8, R13	Resistor, 3K9, 1/16 W, 1%	
1	R7	Resistor, 270 R, 1/16 W, 1%	
1	R19	Resistor, 22 K, 1/16 W, 1%	
1	R18	Resistor, 18 K, 1/16 W, 1%	
Inductor			
1	L1	Wurth SMD power inductor 1.8 µH - 3.68 mΩ - 20 A P/N 744-318-180	N.A.
Active components			
1	D1	Diode, BAT54	SOT23
1	Q5	Dual N-channel MOS, STS8DNF3LL (the STS8DNH3LL model can be used as well)	SO8
1	U1	Controller, L6728AH	VFDFPN 10 3 x 3 mm

12.1 Demonstration board description

12.1.1 Power input (V_{IN})

This is the input voltage for the power conversion. The high-side drain is connected to this input. This voltage can range from 1.5 V to 12 V bus.

If the voltage is between 5 V and 12 V it can supply also the device (through the Vcc pin) and in this case the R16 (0 Ω) resistor must be present.

12.1.2 Output (V_{OUT})

Different output voltage rails have been tested. For each rail a few components need to be changed: these components are used to program the desiderate output voltage. The OCP limit is set to ~6 A but it can be changed by replacing the resistors R18.

Table 9. Rail dependent components

Ref.	8 V rail	5 V rail	3.3 V rail	2.5 V rail	1.25 V rail	0.8 V rail
R8, R13	240 Ω	430 Ω	680 Ω	1 kΩ	3.9 kΩ	Open

Note: All the previous resistors are the SMD 0603 package, 1/16 W, 1% tolerance.

12.1.3 Signal input (V_{CC})

Using the input voltage V_{IN} to supply the controller no power is required at this input. However the controller can be supplied separately from the power stage through the V_{CC} input (5-12 V) and, in this case, the R16 (0 Ω) resistor must be unsoldered.

12.1.4 Test points

Several test points are provided to have easy access at all important signal characterizing the device:

- COMP: the output of the error amplifier
- FB: the inverting input of the error amplifier
- PGOOD: signaling the regular functioning (active high)
- VGDHS: the bootstrap diode anode
- PHASE: the phase node
- LGATE: the low-side gate pin of the device
- the HGATE: the high-side gate pin of the device.

12.2 Demonstration board characterization

Figure 16 and *Figure 17* show the electrical performances of the demonstration board in terms of accuracy and efficiency.

Figure 16. 5 A demonstration board performances

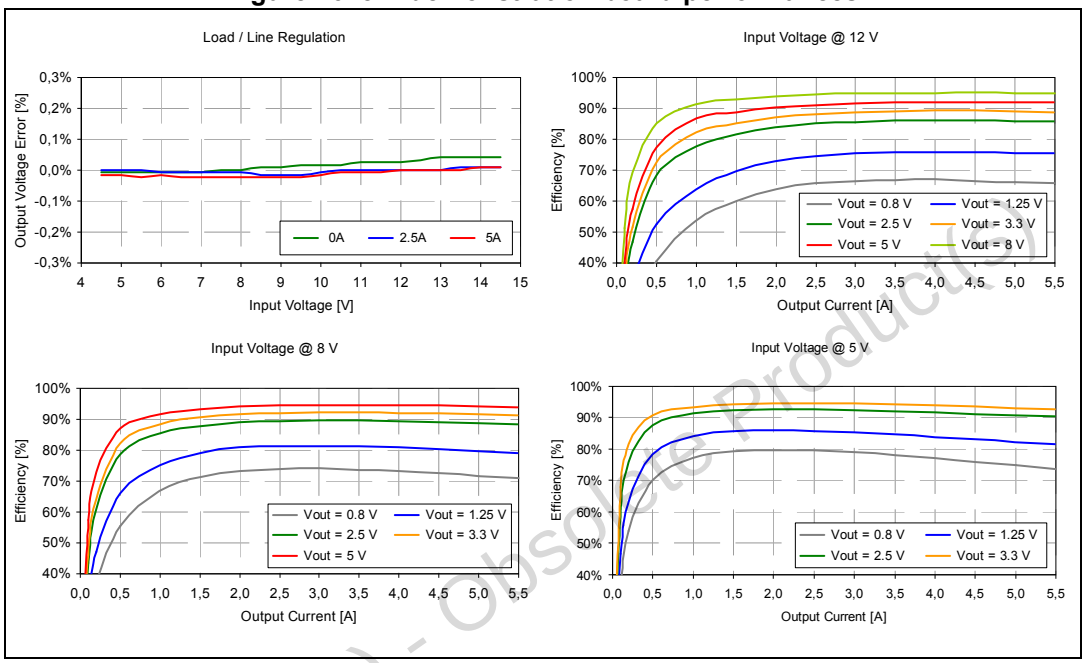
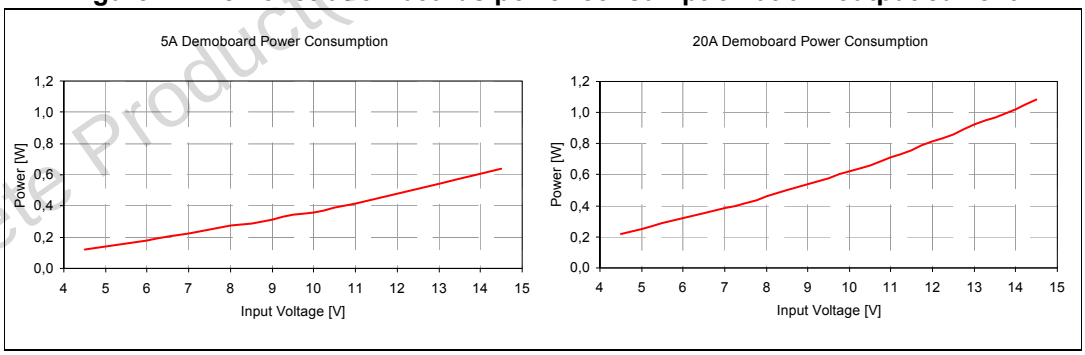


Figure 17. Demonstration boards power consumption at 0 A output current



13 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

13.1 VFDFPN10 3 x 3 mm package information

Figure 18. VFDFPN10 3 x 3 mm package outline

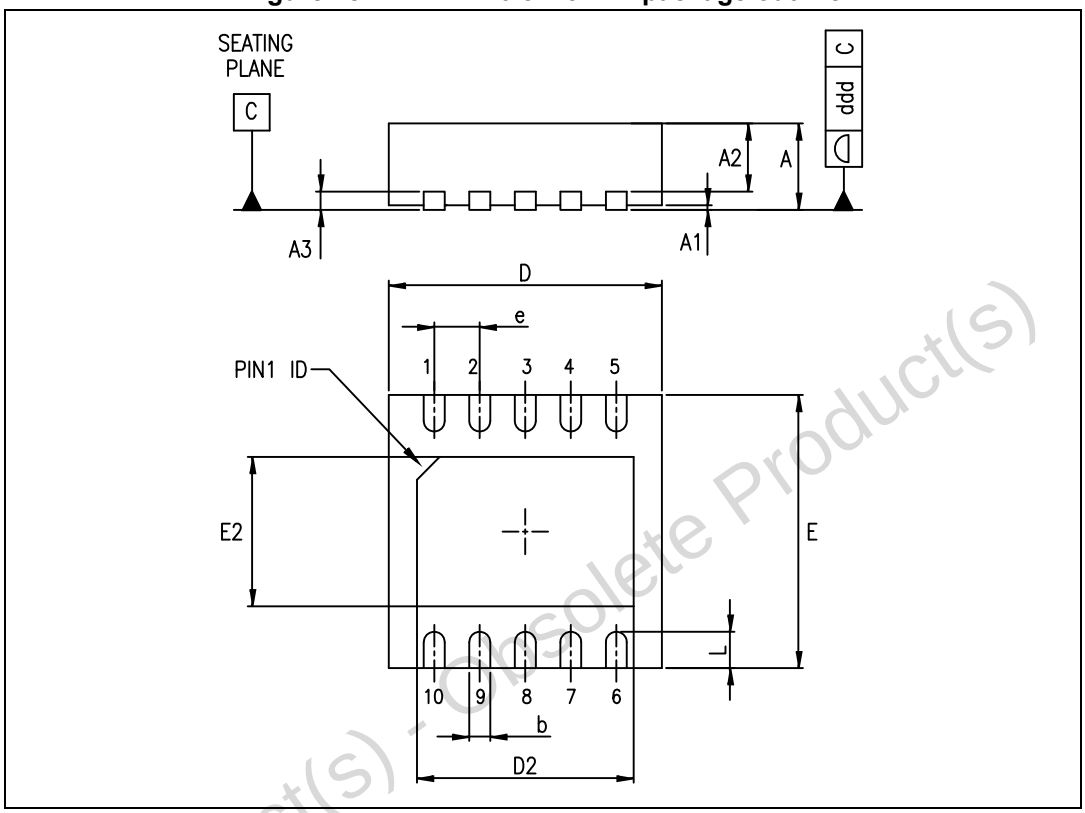


Table 10. VFDFPN10 3 x 3 mm package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1		0.02	0.05
A2		0.70	
A3		0.20	
b	0.18	0.23	0.30
D		3.00	
D2	2.21	2.26	2.31
E		3.00	
E2	1.49	1.64	1.74
e		0.50	
L	0.3	0.4	0.5
M		0.75	
m		0.25	

14 Revision history

Table 11. Document revision history

Date	Revision	Changes
20-May-2009	1	Initial release
01-Aug-2016	2	Updated VFDFPN 10 figure on page 1 (replaced by new figure). Updated *Figure 18 on page 34* (replaced by new figure). Updated *Table 10 on page 34* (removed mils values). Minor modifications throughout document.

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