NEC

MOS INTEGRATED CIRCUIT

μPD42S16160L, 4216160L, 42S18160L, 4218160L

3.3 V OPERATION 16M-BIT DYNAMIC RAM
1M-WORD BY 16-BIT, FAST PAGE MODE, BYTE READ/WRITE MODE

Description

The μPD42S16160L, 4216160L, 42S18160L, 4218160L are 1 048 576 words by 16 bits dynamic CMOS RAMs.

These differ in refresh cycle and the μPD42S16160L, 42S18160L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh (see the table below).

These are packed in 50-pin plastic TSOP(II) and 42-pin plastic SOJ.

Features

- 1 048 576 words by 16 bits organization
- Fast page mode
- Fast access and cycle time
- Single +3.3 V ± 0.3 V power supply
- Byte read/write mode

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μPD42S16160L-A60, 4216160L-A60	324 mW	60 ns	110 ns	40 ns
μPD42S18160L-A60, 4218160L-A60	540 mW			
μPD42S16160L-A70, 4216160L-A70	288 mW	70 ns	130 ns	45 ns
μPD42S18160L-A70, 4218160L-A70	504 mW			

- The μPD42S16160L, 42S18160L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S16160L	4 096 cycles/128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, hidden refresh	0.54 mW (CMOS level input)
μPD42S18160L	1 024 cycles/128 ms		
μPD4216160L	4 096 cycles/64 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, hidden refresh	1.8 mW (CMOS level input)
μPD4218160L	1 024 cycles/16 ms		

Ordering Information

Part number	Access time (MAX.)	Package	Refresh
μPD42S16160LG5-A60	60 ns	50-pin Plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD42S18160LG5-A60			
μPD42S16160LG5-A70	70 ns		
μPD42S18160LG5-A70			
μPD42S16160LLE-A60	60 ns	42-pin Plastic SOJ (400 mil)	
μPD42S18160LLE-A60			
μPD42S16160LLE-A70	70 ns		
μPD42S18160LLE-A70			
μPD4216160LG5-A60	60 ns	50-pin Plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4218160LG5-A60			
μPD4216160LG5-A70	70 ns		
μPD4218160LG5-A70			
μPD4216160LLE-A60	60 ns	42-pin Plastic SOJ (400 mil)	
μPD4218160LLE-A60			
μPD4216160LLE-A70	70 ns		
μPD4218160LLE-A70			

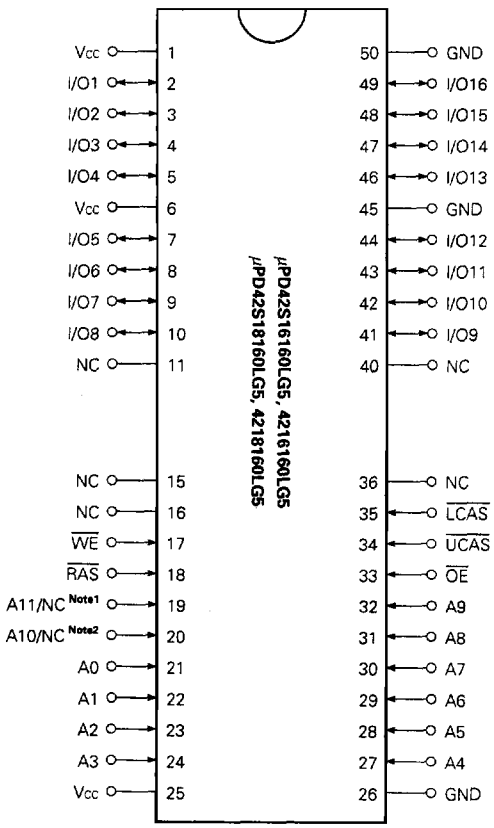
Quality Grade

Standard

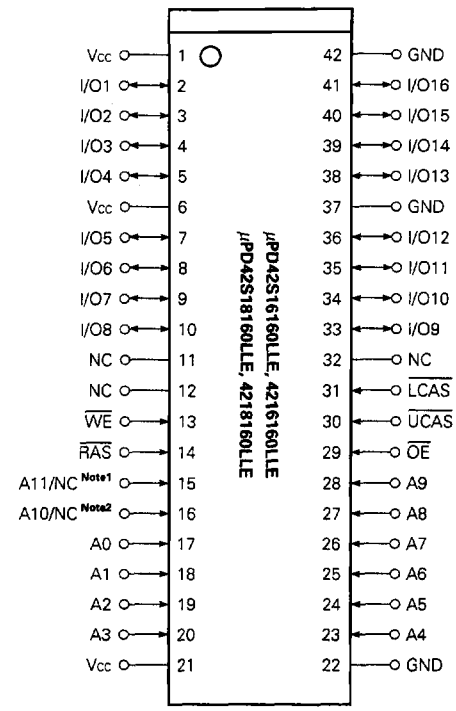
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configurations (Marking Side)

50-pin Plastic TSOP (II)



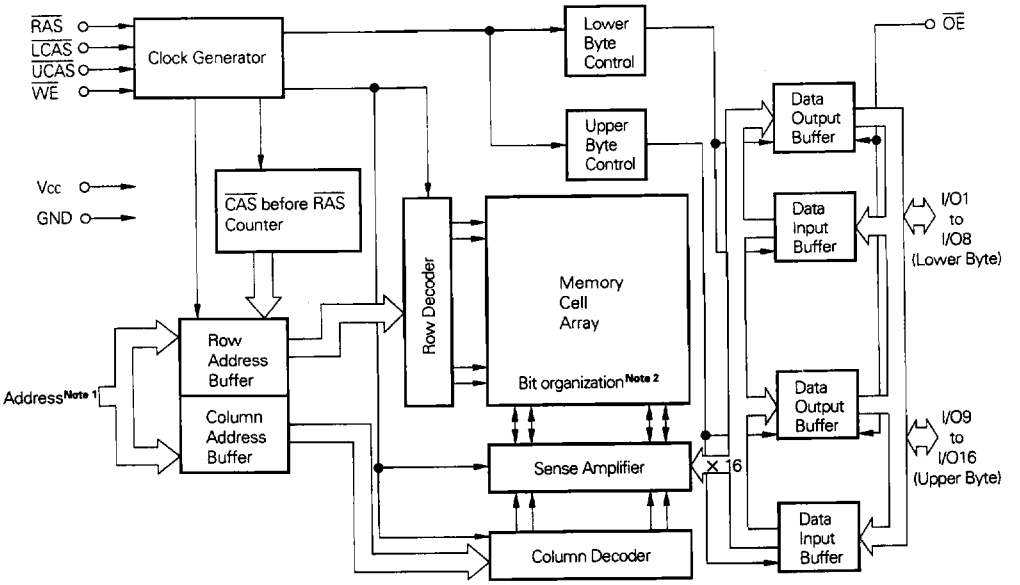
42-pin Plastic SOJ



Notes 1. A11 · · · μPD42S16160L, 4216160L NC . . . μPD42S18160L, 4218160L
2. A10 · · · μPD42S16160L, 4216160L NC . . . μPD42S18160L, 4218160L

A0 to A11	:	Address Inputs
I/O1 to I/O16	:	Data Inputs/Outputs
$\overline{RAS}$	:	Row Address Strobe
$\overline{UCAS}$	:	Column Address Strobe (upper)
$\overline{LCAS}$	:	Column Address Strobe (lower)
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No Connection

Block Diagram



Notes 1.

Part number	Row address	Column address
μPD42S16160L, 4216160L	A0 to A11	A0 to A7
μPD42S18160L, 4218160L	A0 to A9	A0 to A9

2. μPD42S16160L, 4216160L · · · 4 096 × 256 × 16 μPD42S18160L, 4218160L · · · 1 024 × 1 024 × 16

Input/Output Pin Functions

The μPD42S16160L, 4216160L, 42S18160L, 4218160L have input pins $\overline{RAS}$, $\overline{CAS}$ Note1, $\overline{WE}$, $\overline{OE}$, A0 to A11/A9 Note2 and input/output pins I/O1 to I/O16.

Pin name	Input/ Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)		$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A11/A9Note2 (Address inputs)		Address bus. Input total 20-bit of address signal, upper 12/10Note3-bit and lower 8/10Note4-bit in sequence (address multiplex method). Therefore, one word is selected from 1 048 576-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data inputs/outputs)	Input/ Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

Notes 1. $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.
2. A11 ... μPD42S16160L, 4216160L A9 ... μPD42S18160L, 4218160L
3. 12 ... μPD42S16160L, 4216160L 10 ... μPD42S18160L, 4218160L
4. 8 ... μPD42S16160L, 4216160L 10 ... μPD42S18160L, 4218160L

Electrical Specifications

- $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.
- All voltages are referenced to GND.
- After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		− 0.5 to +4.6	V
Supply voltage	V_{CC}		− 0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		1	W
Operating temperature	T_{opt}		0 to +70	°C
Storage temperature	T_{stg}		− 55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} +0.3	V
Low level input voltage	V_{IL}		− 0.3		+0.8	V
Ambient temperature	T_a		0		70	°C

Capacitance (T_a = +25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 to A11			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	pF
Data Input/Output capacitance	$C_{I/O}$	I/O1 to I/O16			7	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)
[μPD42S16160L, 4216160L]

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		90	mA	1,2,3
				t_{RAC} = 70 ns		80		
Standby current	μPD42S16160L	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geqq V_{IH(MIN.)}$	I_O = 0 mA		0.5	mA	
			$\overline{RAS}$, $\overline{CAS} \geqq V_{CC} - 0.2$ V	I_O = 0 mA		0.15		
	μPD4216160L		$\overline{RAS}$, $\overline{CAS} \geqq V_{IH(MIN.)}$	I_O = 0 mA		2		
			$\overline{RAS}$, $\overline{CAS} \geqq V_{CC} - 0.2$ V	I_O = 0 mA		0.5		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geqq V_{IH(MIN.)}$ $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		90	mA	1,2,3,4
				t_{RAC} = 70 ns		80		
Operating current (Fast page mode)		I_{CC4}	$\overline{RAS} \leqq V_{IL(MAX.)}$ $\overline{CAS}$ Cycling $t_{PC} = t_{PC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		90	mA	1,2,5
				t_{RAC} = 70 ns		80		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		90	mA	1,2
				t_{RAC} = 70 ns		80		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (4 096 cycles / 128 ms, only for μPD42S16160L)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh : 4 096 cycles/128 ms $\overline{RAS}$, $\overline{CAS}$: $V_{CC-0.2\,V} \leqq V_{IH} \leqq V_{IH(MAX.)}$ 0 V ≦ V_{IL} ≦ 0.2 V Standby : $\overline{RAS} \geqq V_{CC-0.2\,V}$ Address : Don't care $\overline{WE}$, $\overline{OE}$: V_{IH} I_O = 0 mA	$t_{RAS} \leqq 1$ μs		220	μA	1,2
Self refresh current ($\overline{CAS}$ before $\overline{RAS}$ self refresh, only for μPD42S16160L)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: $V_{CC-0.2\,V} \leqq V_{IH} \leqq V_{IH(MAX.)}$ 0 V ≦ V_{IL} ≦ 0.2 V I_O = 0 mA			150	μA	2
Input leakage current		$I_{I(L)}$	V_I = 0 to 3.6 V all other pins not under test = 0 V		−5	+5	μA	
Output leakage current		$I_{O(L)}$	Output is disabled (Hi-Z) V_O = 0 to 3.6 V		−5	+5	μA	
High level output voltage		V_{OH}	I_O = −2.0 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = 2.0 mA			0.4	V	

[μPD42S18160L, 4218160L]

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		150	mA	1,2,3
				t_{RAC} = 70 ns		140		
Standby current	μPD42S18160L	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ ≧ $V_{IH(MIN.)}$	I_O = 0 mA		0.5	mA	
			$\overline{RAS}$, $\overline{CAS}$ ≧ V_{CC} – 0.2 V	I_O = 0 mA		0.15		
	μPD4218160L		$\overline{RAS}$, $\overline{CAS}$ ≧ $V_{IH(MIN.)}$	I_O = 0 mA		2		
			$\overline{RAS}$, $\overline{CAS}$ ≧ V_{CC} – 0.2 V	I_O = 0 mA		0.5		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS}$ ≧ $V_{IH(MIN.)}$ $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		150	mA	1,2,3,4
				t_{RAC} = 70 ns		140		
Operating current (Fast page mode)		I_{CC4}	$\overline{RAS}$ ≦ $V_{IL(MAX.)}$ $\overline{CAS}$ Cycling $t_{PC} = t_{PC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		90	mA	1,2,5
				t_{RAC} = 70 ns		80		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		150	mA	1,2
				t_{RAC} = 70 ns		140		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (1 024 cycles / 128 ms, only for μPD42S18160L)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh : 1 024 cycles/128 ms $\overline{RAS}$, $\overline{CAS}$: V_{CC}–0.2 V ≦ V_{IH} ≦ $V_{IH(MAX.)}$ 0 V ≦ V_{IL} ≦ 0.2 V Standby : $\overline{RAS}$ ≧ V_{CC}–0.2 V Address : Don't care $\overline{WE}$, $\overline{OE}$: V_{IH} I_O = 0 mA	t_{RAS} ≧ 1 μs		180	μA	1,2
Self refresh current ($\overline{CAS}$ before $\overline{RAS}$ self refresh, only for μPD42S18160L)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: V_{CC}–0.2 V ≦ V_{IH} ≦ $V_{IH(MAX.)}$ 0 V ≦ V_{IL} ≦ 0.2 V I_O = 0 mA			150	μA	2
Input leakage current		$I_{I(L)}$	V_I = 0 to 3.6 V all other pins not under test = 0 V		–5	+5	μA	
Output leakage current		$I_{O(L)}$	Output is disabled (Hi-Z) V_O = 0 to 3.6 V		–5	+5	μA	
High level output voltage		V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = 2.0 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS}$ ≦ $V_{IL(MAX.)}$ and $\overline{CAS}$ ≧ $V_{IH(MIN.)}$.

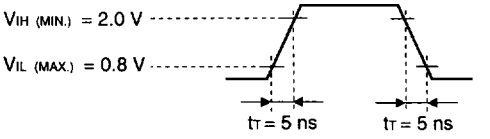
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

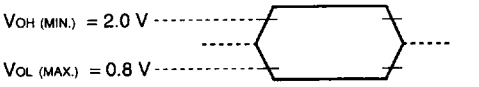
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	tRAC = 60 ns		tRAC = 70 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time		tRC	110	–	130	–	ns	
$\overline{RAS}$ Precharge Time		tRP	40	–	50	–	ns	
$\overline{CAS}$ Precharge Time		tCPN	10	–	10	–	ns	
$\overline{RAS}$ Pulse Width		tRAS	60	10 000	70	10 000	ns	
$\overline{CAS}$ Pulse Width		tCAS	15	10 000	20	10 000	ns	
$\overline{RAS}$ Hold Time		tRSH	15	–	18	–	ns	
$\overline{CAS}$ Hold Time		tCSH	60	–	70	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time		tRCD	20	45	20	50	ns	1
$\overline{RAS}$ to Column Address Delay Time		tRAD	15	30	15	35	ns	1
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		tCRP	5	–	5	–	ns	2
Row Address Setup Time		tASR	0	–	0	–	ns	
Row Address Hold Time		tRAH	10	–	10	–	ns	
Column Address Setup Time		tASC	0	–	0	–	ns	
Column Address Hold Time		tCAH	15	–	15	–	ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$		tOES	0	–	0	–	ns	
$\overline{CAS}$ to Data Setup Time		tCLZ	0	–	0	–	ns	
$\overline{OE}$ to Data Setup Time		tOLZ	0	–	0	–	ns	
$\overline{OE}$ to Data Delay Time		tOED	13	–	15	–	ns	
Masked Byte Write Hold Time Referenced to $\overline{RAS}$		tMRH	0	–	0	–	ns	
Transition Time (Rise and Fall)		tT	3	50	3	50	ns	
Refresh Time	μPD42S16160L, 42S18160L	tREF	–	128	–	128	ms	3
	μPD4216160L		–	64	–	64		
	μPD4218160L		–	16	–	16		

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD(MAX.)}$ and $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.

2. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.
3. This specification is applied only to the μPD42S16160L, 42S18160L.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	–	60	–	70	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	–	15	–	20	ns	1
Access Time from Column Address	t_{AA}	–	30	–	35	ns	1
Access Time from $\overline{OE}$	t_{OEA}	–	15	–	20	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	ns	
Read Command Setup Time	t_{RCS}	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	3
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	13	0	15	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD(MAX.)}$ and $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.
3. $t_{OFF(MAX.)}$ and $t_{OEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	ns	1
$\overline{WE}$ Pulse Width	t_{WP}	10	–	10	–	ns	1
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	20	–	20	–	ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	15	–	15	–	ns	
$\overline{WE}$ Setup Time	t_{WCS}	0	–	0	–	ns	2
$\overline{OE}$ Hold Time	t_{OEH}	0	–	0	–	ns	
Data-in Setup Time	t_{DS}	0	–	0	–	ns	3
Data-in Hold Time	t_{DH}	10	–	15	–	ns	3

Notes 1. $t_{WP(MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH(MIN.)}$ should be met.

2. If $t_{WCS} \geqq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS(MIN.)}$ and $t_{DH(MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	t_{RWC}	160	–	180	–	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	83	–	95	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	38	–	40	–	ns	1
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	53	–	60	–	ns	1

Note 1. If $t_{WCS} \geqq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geqq t_{RWD(MIN.)}$, $t_{CWD} \geqq t_{CWD(MIN.)}$, $t_{AWD} \geqq t_{AWD(MIN.)}$ and $t_{CPWD} \geqq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Fast Page Mode Cycle Time	t_{PC}	40	–	45	–	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	–	35	–	40	ns	
$\overline{RAS}$ Pulse Width	t_{RASP}	60	125 000	70	125 000	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	–	10	–	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	–	40	–	ns	
Read Modify Write Cycle Time	t_{PRWC}	85	–	90	–	ns	
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	60	–	65	–	ns	1

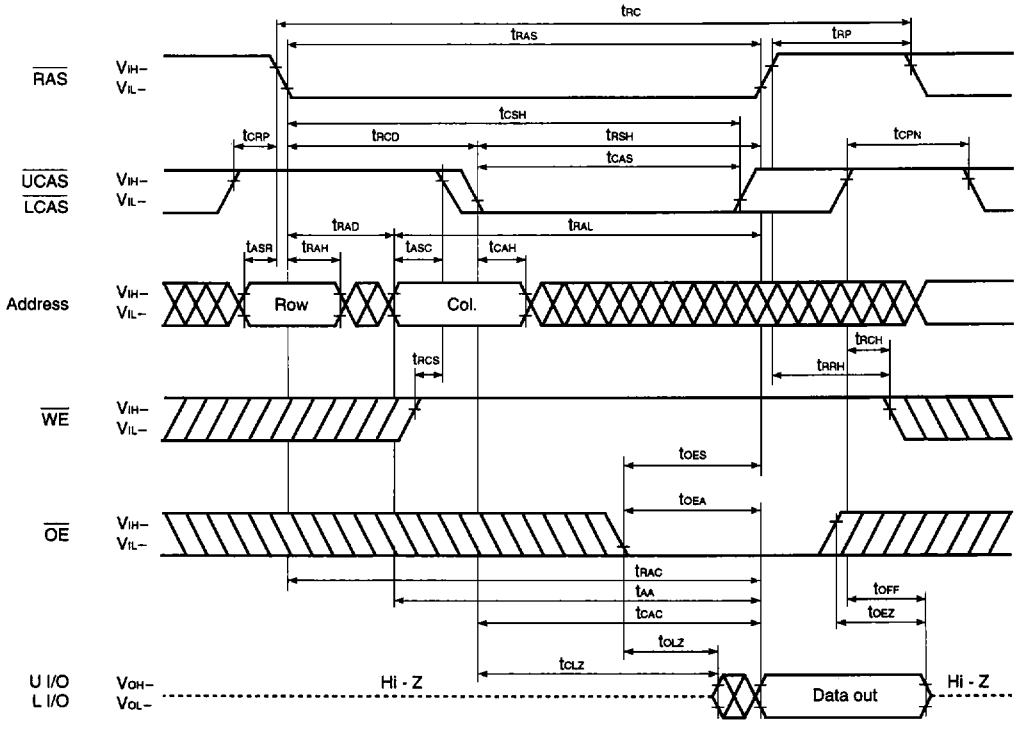
Note 1. If $t_{WCS} \geqq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If $t_{RWD} \geqq t_{RWD(MIN.)}$, $t_{CWD} \geqq t_{CWD(MIN.)}$, $t_{AWD} \geqq t_{AWD(MIN.)}$ and $t_{CPWD} \geqq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Refresh Cycle

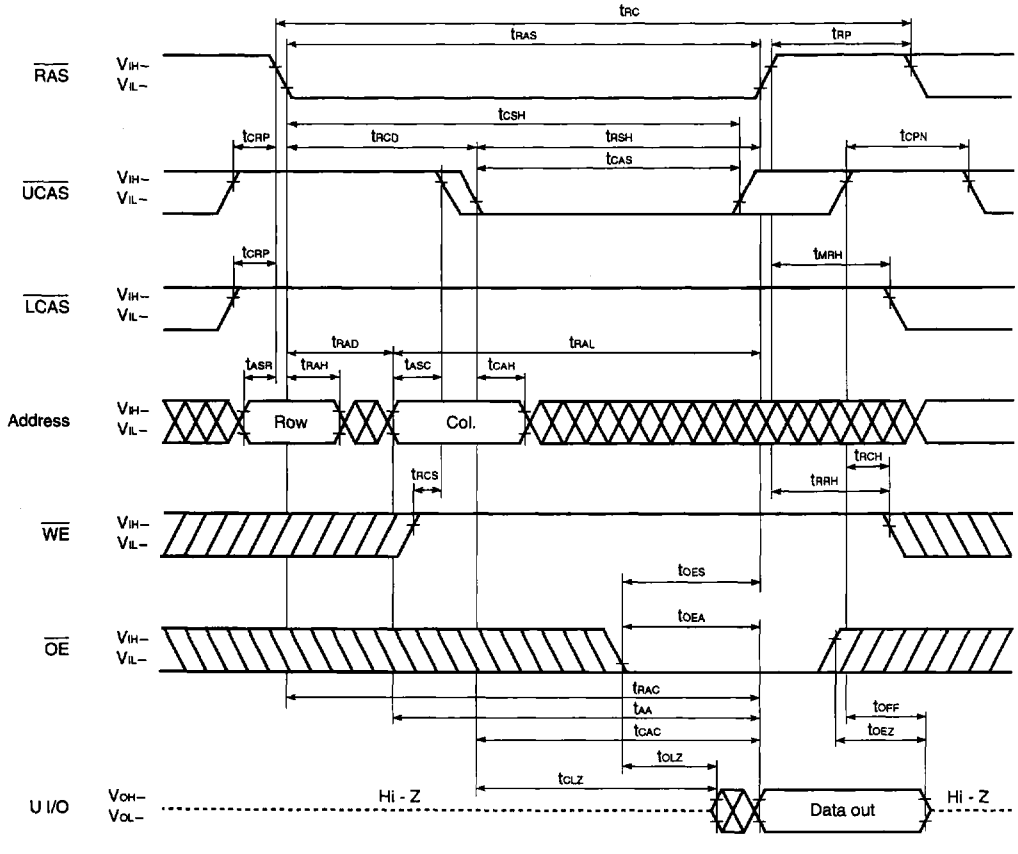
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ Setup Time	t_{CSR}	5	–	5	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5	–	5	–	ns	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh Cycle)	t_{RASS}	100	–	100	–	μs	1
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh Cycle)	t_{RPS}	110	–	130	–	ns	1
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh Cycle)	t_{CHS}	-50	–	-50	–	ns	1
$\overline{WE}$ Hold Time (Hidden Refresh Cycle)	t_{WHR}	15	–	15	–	ns	

Note 1. This specification is applied only to the μPD42S16160L, 42S18160L.

Read Cycle

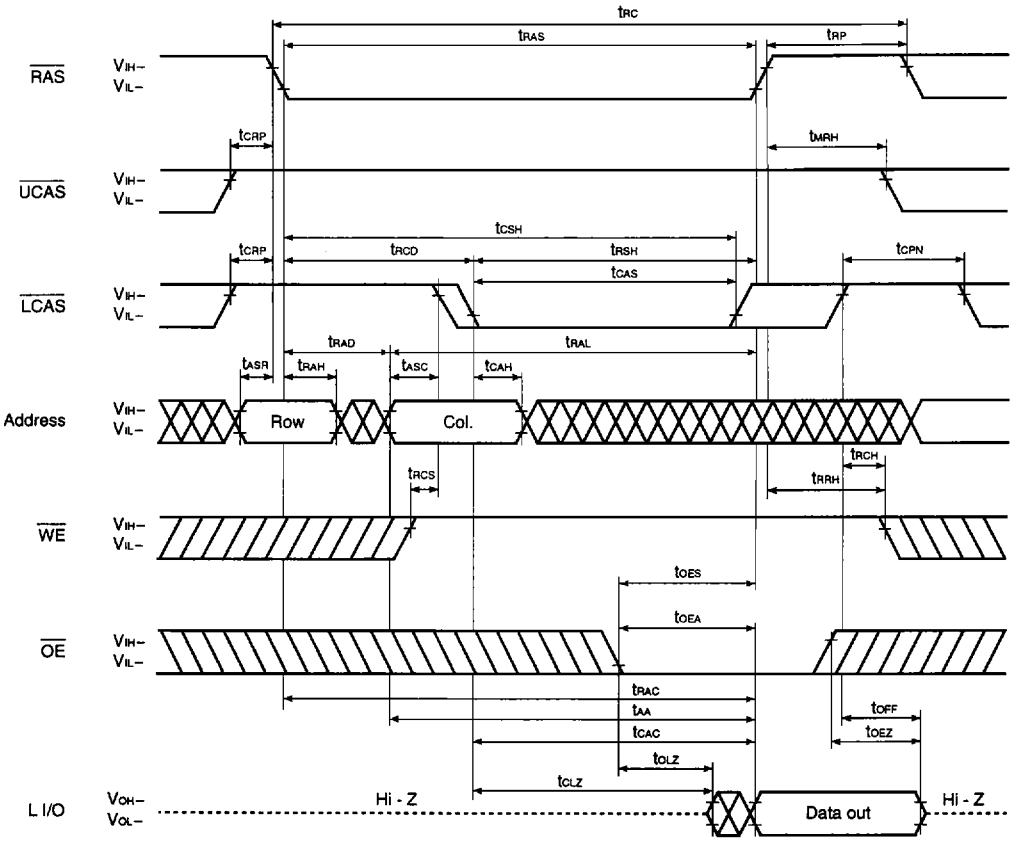

tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCAS
tCPN
UCAS
LCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
WE
tOES
tOEA
OE
tRAC
tAA
tOFF
tCAC
tOEZ
tOLZ
tCLZ
U I/O
L I/O
VOH–
VOL–
Hi - Z
Data out
Hi - Z

Upper Byte Read Cycle



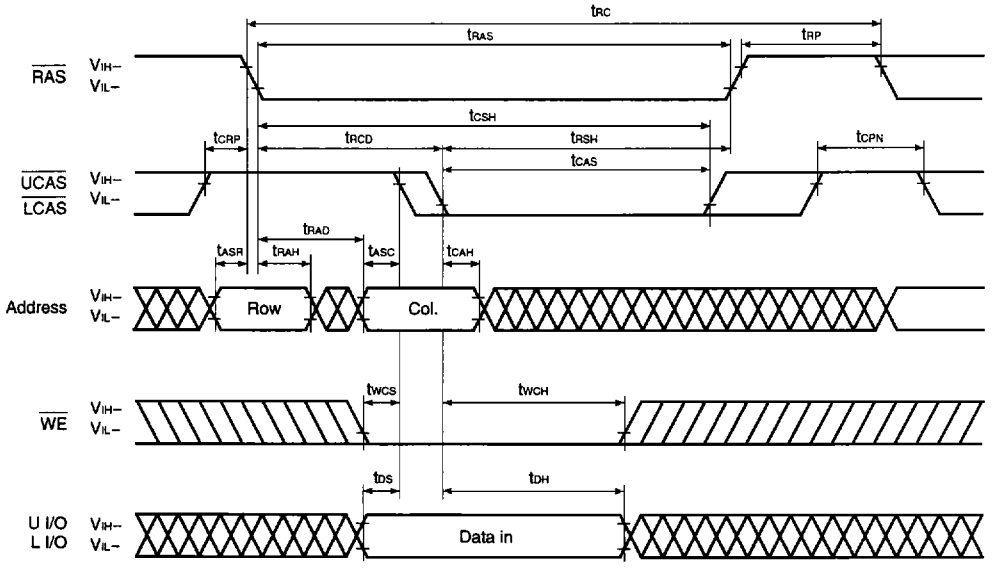
Remark L I/O : Hi-Z

Lower Byte Read Cycle



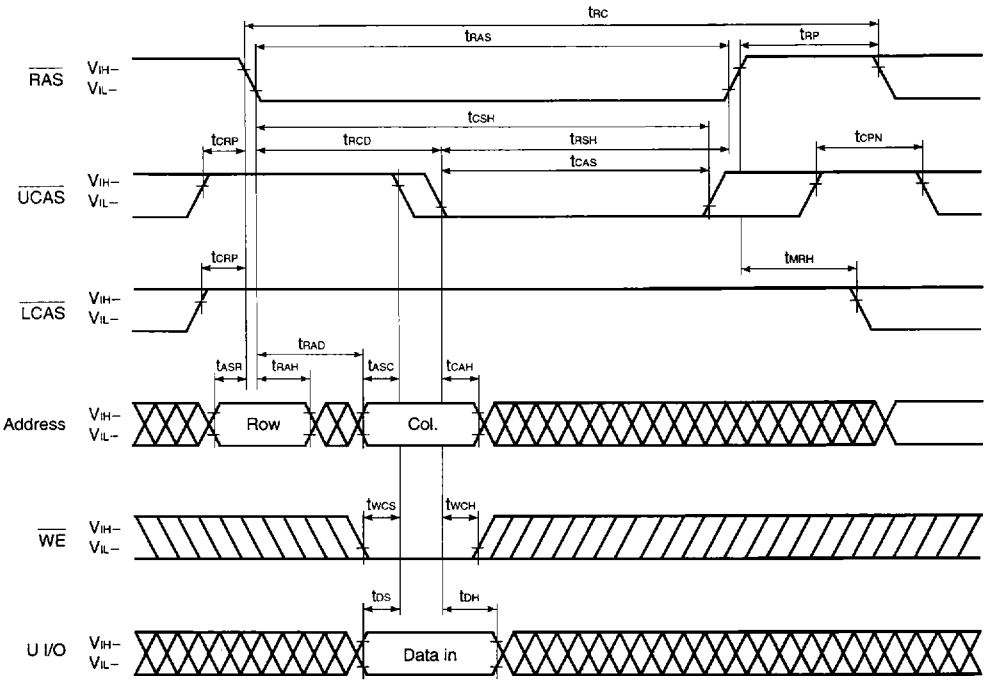
Remark U I/O : Hi-Z

Early Write Cycle



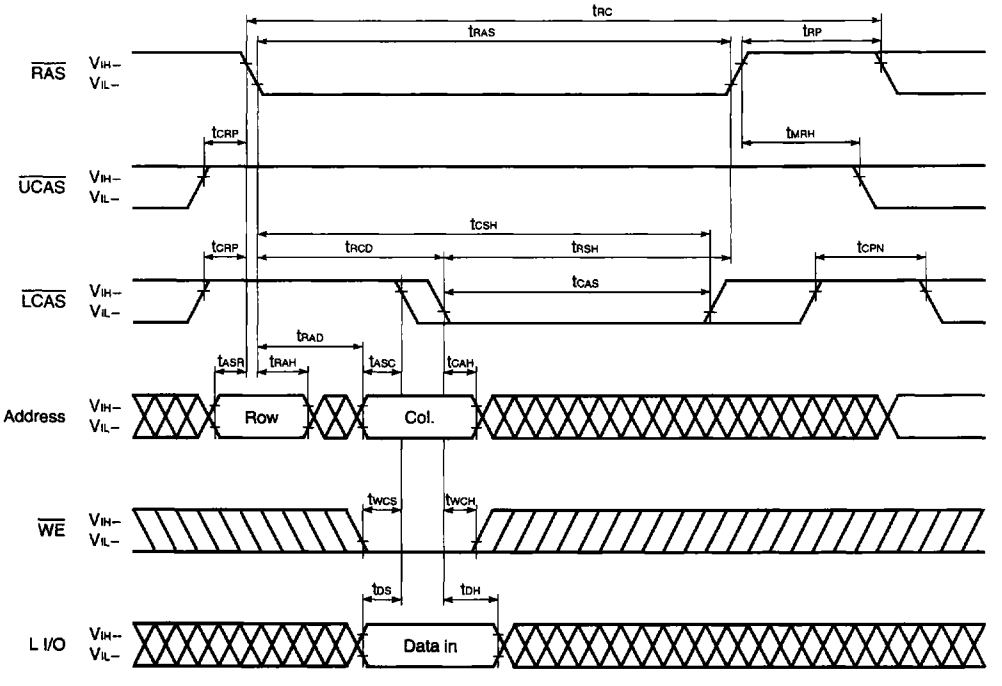
Remark $\overline{OE}$: Don't care

Upper Byte Early Write Cycle



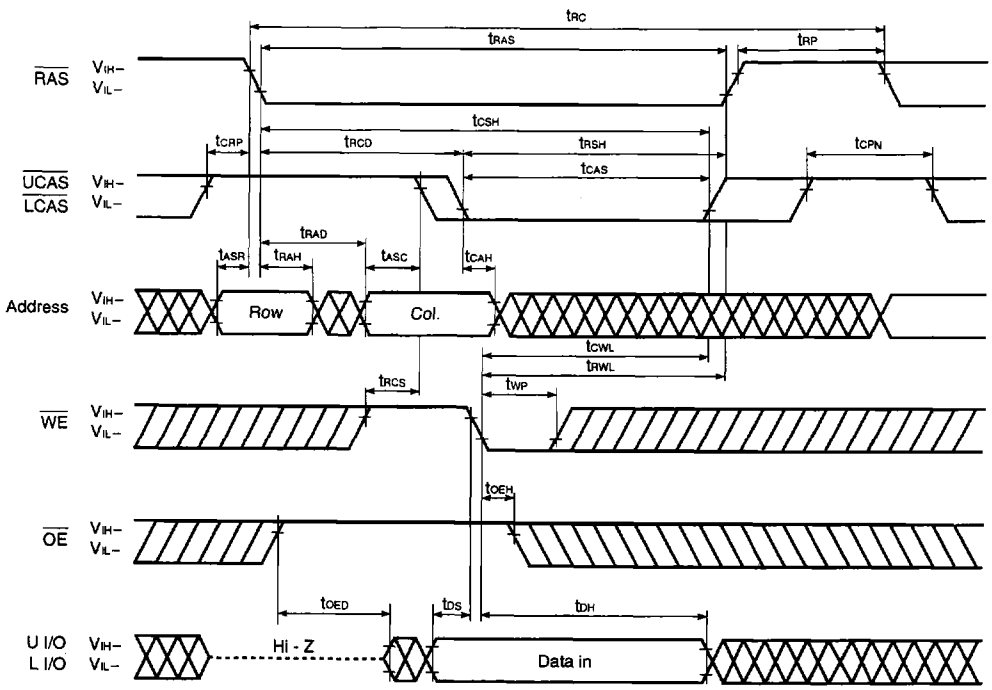
Remark $\overline{OE}$, L I/O : Don't care

Lower Byte Early Write Cycle

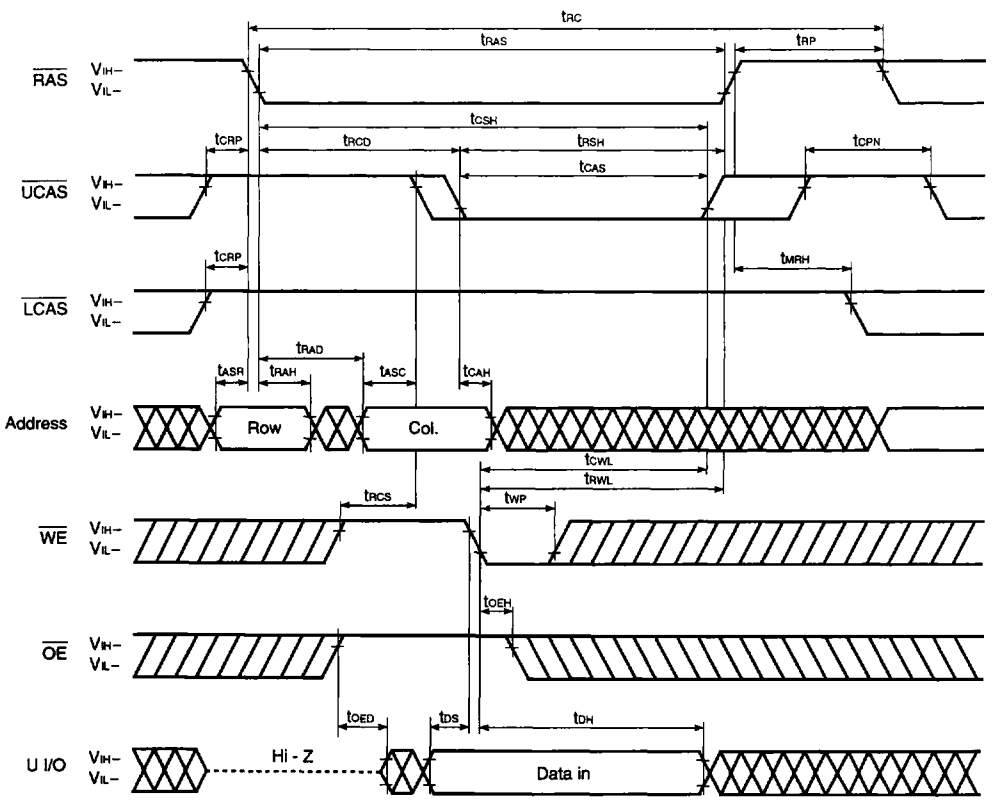


Remark $\overline{OE}$, U I/O : Don't care

Late Write Cycle

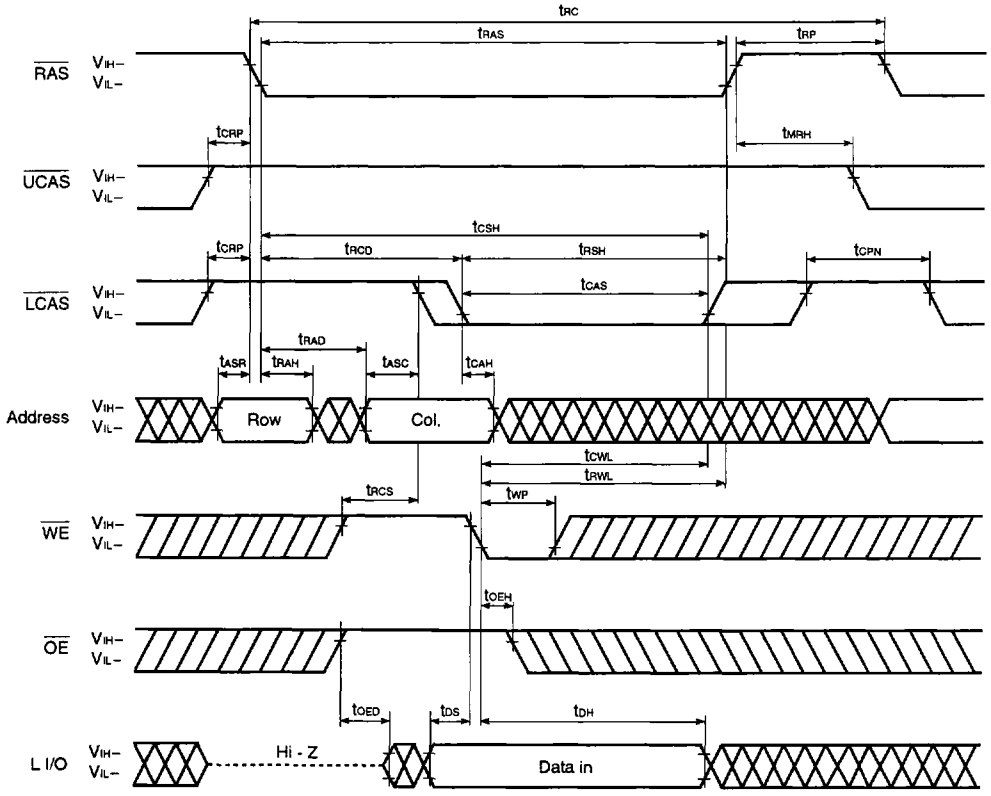


Upper Byte Late Write Cycle



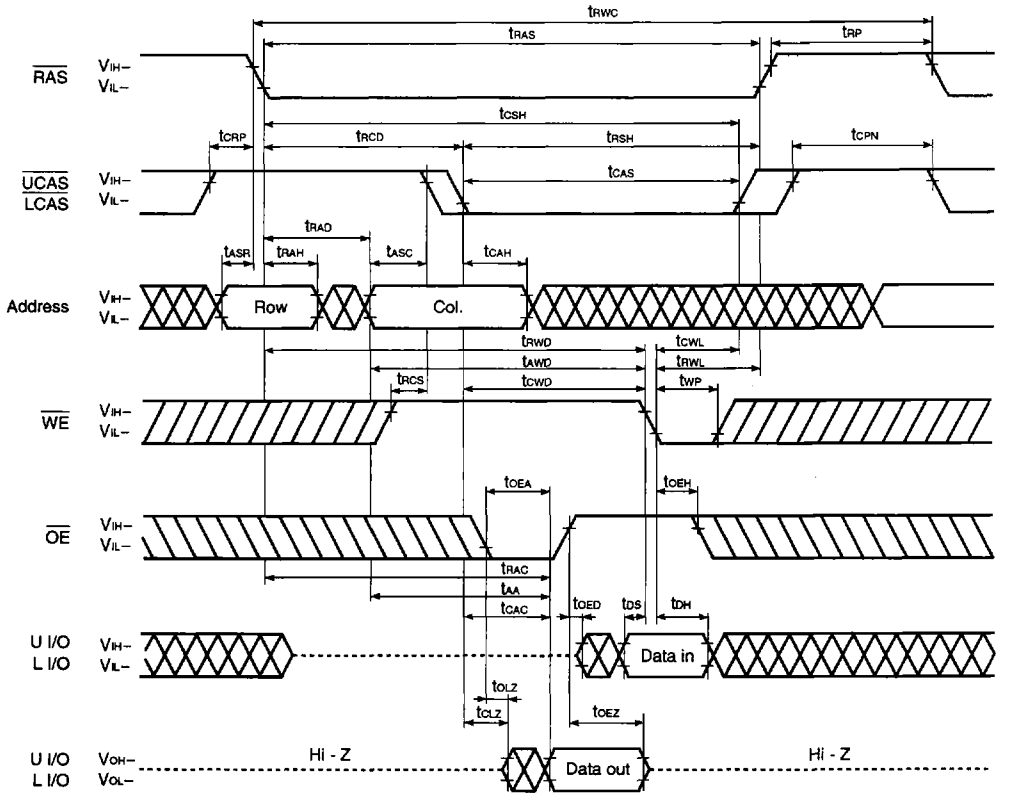
Remark L I/O : Don't care

Lower Byte Late Write Cycle

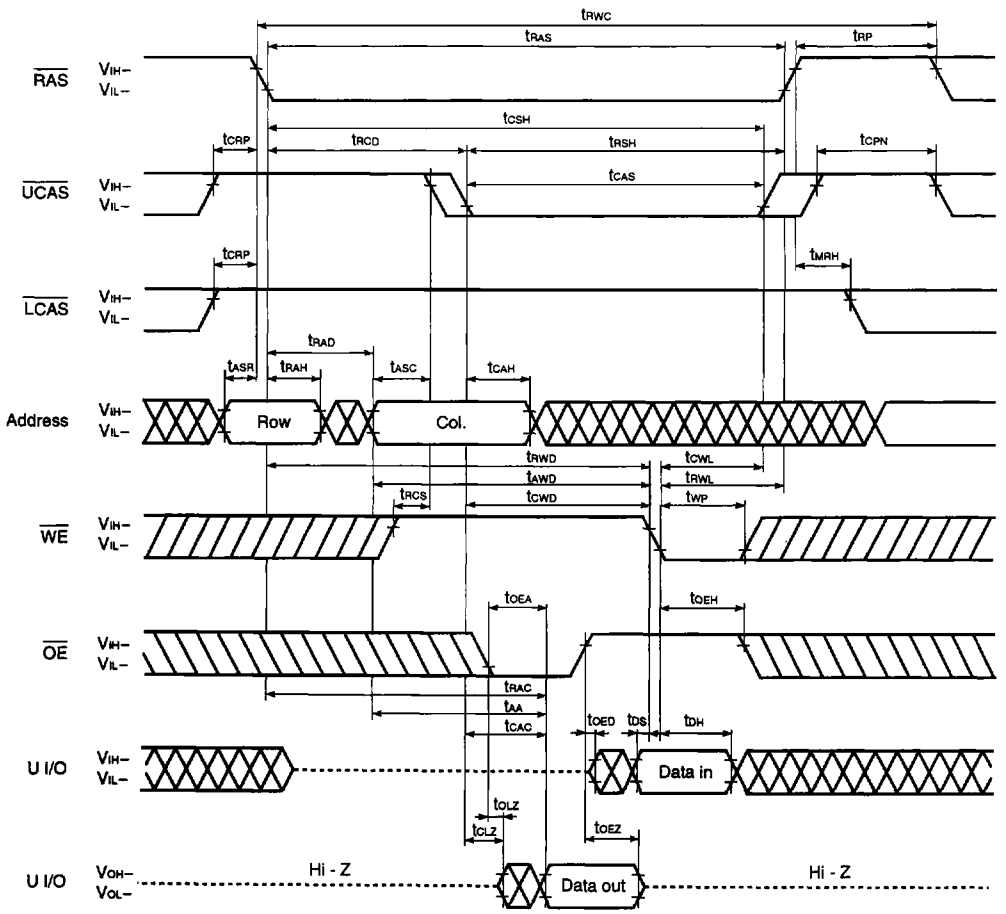


Remark U I/O : Don't care

Read Modify Write Cycle

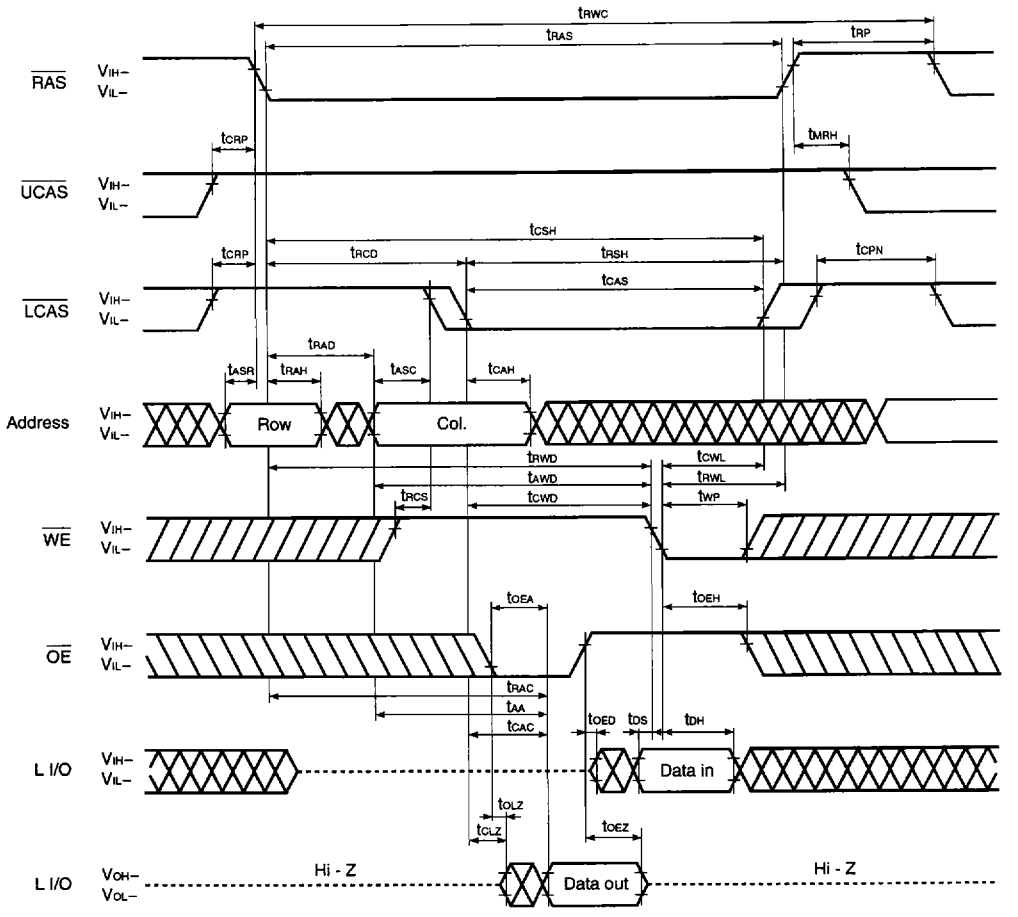


Upper Byte Read Modify Write Cycle



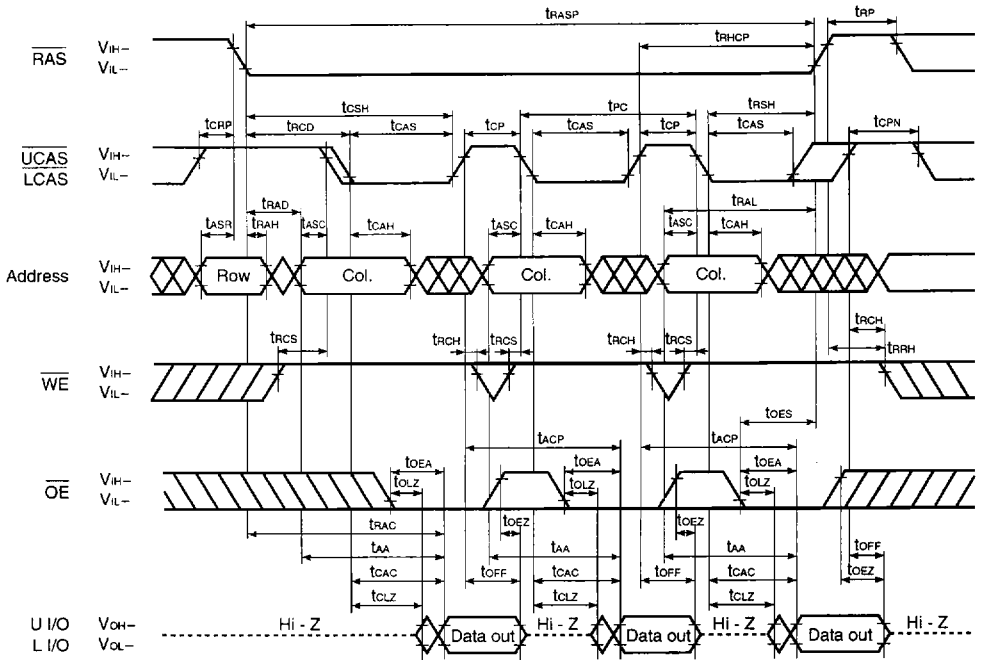
Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

Lower Byte Read Modify Write Cycle



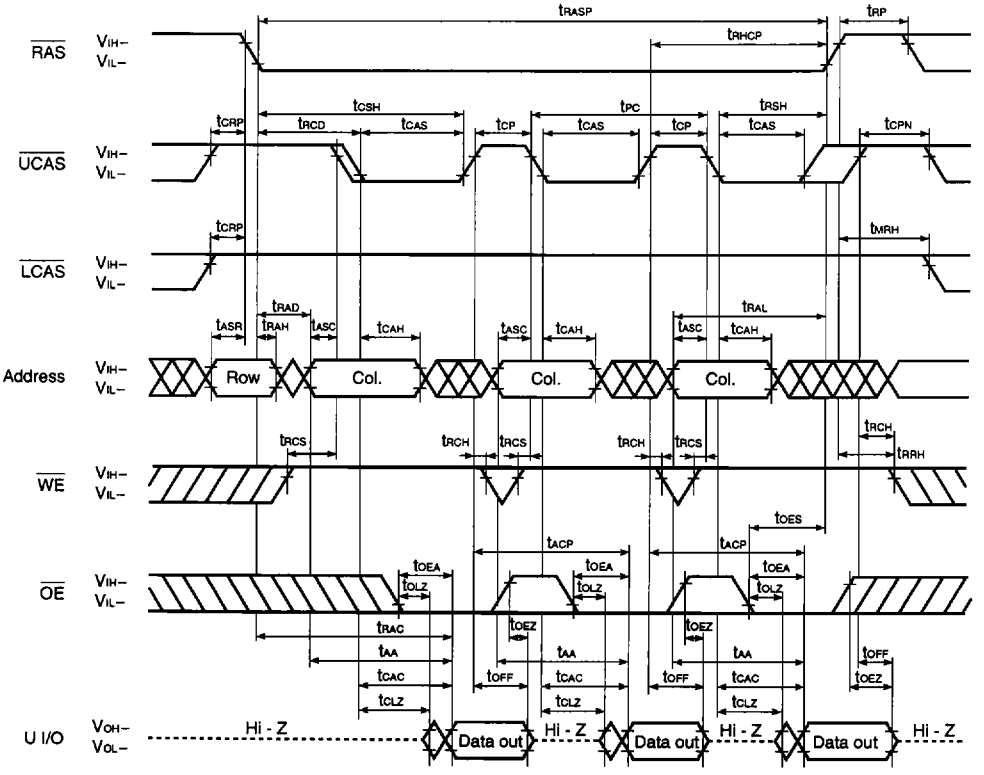
Remark In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

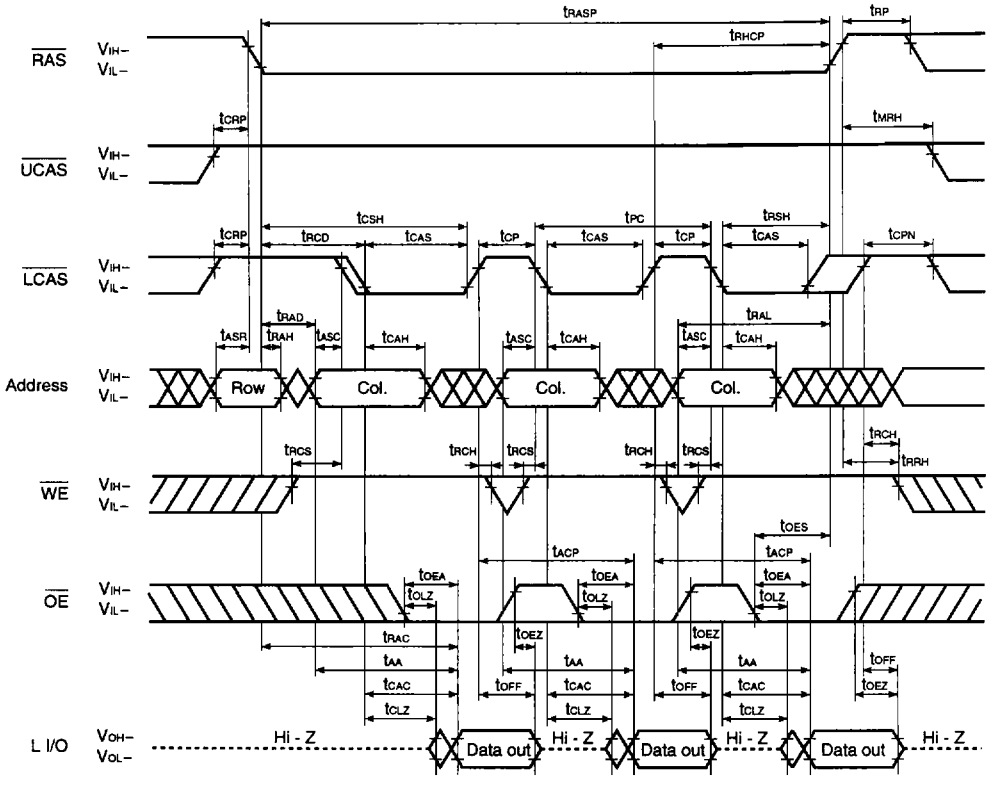
Fast Page Mode Upper Byte Read Cycle



Remark L I/O : Hi-Z

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

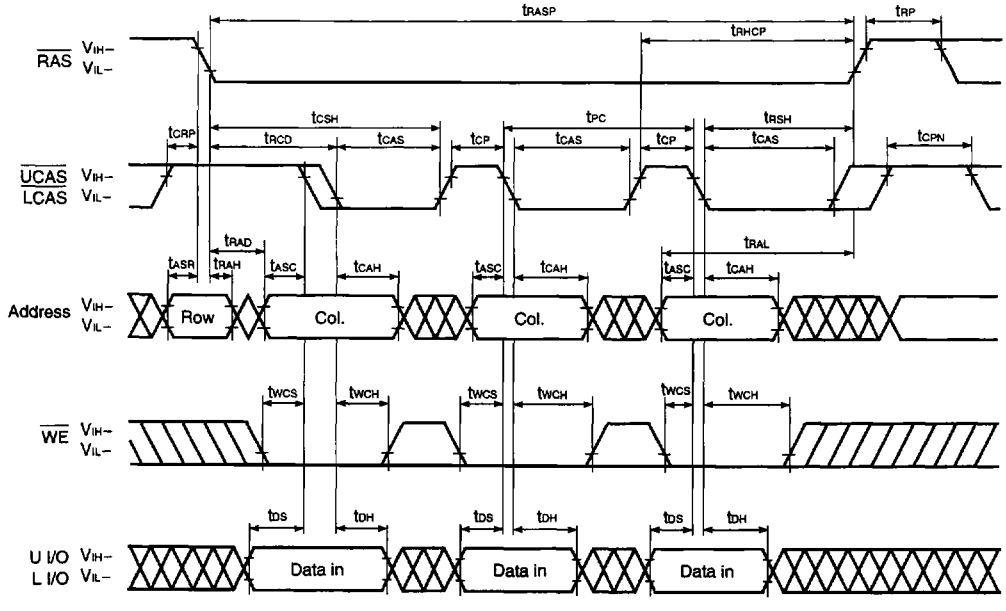
Fast Page Mode Lower Byte Read Cycle



Remark U I/O : Hi-Z

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

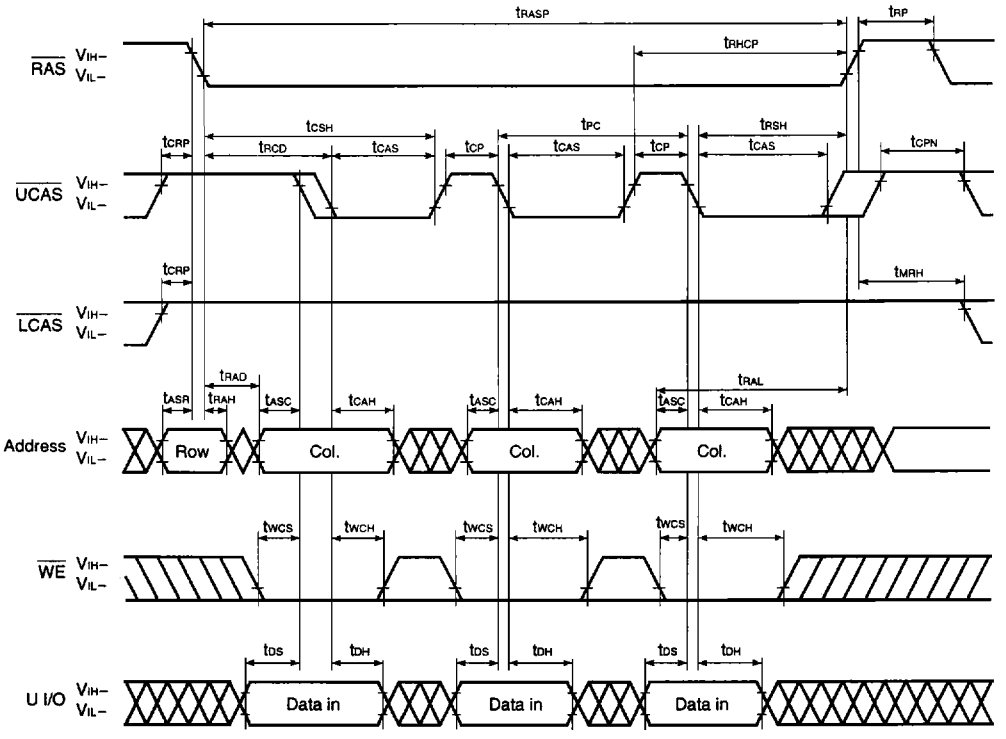
Fast Page Mode Early Write Cycle



Remark $\overline{OE}$: Don't care

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

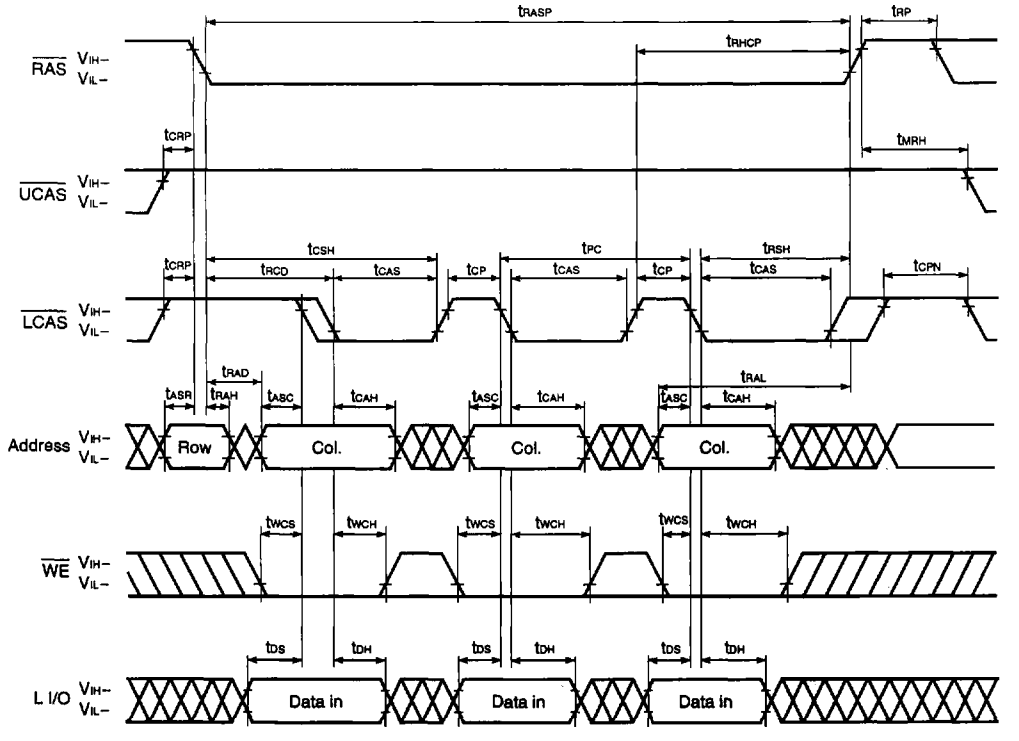
Fast Page Mode Upper Byte Early Write Cycle



Remark $\overline{OE}$, L I/O : Don't care

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

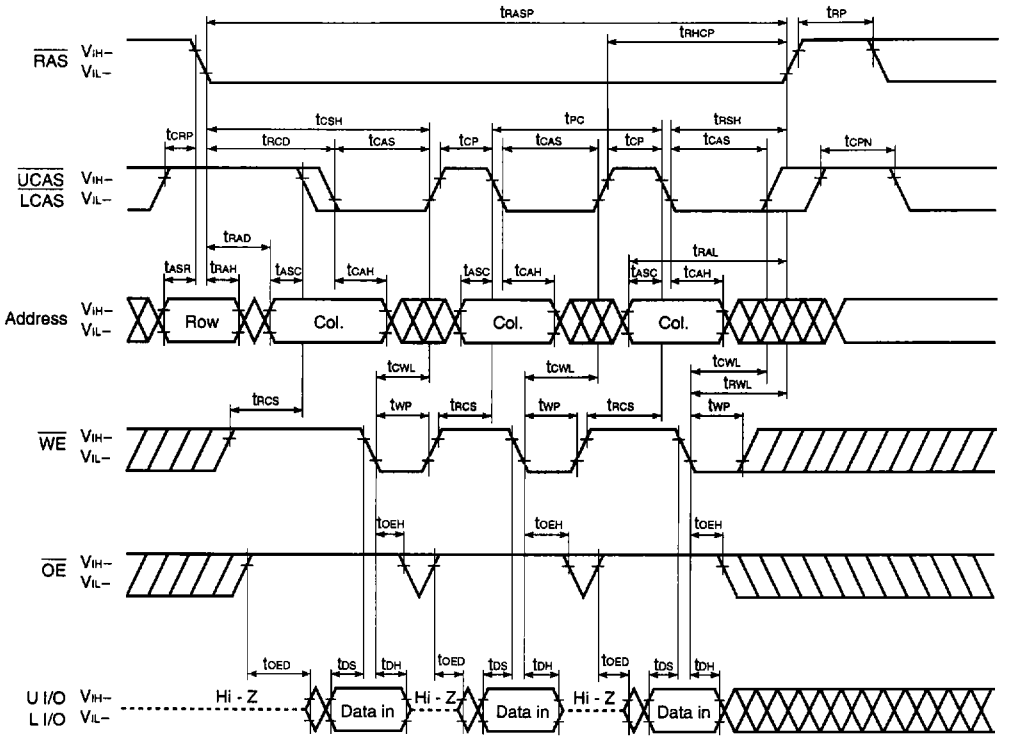
Fast Page Mode Lower Byte Early Write Cycle



Remark $\overline{OE}$, U I/O : Don't care

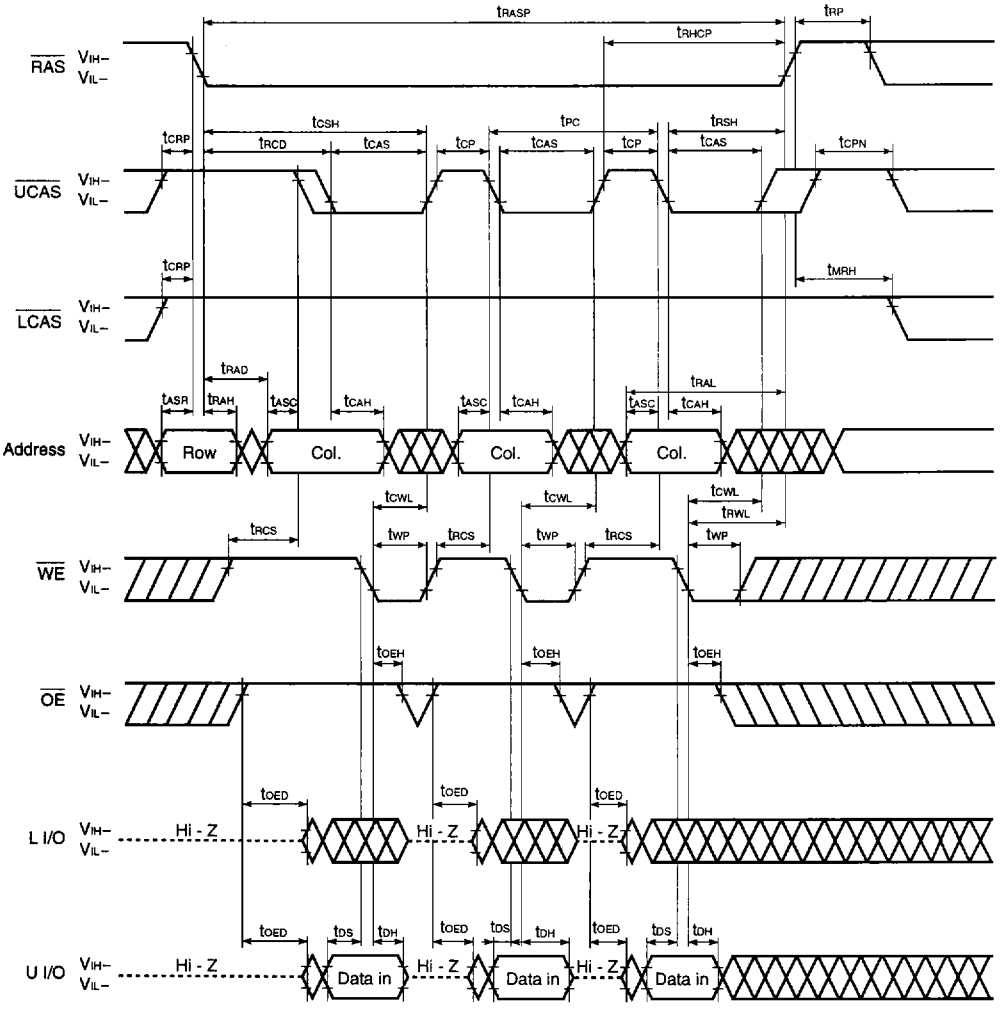
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Late Write Cycle



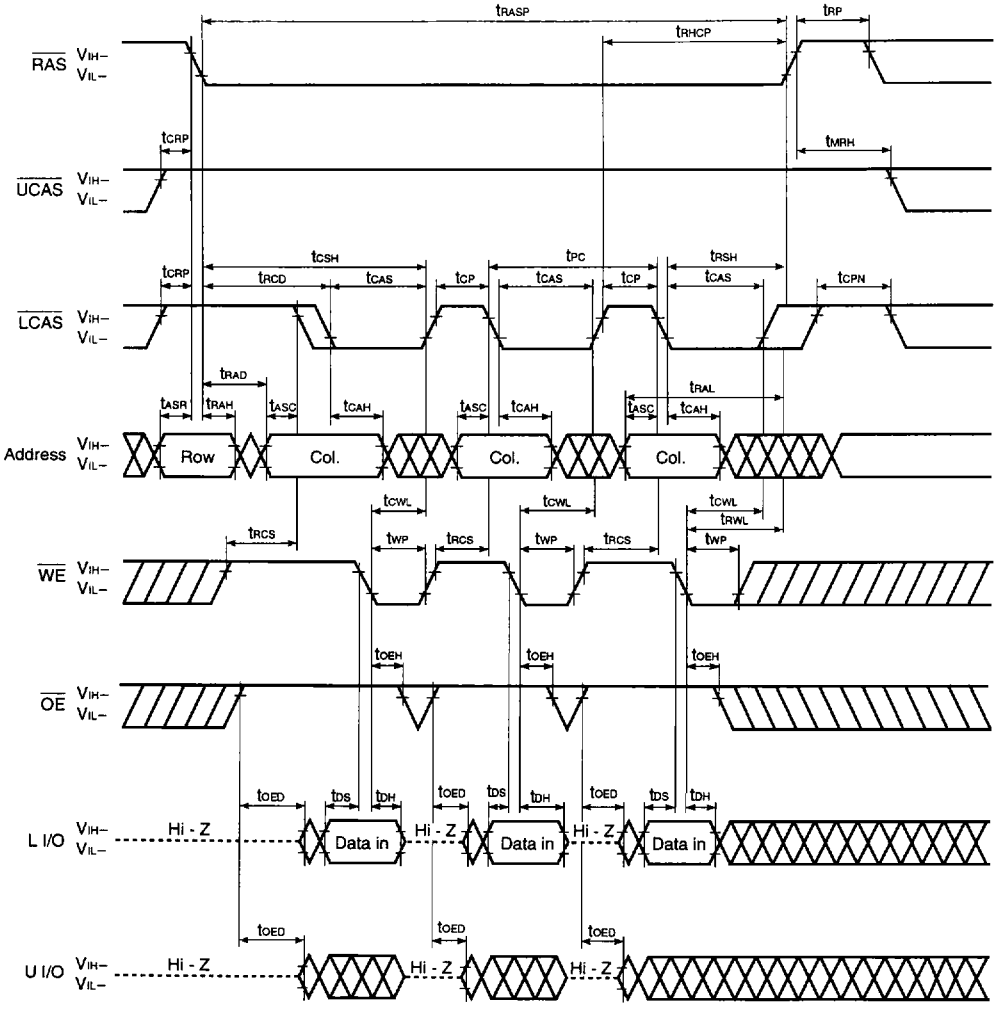
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Upper Byte Late Write Cycle



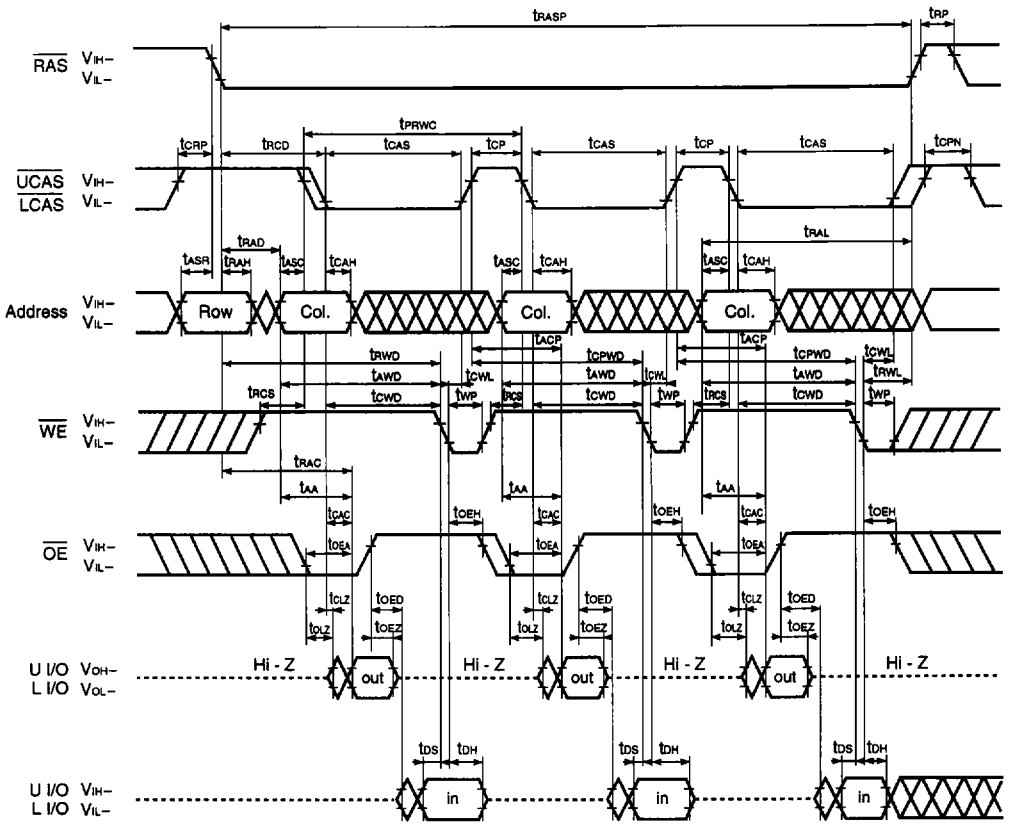
Remark In this cycle, the input data to Lower I/O is ineffective.
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Lower Byte Late Write Cycle



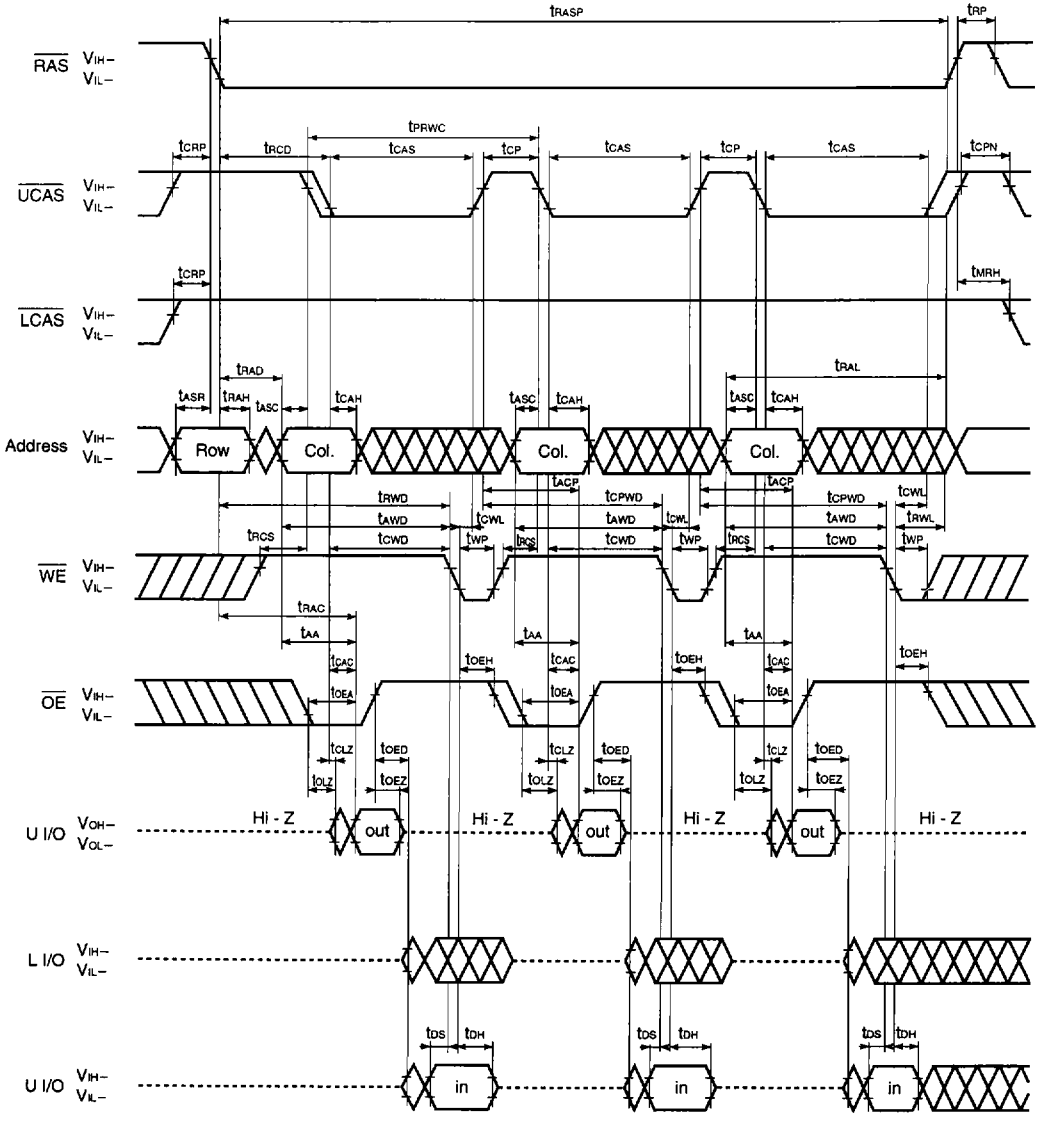
Remark In this cycle, the input data to Upper I/O is ineffective.
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Read Modify Write Cycle



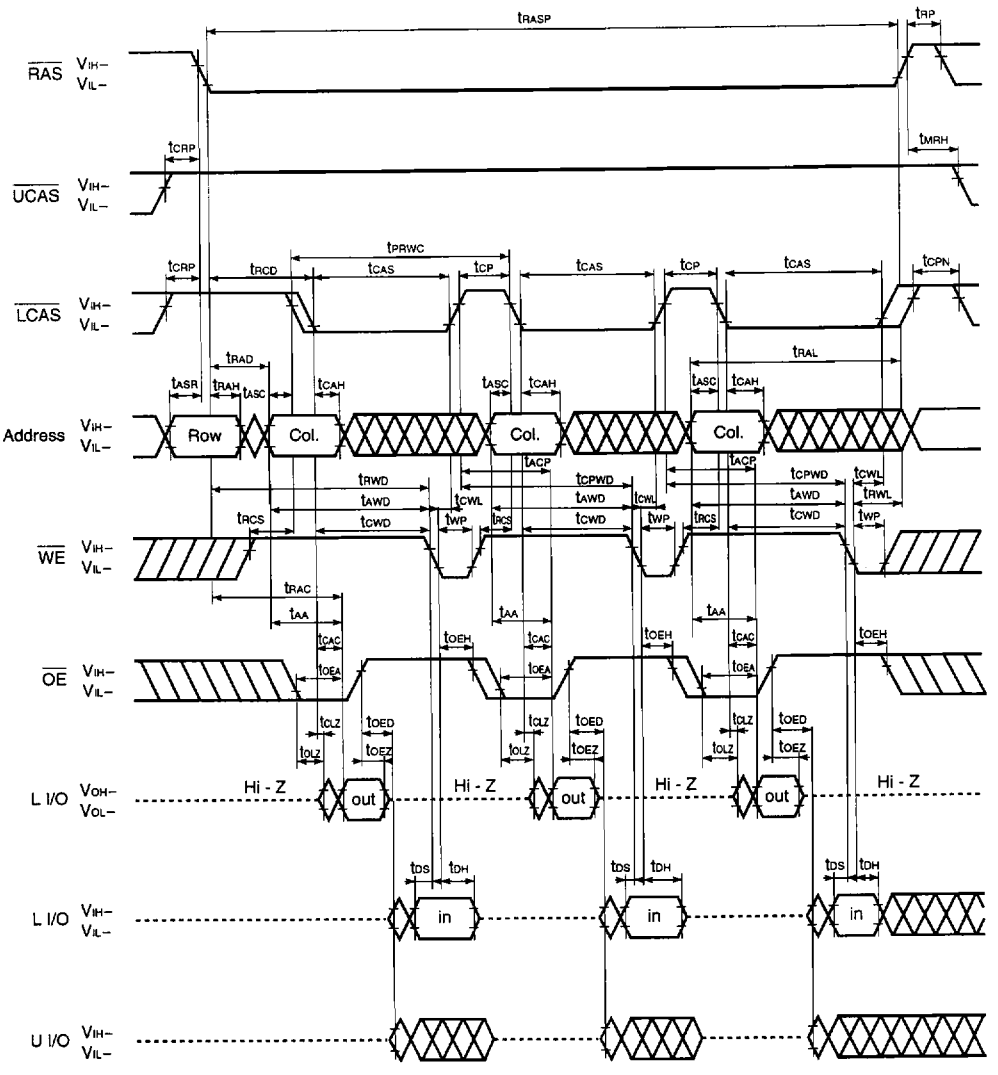
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Upper Byte Read Modify Write Cycle



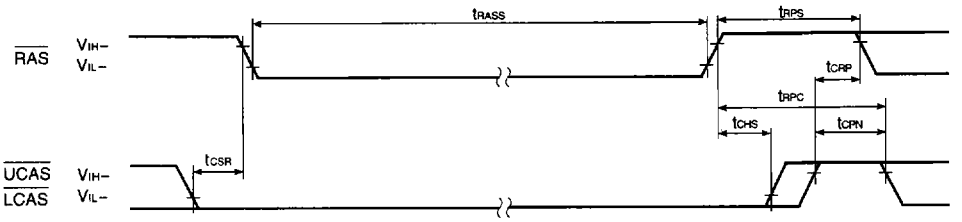
Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Lower Byte Read Modify Write Cycle



Remark In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S16160L, 42S18160L)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O : Hi - Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with burst long $\overline{RAS}$ only refresh, the following cautions must be observed.

(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

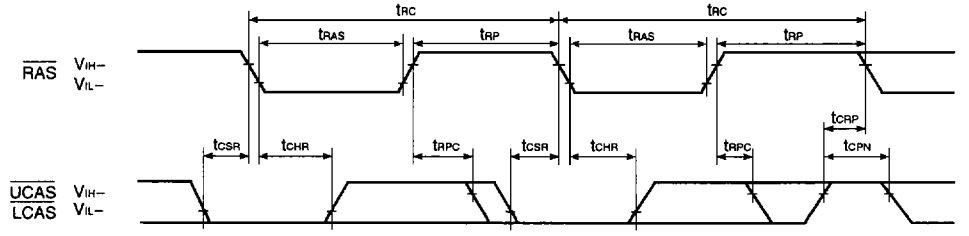
μPD42S16160L : 4 096 times within a 64 ms interval
μPD42S18160L : 1 024 times within a 16 ms interval

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

μPD42S16160L : 4 096 times within a 64 ms interval
μPD42S18160L : 1 024 times within a 16 ms interval

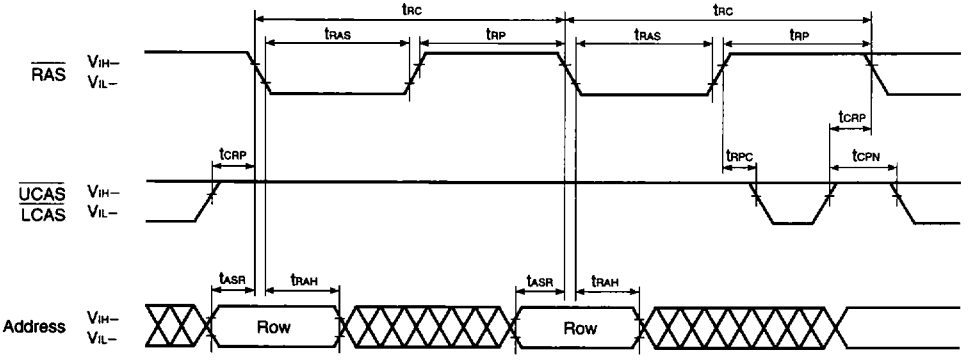
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



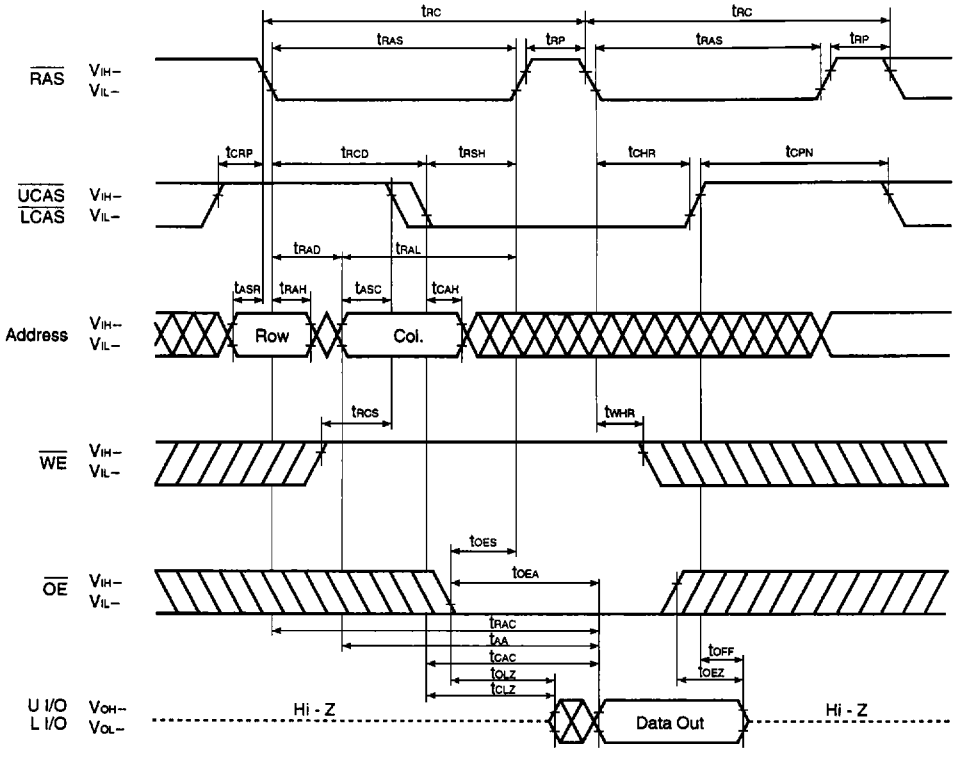
Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O : Hi - Z

$\overline{RAS}$ Only Refresh Cycle

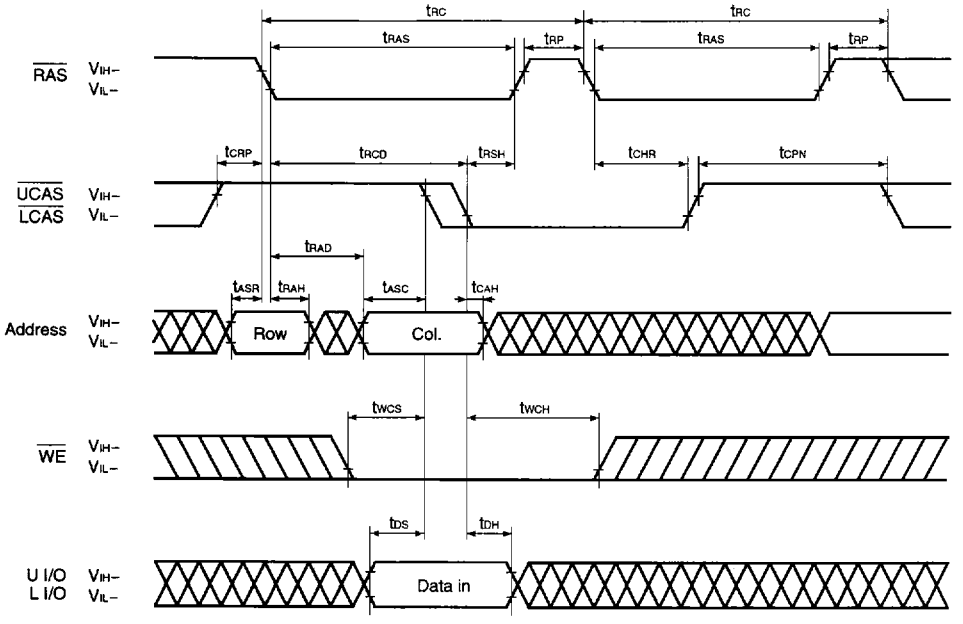


Remark $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O : Hi - Z

Hidden Refresh Cycle (Read)



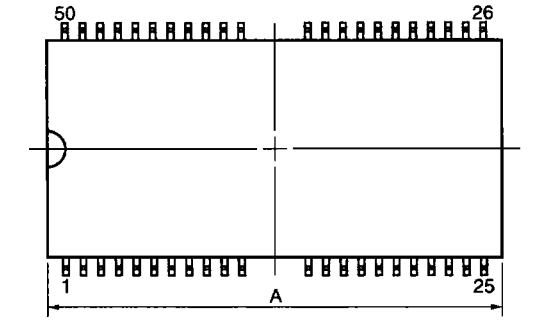
Hidden Refresh Cycle (Write)



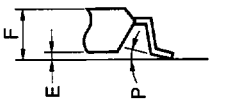
Remark $\overline{OE}$: Don't care

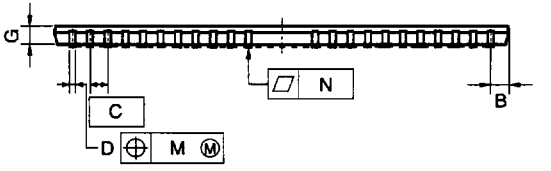
Package Drawings

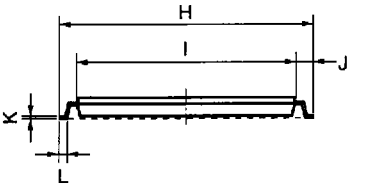
50 PIN PLASTIC TSOP (II) (400 mil)



detail of lead end







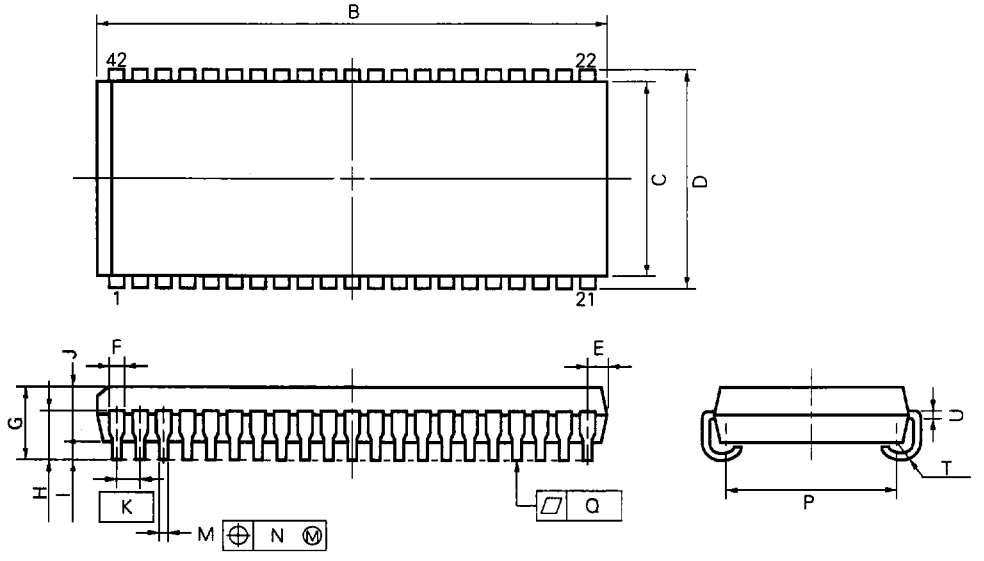
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A*	21.17 MAX.	0.834 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.13	0.005
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S50G5-80-7JF4

42 PIN PLASTIC SOJ (400 mil)



P42LE-400A

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$27.56^{+0.2}_{-0.35}$	$1.085^{+0.008}_{-0.014}$
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.08±0.15	$0.043^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met when soldering μPD42S16160L, 4216160L, 42S18160L, 4218160L.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S16160LG5, 4216160LG5, 42S18160LG5, 4218160LG5 : 50-pin plastic TSOP (II) (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time : 30 seconds or below (210 °C or higher), Number of reflow processes : MAX. 2 Exposure limit [Note] : 7 days (10 hours pre-baking is required at 125 °C afterwards) **[Remark]** (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	IR35-107-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes : MAX. 2 Exposure limit[Note] : 7 days (10 hours pre-baking is required at 125 °C afterwards) **[Remark]** (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	VP15-107-2
Partial heating method	Terminal temperature : 300 °C or below, Time : 3 seconds or below (Per one side of the device).	———

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD42S16160LLE, 4216160LLE, 42S18160LLE, 4218160LLE : 42-pin plastic SOJ (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time : 30 seconds or below (210 °C or higher), Number of reflow processes : MAX. 2 Exposure limit[Note] : 7 days (20 hours pre-baking is required at 125 °C afterwards) **[Remark]** (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	IR35-207-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes : MAX. 2 Exposure limit[Note] : 7 days (20 hours pre-baking is required at 125 °C afterwards) **[Remark]** (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	VP15-207-2
Partial heating method	Terminal temperature : 300 °C or below, Time : 3 seconds or below (Per one side of the device).	———

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".