

# SN54LVC74A, SN74LVC74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

SCAS287H – JANUARY 1993 – REVISED JUNE 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$**
- **Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) > 2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$**
- **Inputs Accept Voltages to 5.5 V**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and DIPs (J)**

## description

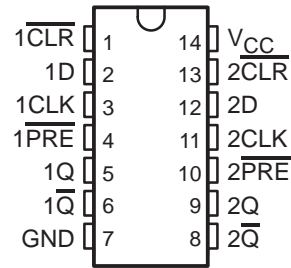
The SN54LVC74A dual positive-edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V  $V_{CC}$  operation and the SN74LVC74A dual positive-edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

A low level at the preset ( $\overline{\text{PRE}}$ ) or clear ( $\overline{\text{CLR}}$ ) inputs sets or resets the outputs, regardless of the levels of the other inputs. When  $\overline{\text{PRE}}$  and  $\overline{\text{CLR}}$  are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

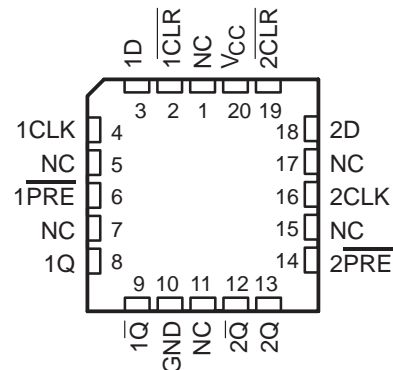
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN54LVC74A is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74LVC74A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54LVC74A . . . J OR W PACKAGE  
SN74LVC74A . . . D, DB, OR PW PACKAGE  
(TOP VIEW)



SN54LVC74A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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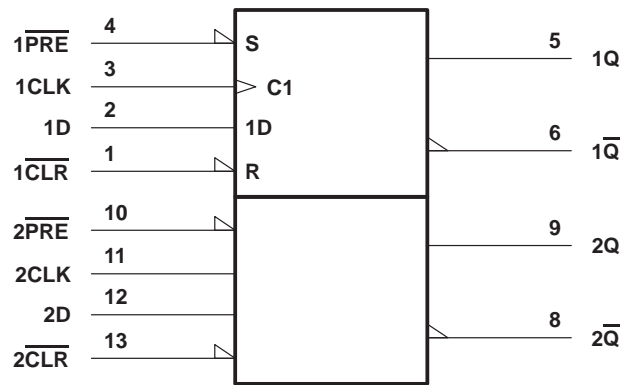
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FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H <sup>†</sup>	H <sup>†</sup>
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q <sub>0</sub>	$\overline{\text{Q}}_0$

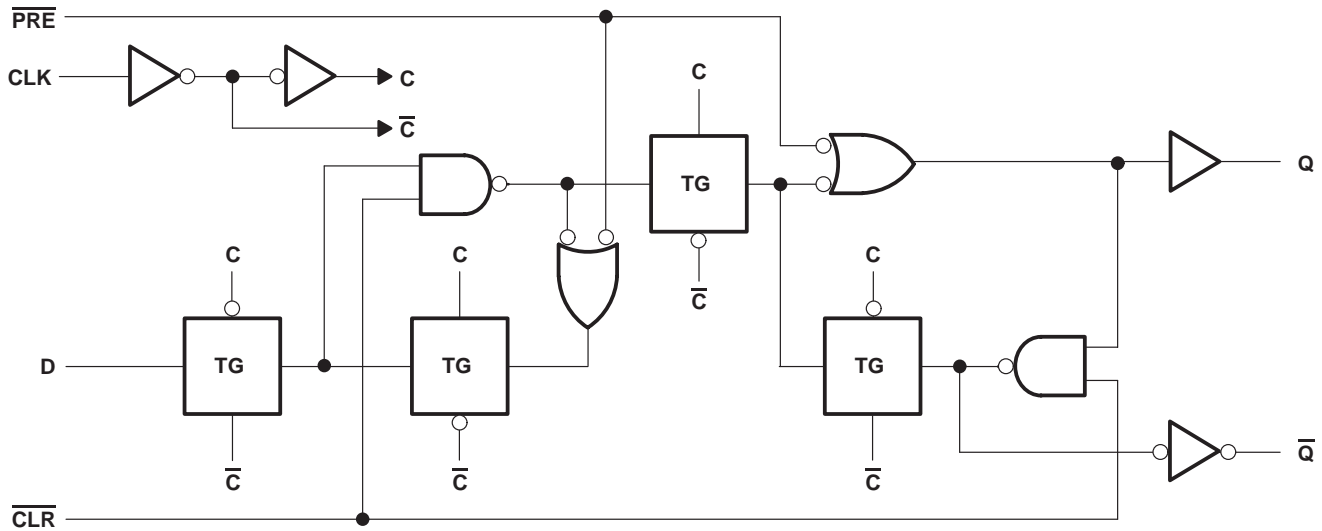
† This configuration is unstable; that is, it does not persist when  $\overline{\text{PRE}}$  or  $\overline{\text{CLR}}$  returns to its inactive (high) level.

## logic symbol<sup>‡</sup>



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, J, PW, and W packages.

## logic diagram, each flip-flop (positive logic)



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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply-voltage range, $V_{CC}$ .....	–0.5 V to 6.5 V
Input-voltage range, $V_I$ (see Note 1) .....	–0.5 V to 6.5 V
Output-voltage range, $V_O$ (see Notes 1 and 2) .....	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	–50 mA
Continuous output current, $I_O$ .....	±50 mA
Continuous current through $V_{CC}$ or GND .....	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package .....	127°C/W
DB package .....	158°C/W
PW package .....	170°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The value of  $V_{CC}$  is provided in the recommended operating conditions table.  
 3. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 4)

		SN54LVC74A		SN74LVC74A		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	Operating		2	3.6	V
		Data retention only		1.5	1.5	
$V_{IH}$	High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V		$0.65 \times V_{CC}$		V
		$V_{CC} = 2.3$ V to 2.7 V		1.7		
		$V_{CC} = 2.7$ V to 3.6 V		2	2	
$V_{IL}$	Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V		$0.35 \times V_{CC}$		V
		$V_{CC} = 2.3$ V to 2.7 V		0.7		
		$V_{CC} = 2.7$ V to 3.6 V		0.8	0.8	
$V_I$	Input voltage	0	5.5	0	5.5	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 1.65$ V		–4		mA
		$V_{CC} = 2.3$ V		–8		
		$V_{CC} = 2.7$ V		–12	–12	
		$V_{CC} = 3$ V		–24	–24	
$I_{OL}$	Low-level output current	$V_{CC} = 1.65$ V		4		mA
		$V_{CC} = 2.3$ V		8		
		$V_{CC} = 2.7$ V		12	12	
		$V_{CC} = 3$ V		24	24	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LVC74A			SN74LVC74A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V				V <sub>CC</sub> -0.2			V
		2.7 V to 3.6 V	V <sub>CC</sub> -0.2						
	I <sub>OH</sub> = -4 mA	1.65 V			1.2				
	I <sub>OH</sub> = -8 mA	2.3 V			1.7				
	I <sub>OH</sub> = -12 mA	2.7 V	2.2		2.2				
		3 V	2.4		2.4				
I <sub>OH</sub> = -24 mA	3 V	2.2		2.2					
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V				0.2			V
		2.7 V to 3.6 V			0.2				
	I <sub>OL</sub> = 4 mA	1.65 V				0.45			
	I <sub>OL</sub> = 8 mA	2.3 V				0.7			
	I <sub>OL</sub> = 12 mA	2.7 V			0.4		0.4		
3 V				0.55		0.55			
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	3.6 V			±5			±5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V			10			10	μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V			500			500	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V			5			5	pF

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

		SN54LVC74A				UNIT
		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		
		MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency		83		100	MHz
t <sub>w</sub>	Pulse duration	PRE or CLR low		3.3	3.3	ns
		CLK high or low		3.3	3.3	
t <sub>su</sub>	Setup time before CLK↑	Data		3.4	3	ns
		PRE or CLR inactive		2.2	2	
t <sub>h</sub>	Hold time, data after CLK↑		1		1	ns



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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			SN74LVC74A								UNIT
			$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency		†		†			83		100	MHz
$t_w$	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	†		†			3.3		3.3	ns
		CLK high or low	†		†			3.3		3.3	
$t_{\text{su}}$	Setup time before CLK↑	Data	†		†			3.4		3	ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	†		†			2.2		2	
$t_h$	Hold time, data after CLK↑		†		†			1		0	ns

† This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC74A				UNIT	
			$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			
			MIN	MAX	MIN	MAX		
$f_{\text{max}}$				83		100	MHz	
$t_{\text{pd}}$	CLK	Q or $\overline{Q}$		6		1	5.2	ns
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$			6.4		1	5.4	

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC74A								UNIT	
			$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$f_{\text{max}}$			†		†			83		100	MHz	
$t_{\text{pd}}$	CLK	Q or $\overline{Q}$	†	†	†	†		6		1	5.2	ns
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$		†	†	†	†		6.4		1	5.4	
$t_{\text{sk}(o)}^\ddagger$										1	ns	

† This information was not available at the time of publication.

‡ Skew between any two outputs of the same package switching in the same direction

operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	UNIT	
		TYP	TYP	TYP		
$C_{\text{pd}}$	Power dissipation capacitance per flip-flop	$f = 10\text{ MHz}$	†	†	27	pF

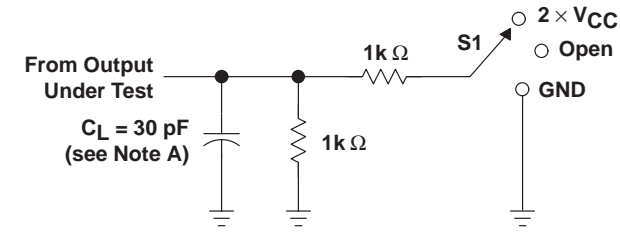
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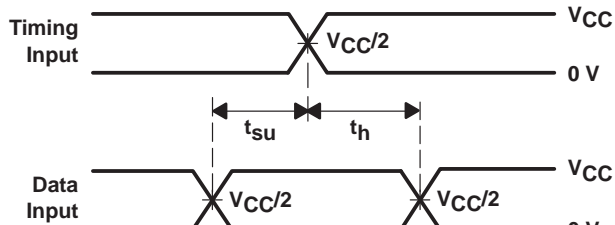
## PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

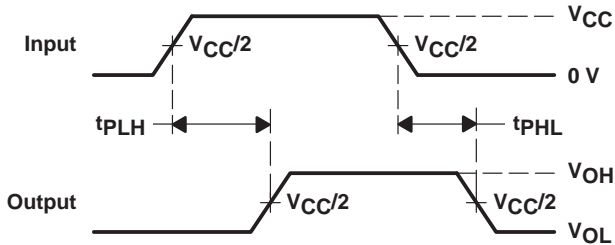


LOAD CIRCUIT

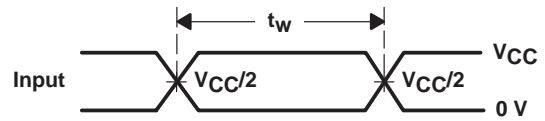
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	Open



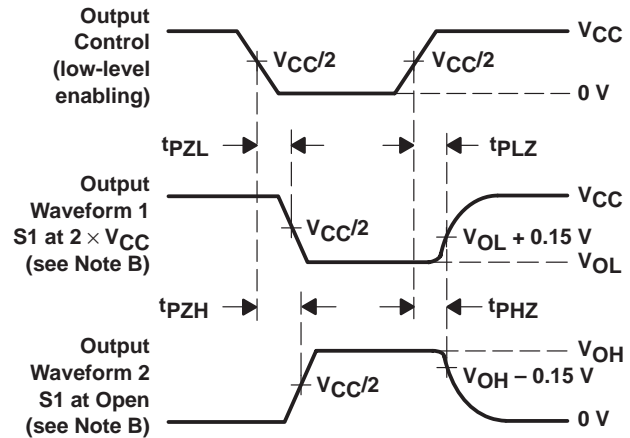
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

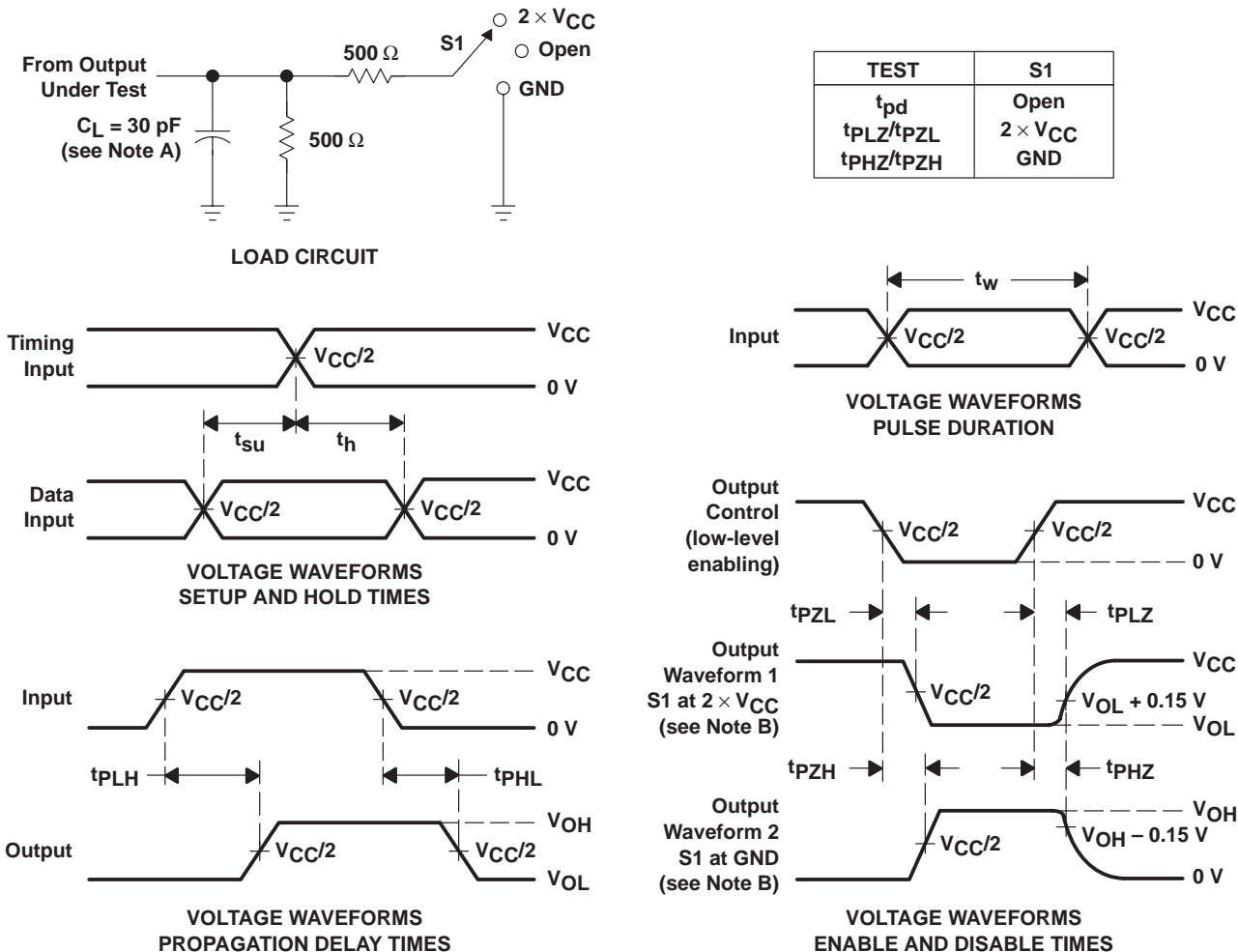
Figure 1. Load Circuit and Voltage Waveforms

# SN54LVC74A, SN74LVC74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

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## PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

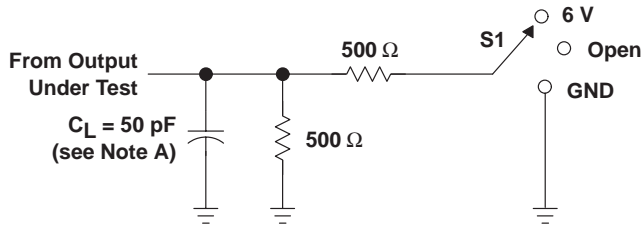
**Figure 2. Load Circuit and Voltage Waveforms**

# SN54LVC74A, SN74LVC74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

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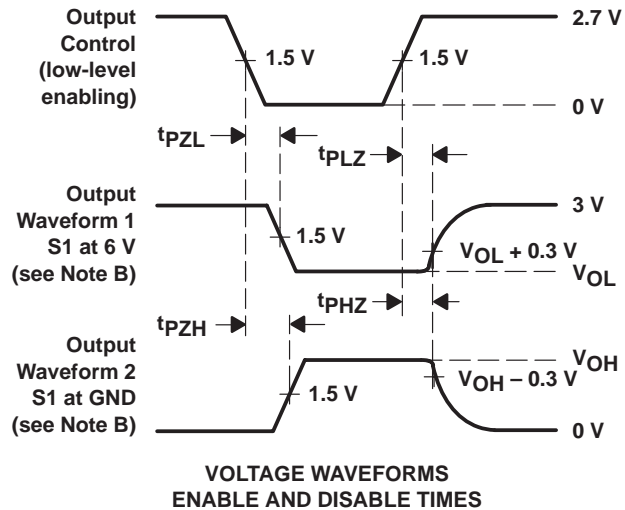
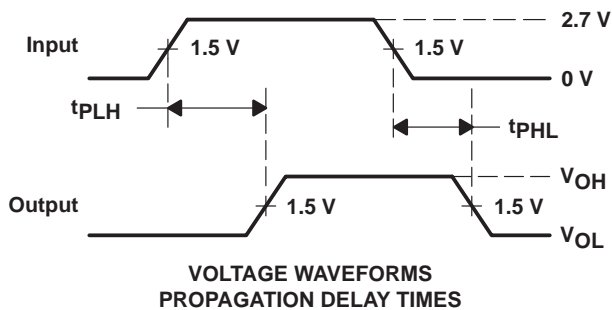
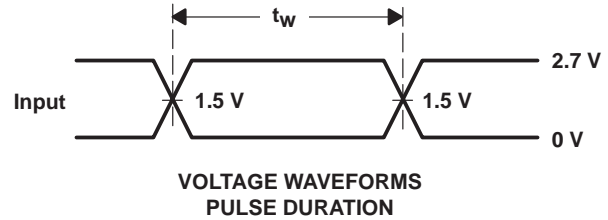
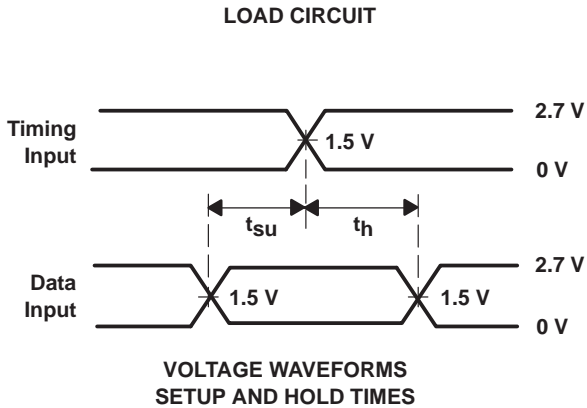
## PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



LOAD CIRCUIT

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 3. Load Circuit and Voltage Waveforms



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