Document Title

512K x8 bit Low Power and Low Voltage CMOS Static RAM

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft	August 16, 1994	Advance
0.1	Revise - Speed bin=70/85/100ns at Vcc=3.3V	December 22, 1994	Preliminary
0.2	Revise - Seperate read and write for I_{CC1}, I_{CC2} : I_{CC1}= I_{CC2} → Read=10mA and Write=20mA at Vcc=3.3V - One datasheet for commercial and industrial product.	April 15, 1996	Preliminary
1.0	Finalize - Add 85ns with 30pF part in 3.3V product.	September 19, 1996	Final
2.0	Revise - Change datasheet format - Remove 70/100ns part from KM68V4000A Family - Remove 70ns part form KM68U4000A Family	February 25, 1998	Final

512K x8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology :TFT
- Organization : 512Kx8
- Power Supply Voltage
  KM68V4000A Family : 3.0~3.6V
  KM68U4000A Family : 2.7~3.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : 32-SOP-525, 32-TSOP2-400F/R

GENERAL DESCRIPTION

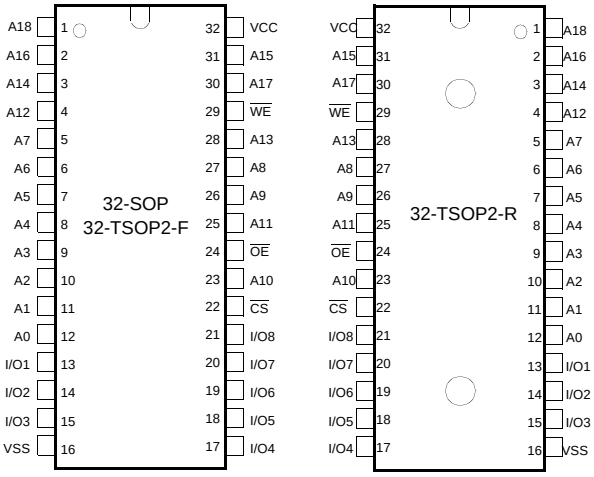
The KM68V4000A and KM68U4000A families are fabricated by SAMSUNG′s advanced CMOS process technology. The families supports various operating temperature ranges and have various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed(ns)	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max)	Operating (I_{CC2}, Max)	
KM68V4000AL KM68V4000AL-L	Commercial(0~70°C)	3.0~3.6V	85[1]	50/15µA	50mA	32-SOP 32-TSOP2-F/R
KM68V4000ALI LM68V4000ALI-L	Industrial(-40~85°C)	3.0~3.6V	85[1]	50/20µA		
KM68U4000AL KM68U4000ALI-L	Commercial(0~70°C)	2.7~3.3V	85[1]/100	30/10µA		
KM68U4000ALI KM68U4000ALI-L	Industrial(-40~85°C)	2.7~3.3V	85[1]/100	30/15µA		

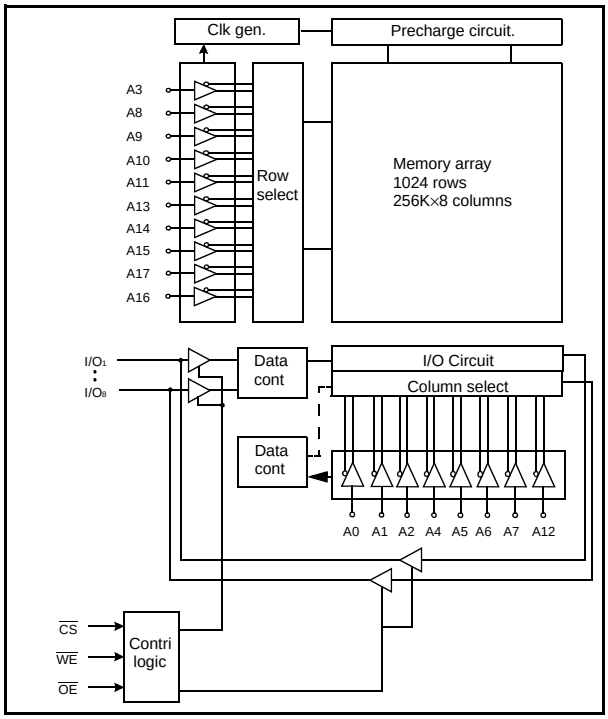
1. The parameter is measured with 30pF test load.

PIN DESCRIPTION



Name	Function	Name	Function
$\overline{CS}$	Chip Select Input	A_0~A_{18}	Address Inputs
$\overline{OE}$	Output Enable Input	I/O_1~I/O_8	Data Inputs/Outputs
$\overline{WE}$	Write Enable Input	Vcc	Power
		Vss	Ground

FUNCTIONAL BLOCK DIAGRAM



PRODUCT LIST

Commercial Temperature Products(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	**Function**	**Part Name**	**Function**
KM68V4000ALG-8	32-SOP, 85ns, 3.3V,L	KM68V4000ALGI-8	32-SOP, 85ns, 3.3V,L
KM68V4000ALG-8L	32-SOP, 85ns, 3.3V,LL	KM68V4000ALGI-8L	32-SOP, 85ns, 3.3V,LL
KM68V4000ALT-8L	32-TSOP2-F, 85ns, 3.3V,LL	KM68V4000ALTI-8L	32-TSOP2-F, 85ns, 3.3V,LL
KM68V4000ALR-8L	32-TSOP2-R, 85ns, 3.3V,LL	KM68V4000ALRI-8L	32-TSOP2-R, 85ns, 3.3V,LL
KM68U4000ALG-8	32-SOP, 85ns, 3.0V,L	KM68U4000ALGI-8	32-SOP, 85ns, 3.0V,L
KM68U4000ALG-8L	32-SOP, 85ns, 3.0V,LL	KM68U4000ALGI-8L	32-SOP, 85ns, 3.0V,LL
KM68U4000ALG-10	32-SOP, 100ns, 3.0V,L	KM68U4000ALGI-10	32-SOP, 100ns, 3.0V,L
KM68U4000ALG-10L	32-SOP, 100ns, 3.0V,LL	KM68U4000ALGI-10L	32-SOP, 100ns, 3.0V,LL
KM68U4000ALT-8L	32-TSOP2-F, 85ns, 3.0V,LL	KM68U4000ALTI-8L	32-TSOP2-F, 85ns, 3.0V,LL
KM68U4000ALT-10L	32-TSOP2-F, 100ns, 3.0V,LL	KM68U4000ALTI-10L	32-TSOP2-F, 100ns, 3.0V,LL
KM68U4000ALR-8L	32-TSOP2-R, 85ns, 3.0V,LL	KM68U4000ALRI-8L	32-TSOP2-R, 85ns, 3.0V,LL
KM68U4000ALR-10L	32-TSOP2-R, 100ns, 3.0V,LL	KM68U4000ALRI-10L	32-TSOP2-R, 100ns, 3.0V,LL

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Mode	Power
H	X[1)]	X[1)]	High-Z	Deselected	Standby
L	H	H	High-Z	Output disbaled	Active
L	L	H	Dout	Read	Active
L	X[1)]	L	Din	Write	Active

1. X means don't care (Must be low or high state)

ABSOLUTE MAXIMUM RATINGS[1)]

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to V_{CC}+0.5	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.3 to 4.6	V	-
Power Dissipation	P_D	0.7	W	-
Storage temperature	T_{STG}	-65 to 150	°C	-
Operating Temperature	T_A	0 to 70	°C	KM68V4000AL, KM68U4000AL
		-40 to 85	°C	KM68V4000ALI, KM68U4000ALI
Soldering temperature and time	T_{SOLDER}	260°C, 10sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	Vcc	KM68V4000A Family KM68U4000A Family	3.0 2.7	3.3 3.0	3.6 3.3	V
Ground	Vss	All Family	0	0	0	V
Input high voltage	V_{IH}	KM68V4000A, KM68U4000A Family	2.2	-	Vcc+0.3[2)]	V
Input low voltage	V_{IL}	KM68V4000A, KM68U4000A Family	-0.3[3)]	-	0.4	V

Note:
1. Commercial Product : T_A=0 to 70°C, otherwise specified
   Industrial Product : T_A=-40 to 85°C, otherwise specified
2. Overshoot : V_{CC}+3.0V in case of pulse width ≤ 30ns
3. Undershoot : -3.0V in case of pulse width ≤ 30ns
4. Overshoot and undershoot is sampled, not 100% tested.

CAPACITANCE[1)] (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTICS

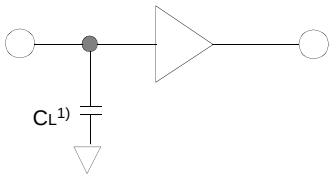
Item	Symbol	Test Conditions[1)]		Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	µA
Output leakage current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc		-1	-	1	µA
Operating power supply current	I_{CC}	I_{IO}=0mA, $\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}, Read		-	-	10	mA
Average operating current	I_{CC1}	Cycle time=1µs, 100% duty, I_{IO}=0mA $\overline{CS}$≤0.2V, V_{IN}≥0.2V or V_{IN} ≥ Vcc-0.2V	Read	-	-	10	mA
			Write	-	-	20	
	I_{CC2}	Cycle time=Min, 100% duty, I_{IO}=0mA, $\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}		-	-	50	mA
Output low voltage	V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage	V_{OH}	I_{OH}=-1.0mA		2.2	-	-	V
Standby Current(TTL)	I_{SB}	$\overline{CS}$=V_{IH}, Other inputs=V_{IL} or V_{IH}		-	-	0.5	mA
Standby Current(CMOS)	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, Other inputs=0~Vcc	KM68V4000AL KM68V4000AL-L	-	-	50 15	µA
			KM68V4000ALI KM68V4000ALI-L	-	-	50 20	µA
			KM68U4000AL KM68U4000AL-L	-	-	30 10	µA
			KM68U4000ALI KM68U4000ALI-L	-	-	30 15	µA

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Input/Output Reference)

Input pulse level : 0.4 to 2.2V
Input rising and faling time : 5ns
Input and output reference voltage :1.5V
Outpuy load(see right) : C_L=100pF+1TTL
C_L[2)]=30pF+1TTL

1. KM68V4000A-8 Family, KM68U4000A-8 Family



1. Including scope and jig capacitance

AC CHARACTERISTICS (KM68V4000A Family : Vcc=3.0~3.3V, KM68U4000A Family : Vcc=2.7~3.3V
Commercial Product : T_A=0 to 70°C, Industrial Product : T_A=-40 to 85°C)

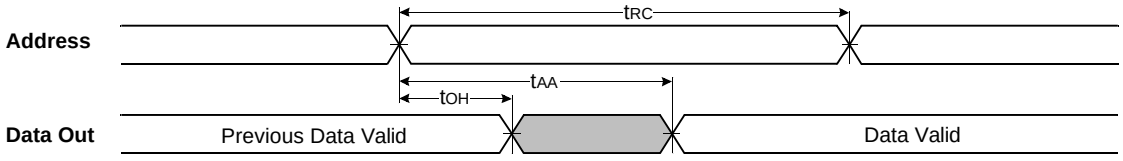
Parameter List		Symbol	Speed Bins				Units
			85ns		100ns		
			Min	Max	Min	Max	
Read	Read cycle time	t_{RC}	85	-	100	-	ns
	Address access time	t_{AA}	-	85	-	100	ns
	Chip select to output	t_{CO}	-	85	-	100	ns
	Output enable to valid output	t_{OE}	-	40	-	50	ns
	Chip select to low-Z output	t_{LZ}	10	-	10	-	ns
	Output enable to low-Z output	t_{OLZ}	5	-	5	-	ns
	Chip disable to high-Z output	t_{HZ}	0	25	0	30	ns
	Output disable to high-Z output	t_{OHZ}	0	25	0	30	ns
	Output hold from address change	t_{OH}	10	-	15	-	ns
Write	Write cycle time	t_{WC}	85	-	100	-	ns
	Chip select to end of write	t_{CW}	70	-	80	-	ns
	Address set-up time	t_{AS}	0	-	0	-	ns
	Address valid to end of write	t_{AW}	70	-	80	-	ns
	Write pulse width	t_{WP}	55	-	70	-	ns
	Write recovery time	t_{WR}	0	-	0	-	ns
	Write to output high-Z	t_{WHZ}	0	20	0	30	ns
	Data to write time overlap	t_{DW}	35	-	40	-	ns
	Data hold from write time	t_{DH}	0	-	0	-	ns
	End write to output low-Z	t_{OW}	5	-	5	-	ns

DATA RETENTION CHARACTERISTICS

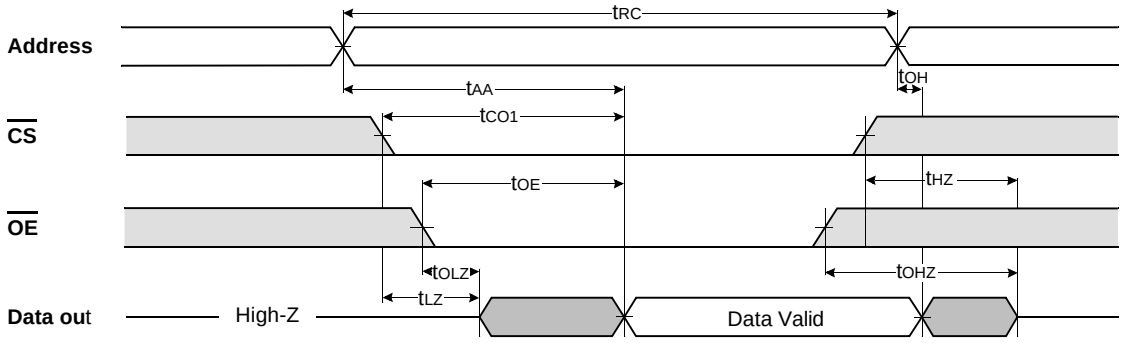
Item	Symbol	Test Condition		Min	Typ	Max	Unit
Vcc for data retention	V_{DR}	$\overline{CS}$≥Vcc-0.2V		2.0	-	3.6	V
Data retention current	I_{DR}	Vcc=3.0V, $\overline{CS}$≥Vcc-0.2V	KM68V4000AL	-	1	30	µA
			KM68V4000AL-L	-	0.5	15	
			KM68V4000ALI	-	-	30	
			KM68V4000ALI-L	-	-	20	
			KM68U4000AL	-	1	30	
			KM68V4000AL-L	-	0.5	10	
			KM68U4000ALI	-	-	30	
			KM68V4000ALI-L	-	-	15	
Data retention set-up time	t_{SDR}	See data retention waveform		0	-	-	ms
Recovery time	t_{RDR}			5	-	-	

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



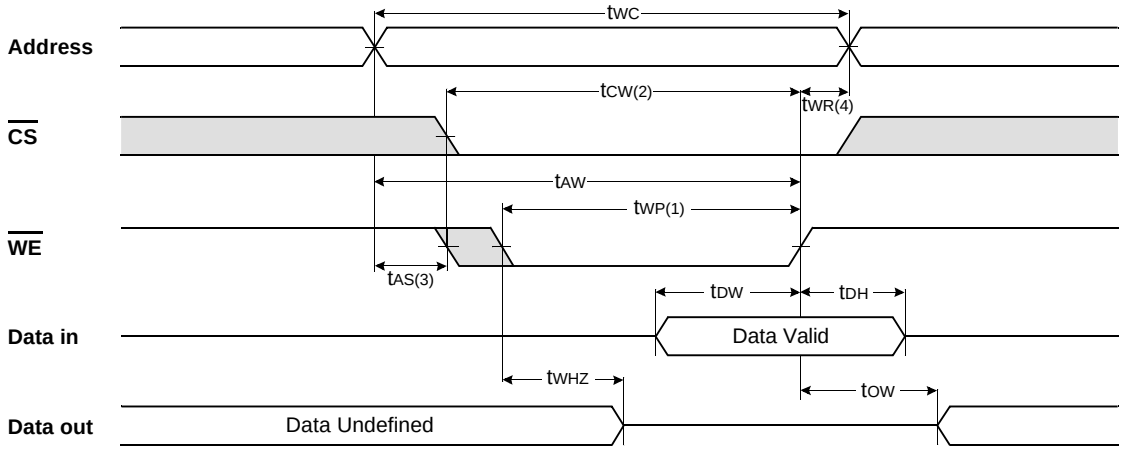
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



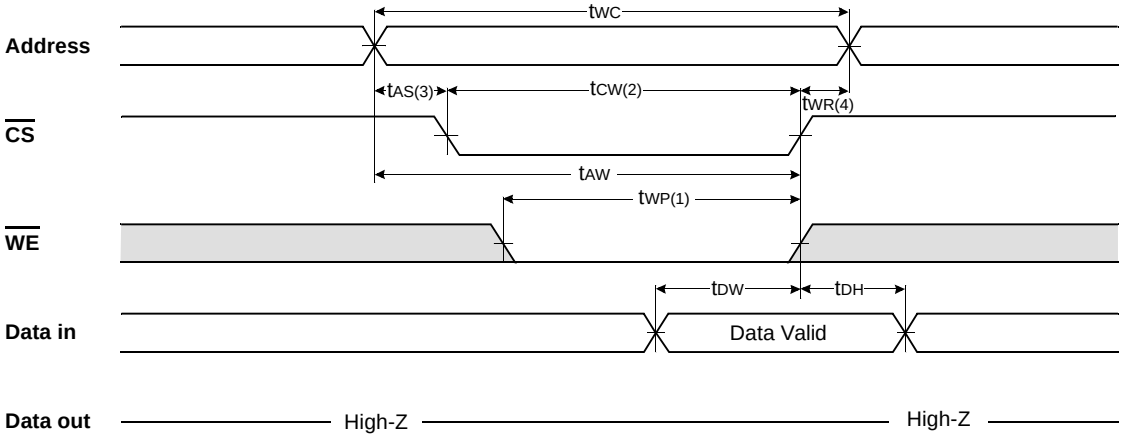
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)

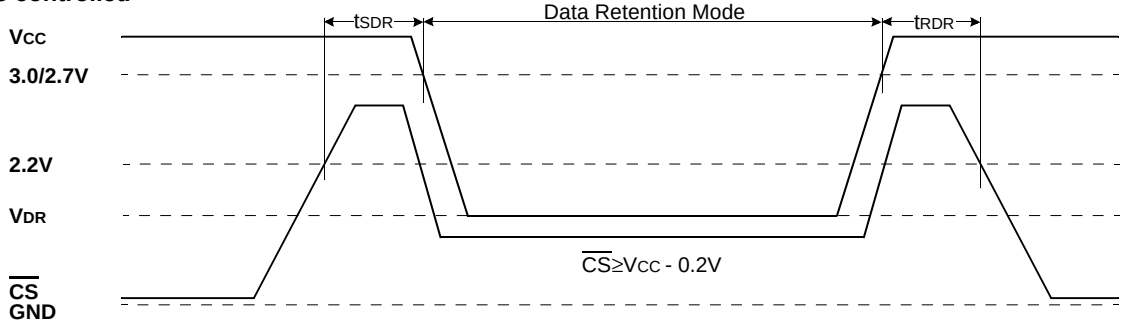


NOTES (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going Low and $\overline{WE}$ going low : A write end at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high, t_{WP} is measured from the begining of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

DATA RETENTION WAVE FORM

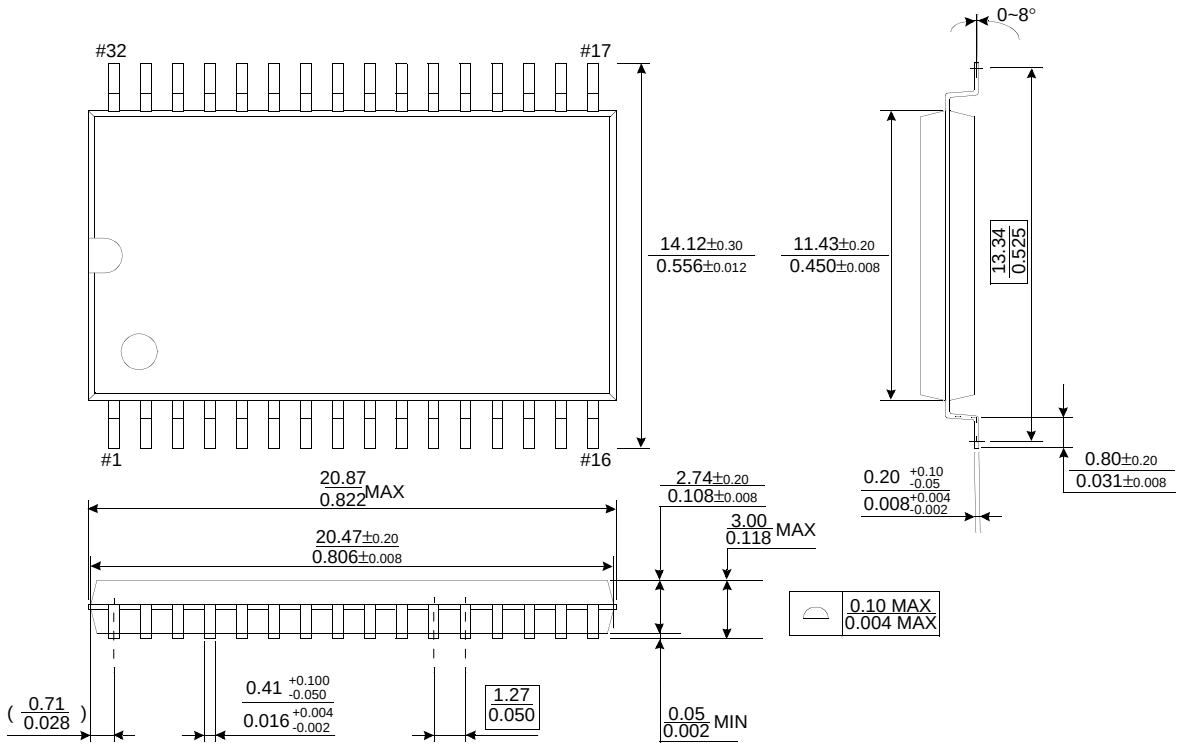
$\overline{CS}$ controlled



PACKAGE DIMENSIONS

Units : millimeter(inch)

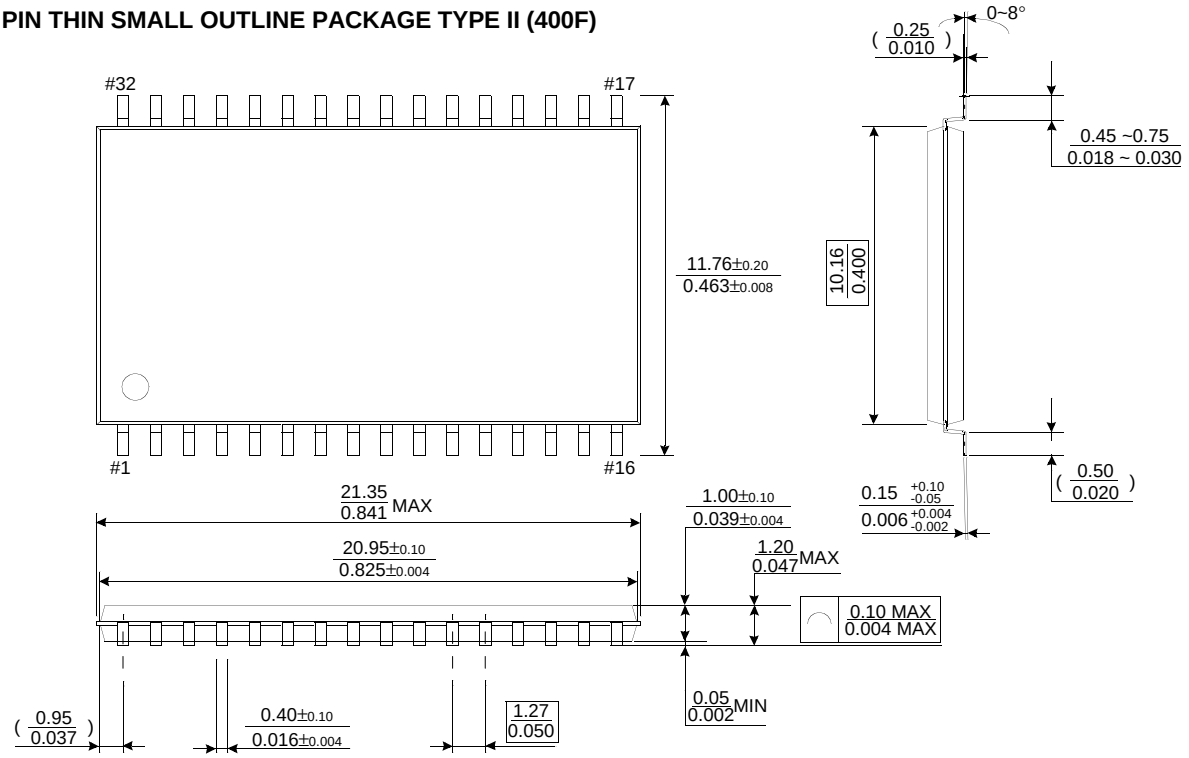
32 PIN PLASTIC SMALL OUTLINE PACKAGE (525mil)



PACKAGE DIMENSIONS

Units : millimeter(inch)

32 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)



32 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400R)