PERICOM

3.3V Fast CMOS Buffer/Clock Driver

Product Features:

- 3.3V version of PI49FCT805/806
- Extremely low output skew: 0.5 ns
- Monitor output pin
- Clock busing with 3-state control
- TTL input and CMOS output compatible
- Extremely low static power (1 mW, typ.)
- Hysteresis on all inputs
- Packages available:
  - 20-pin 300 mil wide DIP (P20)
  - 20-pin 300 mil wide SOIC (S20)
  - 20-pin 150 mil wide QSOP (Q20)
  - 20-pin 209 mil wide SSOP (H20)
- Device models available on request

Product Description:

Pericom Semiconductor's PI49FCT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI49FCT3805 is a 3.3V non-inverting clock driver and the PI49FCT3806 is a 3.3V inverting clock driver designed with two independent groups of buffers. These buffers have 3-state Output Enable inputs (active LOW) with a 1-in, 5-out configuration per group. Each clock driver consists of two banks of drivers, driving five outputs each from a standard TTL compatible CMOS input.

PI49FCT3805 Logic Block Diagram
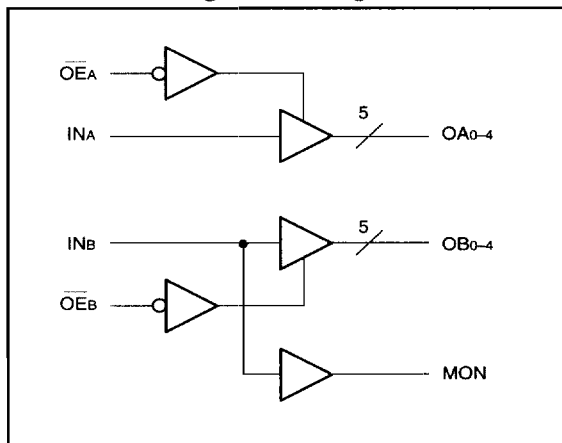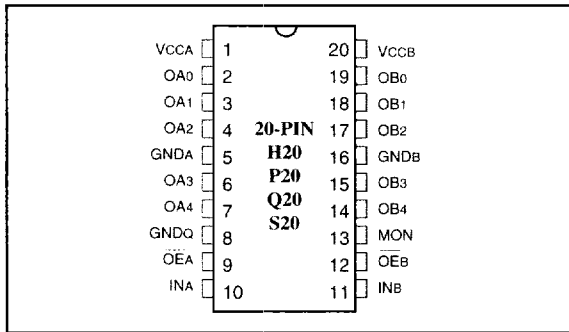

PI49FCT3806 Logic Block Diagram
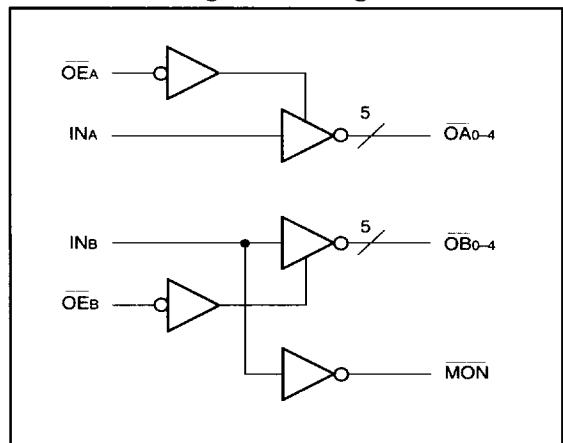
Product Pin Description

Pin Name	Description
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
IN_A, IN_B	Clock Inputs
OA_N, OB_N	Clock Outputs
MON	Monitor Output
GND	Ground
V_{CC}	Power

PI49FCT3805 Truth Table[1]

Inputs		Outputs	
$\overline{OE}_A$, $\overline{OE}_B$	IN_A, IN_B	OA_N, OB_N	MON
L	L	L	L
L	H	H	H
H	L	Z	L
H	H	Z	H

NOTE: 1. H = High Voltage Level, L = Low Voltage Level,
Z = High Impedance

PI49FCT3805 Product Pin Configuration

VCCA	1	20	VCCB
OA0	2	19	OB0
OA1	3	18	OB1
OA2	4 **20-PIN** 17		OB2
GNDA	5 **H20** 16		GNDB
OA3	6 **P20** 15		OB3
OA4	7 **Q20** 14		OB4
GNDQ	8 **S20** 13		MON
$\overline{OE}_A$	9	12	OEB
INA	10	11	INB

PI49FCT3806 Truth Table[1]

Inputs		Outputs	
$\overline{OE}_A$, $\overline{OE}_B$	IN_A, IN_B	$\overline{OA}_N$, $\overline{OB}_N$	$\overline{MON}$
L	L	H	H
L	H	L	L
H	L	Z	H
H	H	Z	L

NOTE: 1. H = High Voltage Level, L = Low Voltage Level,
Z = High Impedance
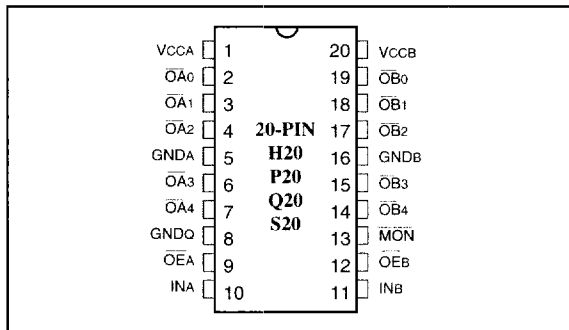
PI49FCT3806 Product Pin Configuration

VCCA	1	20	VCCB
$\overline{OA}_0$	2	19	$\overline{OB}_0$
$\overline{OA}_1$	3	18	$\overline{OB}_1$
$\overline{OA}_2$	4 **20-PIN** 17		$\overline{OB}_2$
GNDA	5 **H20** 16		GNDB
$\overline{OA}_3$	6 **P20** 15		$\overline{OB}_3$
$\overline{OA}_4$	7 **Q20** 14		$\overline{OB}_4$
GNDQ	8 **S20** 13		$\overline{MON}$
$\overline{OE}_A$	9	12	$\overline{OE}_B$
INA	10	11	INB

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[1]	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Notes:
1. This parameter is determined by device characterization but is not production tested.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C	
Ambient Temperature with Power Applied .... 0°C to +70°C	
Supply Voltage to Ground Potential (Inputs & Vcc Only) .... −0.5V to +7.0V	
Supply Voltage to Ground Potential (Outputs & D/O Only) .... −0.5V to +7.0V	
DC Input Voltage .... −0.5V to +7.0V	
DC Output Current .... 120 mA	
Power Dissipation 0.5W	

Note:
Stresses greater than those listed under
MAXIMUM RATINGS may cause permanent
damage to the device. This is a stress rating
only and functional operation of the device at
these or any other conditions above those
indicated in the operational sections of this
specification is not implied. Exposure to
absolute maximum rating conditions for
extended periods may affect reliability.

Operating Range

Ambient Temperature = 0°C to +70°C
Vcc = 3.3V ± 0.3V

DC Electrical Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	Vcc = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −0.1 mA	Vcc−0.2	—	—	V
			I_{OH} = −8 mA	2.4[3]	3.0		
V_{OL}	Output LOW Voltage	Vcc = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1 mA	—	—	0.2	V
			I_{OL} = 16 mA	—	0.2	0.4	
			I_{OL} = 24 mA	—	0.3	0.5	
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	Input Pins	2.0	—	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	Input Pins	−0.5	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max.	V_{IN} = Vcc (Input Pins)	—	—	1	μA
I_{IL}	Input LOW Current	Vcc = Max.	V_{IN} = GND (Input & I/O Pins)	—	—	−1	μA
I_{OZH}	High Impedance	Vcc = Max.	V_{OUT} = Vcc	—	—	1	μA
I_{OZL}	Output Current	(3-State Output Pins)	V_{OUT} = GND	—	—	−1	
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_{IN} = −18 mA		—	−0.7	−1.2	V
I_{ODH}	Output HIGH Current	Vcc = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[4]		−35	−60	−110	mA
I_{ODL}	Output LOW Current	Vcc = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[4]		50	90	200	mA
I_{OS}	Short Circuit Current[5]	Vcc = Max., V_{OUT} = GND[5]		−60	−135	−240	mA
V_H	Input Hysteresis			—	150	—	mV

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient and maximum loading.
3. V_{OH} = Vcc − 0.6V at rated current.
4. This parameter is determined by device characterization but is not production tested.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

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Power Supply Characteristics

| Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}	—	3	30	μA
ΔI_{CC}	Supply Current per Inputs @ TTL HIGH	V_{CC} = Max.	$V_{IN} = V_{CC} - 0.6V$[3]	—	2.0	300	μA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open $\overline{OE}_A$ or $\overline{OE}_B$ = GND Per Output Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	—	0.08	0.16	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open fo = 10 MHz	$V_{IN} = V_{CC}$ V_{IN} = GND	—	3.3	9.0[5]	mA
		50% Duty Cycle $\overline{OE}_A$ or $\overline{OE}_B$ = GND Mon. Output Toggling	$V_{IN} = V_{CC} - 0.6V$ V_{IN} = GND	—	3.3	10.0[5]	
		V_{CC} = Max., Outputs Open fo = 2.5 MHz	$V_{IN} = V_{CC}$ V_{IN} = GND	—	1.8	6.0[5]	
		50% Duty Cycle $\overline{OE}_A$ or $\overline{OE}_B$ = GND Eleven Outputs Toggling	$V_{IN} = V_{CC} - 0.6V$ V_{IN} = GND	—	1.8	7.0[5]	

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input ($V_{IN} = V_{CC} - 0.6V$); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_C formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_O N_O)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = V_{CC} - 0.6V$)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_O = Output Frequency
   N_O = Number of Outputs at f_O
   All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	3805/3806 Com.		3805A/3806A Com.		3805B/3806B Com.		3805C/3806C Com.		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay INa to OAn, INb to OBn	$C_L = 50$ pF $R_L = 500\Omega$	1.5	6.5	1.5	5.8	1.5	5.0	1.5	4.5	ns
tPZH tPZL	Output Enable Time OEa to OAn, OEb to OBn		1.5	8.0	1.5	8.0	1.5	6.5	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time OEa to OAn, OEb to OBn		1.5	7.0	1.5	7.0	1.5	6.0	1.5	5.0	ns
tSK(o)[3]	Skew between two outputs of same package (same transition)		—	0.7	—	0.7	—	0.5	—	0.5	ns
tSK(p)[2]	Skew between opposite transitions (tPHL-tPLH) of the same output		—	1.0	—	0.7	—	0.5	—	0.5	ns
tSK(t)[3]	Skew between two outputs of different package at same temperature (same transition)		—	1.5	—	1.2	—	1.0	—	0.8	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew measured at worse cast temperature (max. temp).

Tests Circuits For All Outputs[1]
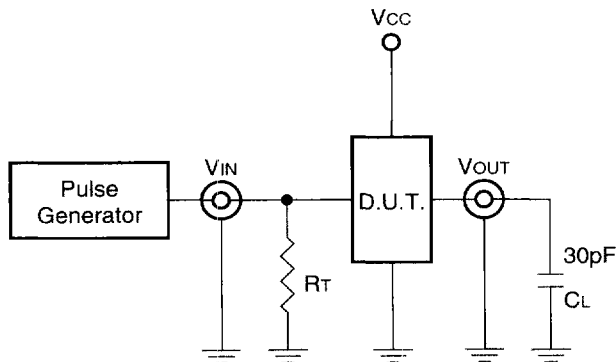
Switch Position

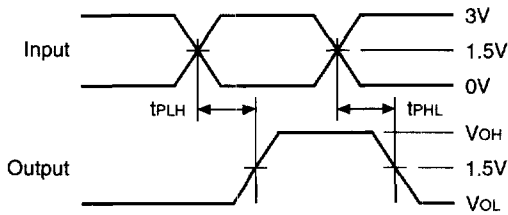| Test	Switch
Disable LOW Enable LOW	6V
Disable HIGH Enable HIGH	GND
All Other Inputs	Open

DEFINITIONS:
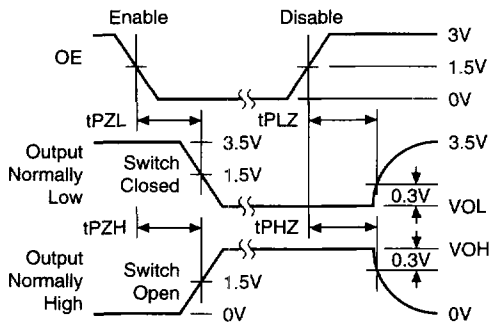C_L = Load capacitance: includes jig and probe capacitance.
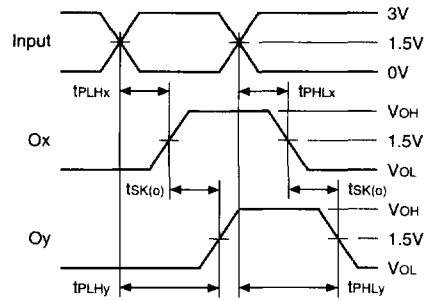R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

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SWITCHING WAVEFORMS

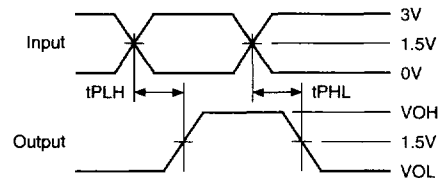## Propagation Delay

Enable and Disable Times

Output Skew – $t_{SK(o)}$
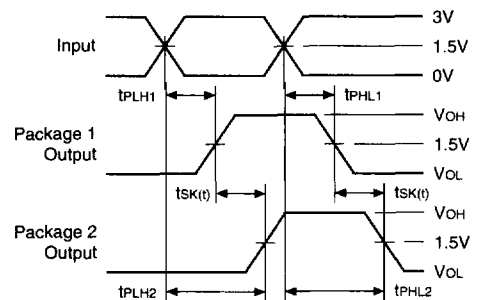

$$t_{SK(o)} = |\ t_{PLHy} - t_{PLHx}\ |\ \text{or}\ |\ t_{PHLy} - t_{PHLx}\ |$$

Pulse Skew – $t_{SK(p)}$

$$t_{SK(p)} = |\ t_{PHL} - t_{PLH}\ |$$

Package Skew – $t_{SK(t)}$

$$t_{SK(t)} = |\ t_{PLH2} - t_{PLH1}\ |\ \text{or}\ |\ t_{PHL2} - t_{PHL1}\ |$$

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