

HM5116160A/AL Series Preliminary

1,048,576-word × 16-bit Dynamic Random Access Memory

The Hitachi HM5116160A/AL is a CMOS dynamic RAM organized 1,048,576 words × 16 bits. It employs the most advanced CMOS technology for high performance and low power. The HM5116160A/AL offers Fast Page Mode as a high speed access mode.

Feature

- Single 5.0 V (± 10%)
- High speed
 - Access time
60 ns/ 70 ns/ 80 ns (max)
- Low power dissipation
 - Active mode
550 mW/495 mW/440mW (max)
 - Standby mode 11 mW (max)
0.83 mW (max) (L-version)
- Fast page mode capability
- Long refresh period
 - 4096 refresh cycles : 64 ms
:128 ms (L-version)
- 4 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh
 - Self refresh (L-version)
- 2 $\overline{\text{CAS}}$ -byte control
- Battery backup operation (L-version)

Ordering Information

Type No.	Access time	Package
HM5116160AJ/ALJ-6	60 ns	400-mil, 42-pin
HM5116160AJ/ALJ-7	70 ns	plastic SOJ
HM5116160AJ/ALJ-8	80 ns	(CP-42D)
HM5116160ATT/ALTT-6	60 ns	400-mil,
HM5116160ATT/ALTT-7	70 ns	50-pin
HM5116160ATT/ALTT-8	80 ns	plastic TSOP II (TTP-50/44DC)

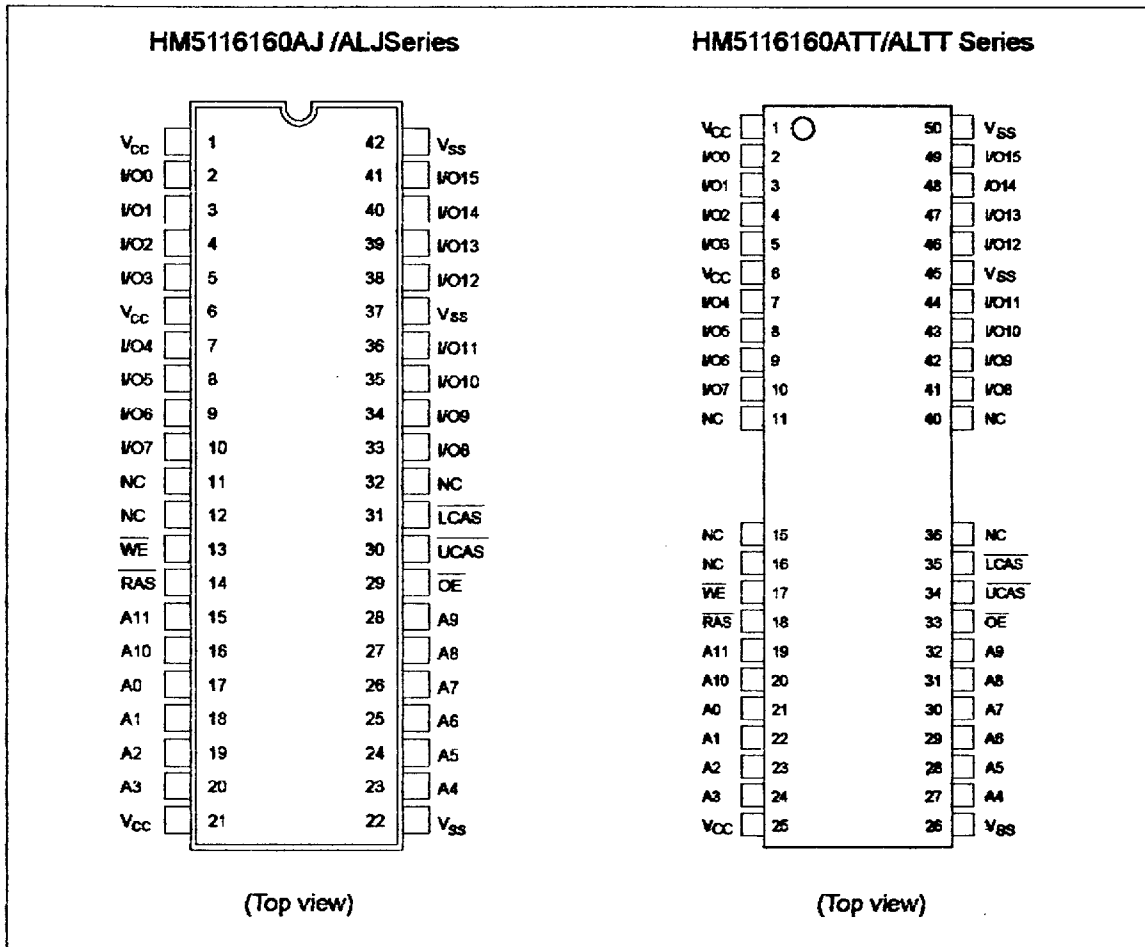
Pin Description

Pin name	Function
A0 to A11	Address input
A0 to A11	Refresh address input
I/O0 to I/O15	Data input/data output
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{UCAS}}, \overline{\text{LCAS}}$	Column address strobe
$\overline{\text{WE}}$	Read/Write enable
$\overline{\text{OE}}$	Output enable
V _{CC}	Power supply (+ 5.0 V)
V _{SS}	Ground
NC	No connection

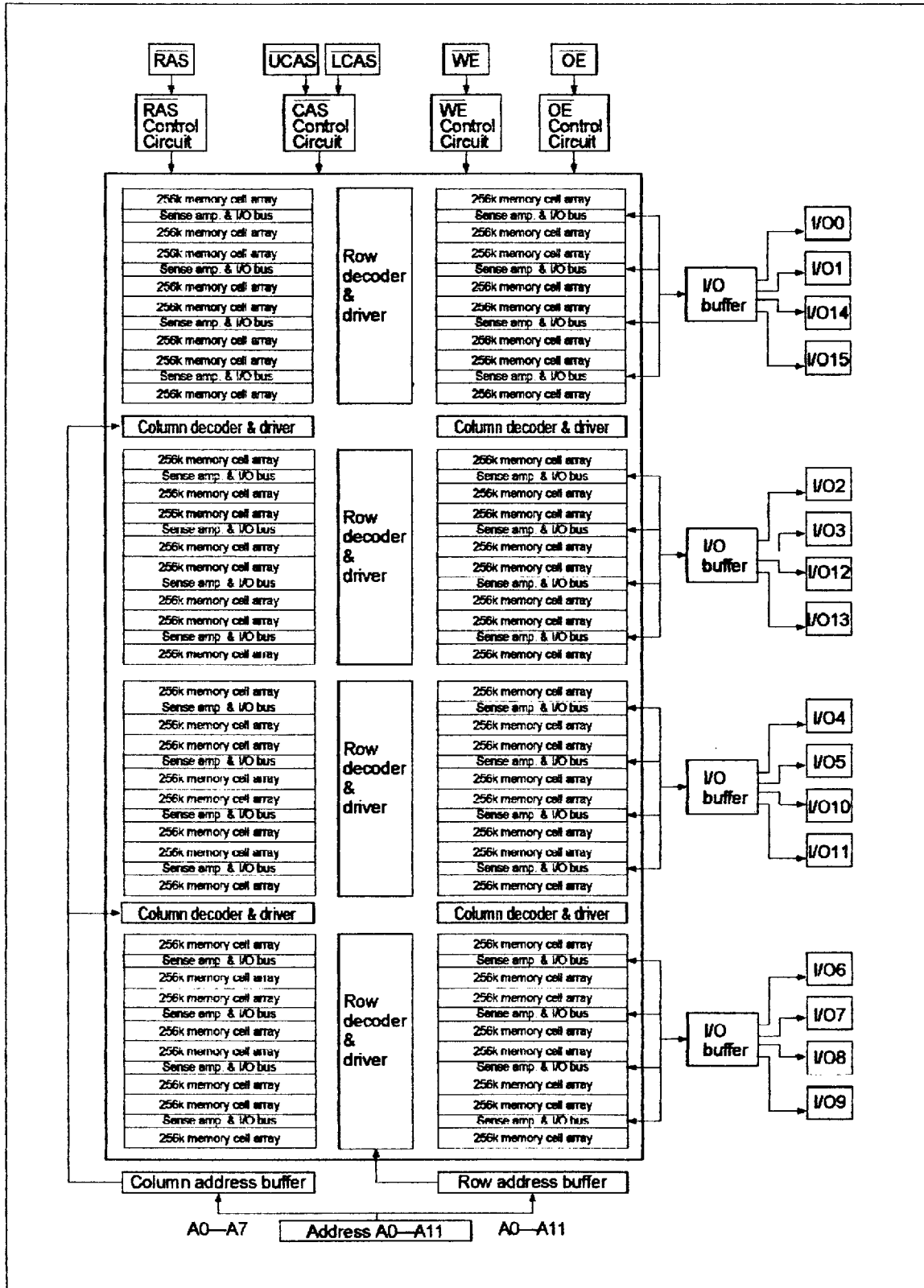
Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

This specification is fully compatible with the preliminary 16-Mbit DRAM specifications from TEXAS INSTRUMENTS.

Pin Arrangement



Block Diagram



Truth Table

Inputs					I/O		Operation	Notes
RAS	LCAS	UCAS	WE	OE	I/O0 – I/O7	I/O8 – I/O15		
H	H	H	H	H	High-Z	High-Z	Standby	1, 3
L	H	H	H	H	High-Z	High-Z	Refresh	1, 3
L	L	H	H	L	Dout	High-Z	Lower byte read	1, 3
L	H	L	H	L	High-Z	Dout	Upper byte read	1, 3
L	L	L	H	L	Dout	Dout	Word read	1, 3
L	L	H	L	H	Din	Don't care	Lower byte write	1, 2, 3
L	H	L	L	H	Don't care	Din	Upper byte write	1, 2, 3
L	L	L	L	H	Din	Din	Word write	1, 2, 3
L	L	L	H	H	High-Z	High-Z		1, 3
H to L	L	H	–	–	High-Z	High-Z	CBR refresh or Self refresh	1, 3
H to L	H	L	–	–	High-Z	High-Z		
H to L	L	L	–	–	High-Z	High-Z		

Notes: 1. H: High(inactive) L: Low(active)

2. $t_{WCS} \geq 0$ ns Early write cycle
 $t_{WCS} < 0$ ns Delayed write cycle

3. Mode is determined by the OR function of the \overline{UCAS} and \overline{LCAS} . (Mode is set by the earliest of \overline{UCAS} and \overline{LCAS} active edge and reset by the latest of \overline{UCAS} and \overline{LCAS} inactive edge.)
 However write OPERATION and output HIZ control are done independently by each \overline{UCAS} , \overline{LCAS} .

ex. if $\overline{RAS} = H$ to L, $\overline{LCAS} = L$, $\overline{UCAS} = H$, then \overline{CAS} -before- \overline{RAS} refresh cycle is selected.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{CC}	4.5	5.0	5.5	V	1
Input high voltage	V _{IH}	2.4	—	6.5	V	1
Input low voltage	V _{IL}	-1.0	—	0.8	V	1

Note : 1. All voltage referred to V_{SS}

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V)

		HM5116160A/AL								
		-6		-7		-8				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test condition	Notes
Operating current	I _{CC1}	—	100	—	90	—	80	mA	t _{RC} = min	1, 2
Standby current	I _{CC2}	—	2	—	2	—	2	mA	TTL interface RAS, UCAS, LCAS = V _{IH} , Dout = High-Z	
		—	1	—	1	—	1	mA	CMOS interface RAS, UCAS, LCAS ≥ V _{CC} - 0.2V Dout = High-Z	
Standby current (L-version)		—	0.15	—	0.15	—	0.15	mA	CMOS interface RAS, UCAS, LCAS ≥ V _{CC} - 0.2V Dout = High-Z	
RAS-only refresh current	I _{CC3}	—	100	—	90	—	80	mA	t _{RC} = min	2
Standby current	I _{CC5}	—	5	—	5	—	5	mA	RAS = V _{IH} UCAS, LCAS = V _{IL} Dout = enable	1
CAS-before-RAS refresh current	I _{CC6}	—	100	—	90	—	80	mA	t _{RC} = min	
Fast page mode current	I _{CC7}	—	100	—	90	—	80	mA	t _{PC} = min	1,3
Battery back up operating current (Stand by with CBR refresh) (L-version)	I _{CC10}	—	0.5	—	0.5	—	0.5	mA	CMOS interface Dout = High-Z CBR refresh: t _{RC} = 31.3 μs t _{RAS} ≤ 0.3 μs	

DC Characteristics (cont.)

Parameter	Symbol	HM5116160A/AL						Unit	Test condition	Notes
		-6		-7		-8				
		Min	Max	Min	Max	Min	Max			
Self refresh mode current (L-version)	I_{CC11}	—	300	—	300	—	300	μA	CMOS interface $\overline{\text{RAS}}, \overline{\text{UCAS}}, \overline{\text{LCAS}} \leq 0.2\text{V}$ Dout = High-Z	
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	μA	$0\text{V} \leq V_{in} \leq 7\text{V}$	
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	μA	$0\text{V} \leq V_{out} \leq 7\text{V}$ Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = -5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

- Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
 2. Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.
 3. Address can be changed once or less while $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}} = V_{IH}$

Capacitance ($T_a = 25^\circ\text{C}, V_{CC} = 5.0\text{V} \pm 10\%$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	7	pF	1, 2

- Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}} = V_{IH}$ to disable Dout.

AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$) *1, *2, *3, *19,

Test Conditions

Input rise and fall times : 5 ns

Input timing reference levels : 0.8 V, 2.4 V

Output timing reference levels : 0.4 V, 2.4 V

Output load : 2 TTL gate + C_L (100 pF)
(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

Parameter	Symbol	HM5116160A/AL						Unit	Notes
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110	—	130	—	150	—	ns	
$\overline{\text{RAS}}$ precharge time	t_{RP}	40	—	50	—	60	—	ns	
$\overline{\text{CAS}}$ precharge time	t_{CP}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns	
$\overline{\text{CAS}}$ pulse width	t_{CAS}	15	10000	18	10000	20	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	10	—	15	—	15	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t_{RCD}	20	45	20	52	20	60	ns	4
$\overline{\text{RAS}}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	5
$\overline{\text{RAS}}$ hold time	t_{RSH}	15	—	18	—	20	—	ns	
$\overline{\text{CAS}}$ hold time	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{\text{OE}}$ to Din delay time	t_{OED}	15	—	18	—	20	—	ns	6
$\overline{\text{OE}}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	7
$\overline{\text{CAS}}$ delay time from Din	t_{DZC}	0	—	0	—	0	—	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	8

Read Cycle

Parameter	Symbol	HM5116160A/AL						Unit	Notes
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	—	80	ns	9, 10
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	15	—	18	—	20	ns	10, 11, 18
Access time from address	t_{AA}	—	30	—	35	—	40	ns	10, 12, 18
Access time from $\overline{\text{OE}}$	t_{OEA}	—	15	—	18	—	20	ns	10
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	13
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	0	—	ns	13
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	30	—	35	—	40	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	30	—	35	—	40	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	0	—	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	3	—	ns	
Output data hold time from $\overline{\text{OE}}$	t_{OHO}	3	—	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	15	—	15	—	15	ns	14
Output buffer turn-off to $\overline{\text{OE}}$	t_{OEZ}	—	15	—	15	—	15	ns	14
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	15	—	18	—	20	—	ns	6

Write Cycle

		HM5116160A/AL							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	15
Write command hold time	t_{WCH}	10	—	15	—	15	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	10	—	ns	
Write command to \overline{RAS} lead time	t_{RWL}	15	—	18	—	20	—	ns	
Write command to \overline{CAS} lead time	t_{CWL}	15	—	18	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	16
Data-in hold time	t_{DH}	10	—	15	—	15	—	ns	16

Read-Modify-Write Cycle

		HM5116160A/AL							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	155	—	181	—	205	—	ns	
\overline{RAS} to \overline{WE} delay time	t_{RWD}	85	—	98	—	110	—	ns	15
\overline{CAS} to \overline{WE} delay time	t_{CWD}	40	—	46	—	50	—	ns	15
Column address to \overline{WE} delay time	t_{AWD}	55	—	63	—	70	—	ns	15
\overline{OE} hold time from \overline{WE}	t_{OEH}	15	—	18	—	20	—	ns	

Refresh Cycle

		HM5116160A/AL							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Note
$\overline{\text{CAS}}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	10	—	ns	
RAS precharge to $\overline{\text{CAS}}$ hold time	t_{RPC}	0	—	0	—	0	—	ns	

Fast Page Mode Cycle

		HM5116160A/AL							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode cycle time	t_{PC}	40	—	45	—	50	—	ns	
Fast page mode $\overline{\text{RAS}}$ pulse width	t_{RASP}	—	100000	—	100000	—	100000	ns	17
Access time from $\overline{\text{CAS}}$ precharge	t_{CPA}	—	35	—	40	—	45	ns	10, 18
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t_{CPRH}	35	—	40	—	45	—	ns	

Fast Page Mode Read-Modify-Write Cycle

		HM5116160A/AL							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Note
Fast page mode read- modify-write cycle time	t_{PRWC}	85	—	96	—	105	—	ns	
$\overline{\text{WE}}$ delay time from $\overline{\text{CAS}}$ precharge	t_{CPW}	60	—	68	—	75	—	ns	15

HM5116160A/AL Series

HM5116160A/AL Series

Refresh

Parameter	Symbol	Max	Unit	Note
Refresh period	t_{REF}	64	ms	4096 cycles
Refresh period (L-version)	t_{REF}	128	ms	4096 cycles

Self-Refresh Mode

Parameter	Symbol	HM5116160AL						Unit	Notes
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
\overline{RAS} pulse width (self refresh)	t_{RASS}	100	—	100	—	100	—	μs	
\overline{RAS} precharge time (self refresh)	t_{RPS}	110	—	130	—	150	—	ns	
\overline{CAS} hold time (self refresh)	t_{CHS}	-50	—	-50	—	-50	—	ns	

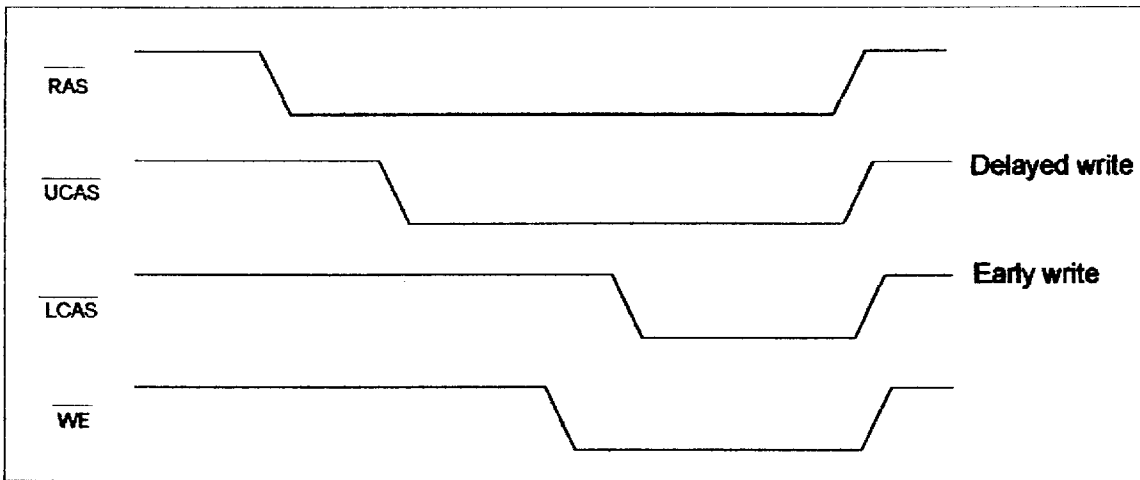
- Notes:
1. AC measurements assume $t_T = 5$ ns.
 2. An initial pause of 200 μ s is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh).
 3. Only row address is indispensable on address A8, A9, A10, A11.
 4. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .
 5. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA} .
 6. Either t_{OED} or t_{CDD} must be satisfied.
 7. Either t_{DZO} or t_{DZC} must be satisfied.
 8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
 9. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}$ (max) and $t_{\text{RAD}} \leq t_{\text{RAD}}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 10. Measured with a load circuit equivalent to 2 TTL loads and 100 pF. ($V_{\text{OH}} = 2.4$ V, $V_{\text{OL}} = 0.4$ V)
 11. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}$ (max) and $t_{\text{RAD}} \leq t_{\text{RAD}}$ (max).
 12. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}$ (max) and $t_{\text{RAD}} \geq t_{\text{RAD}}$ (max).
 13. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
 14. t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
 15. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only, if $t_{\text{WCS}} \geq t_{\text{WCS}}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{\text{RWD}} \geq t_{\text{RWD}}$ (min), $t_{\text{CWD}} \geq t_{\text{CWD}}$ (min), and $t_{\text{AWD}} \geq t_{\text{AWD}}$ (min), or $t_{\text{CWD}} \geq t_{\text{CWD}}$ (min), $t_{\text{AWD}} \geq t_{\text{AWD}}$ (min) and $t_{\text{CPW}} \geq t_{\text{CPW}}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 16. These parameters are referred to $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in delayed write or read-modify-write cycles.
 17. t_{RASP} defines $\overline{\text{RAS}}$ pulse width in fast page mode cycles.
 18. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA} .
 19. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device. After $\overline{\text{RAS}}$ is reset, if $t_{\text{OEH}} \geq t_{\text{CWL}}$, the I/O pin will remain open circuit (high impedance); if $t_{\text{OEH}} \leq t_{\text{CWL}}$, invalid data will be out at each I/O.
 20. When both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ go low at the same time, all 16-bits data are written into the device. $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ cannot be staggered within the same write/read cycles.
 21. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
 22. t_{ASC} , t_{CAH} , t_{RCS} , t_{WCS} , t_{WCH} , t_{CSR} and t_{RPC} are determined by the earlier falling edge of $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$.
 23. t_{CRP} , t_{CHR} , t_{RCH} , t_{ACP} and t_{CPW} are determined by the later rising edge of $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$.
 24. t_{CWL} , t_{DH} , t_{DS} and t_{CHS} should be satisfied by both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.
 25. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large $V_{\text{CC}}/V_{\text{SS}}$ line noise, which causes to degrade V_{IH} min/ V_{IL} max level.
 26. Please do not use t_{RASS} timing, $10 \mu\text{s} \leq t_{\text{RASS}} \leq 100 \mu\text{s}$. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{\text{RASS}} \geq 100 \mu\text{s}$, then $\overline{\text{RAS}}$ precharge time should use t_{RPS} instead of t_{RP} .
 27. If you use distributed CBR refresh mode with 15.6 μs interval in normal read/write cycle, CBR refresh should be executed within 15.6 μs immediately after exiting from and before entering into self refresh mode.

- 28. If you use $\overline{\text{RAS}}$ only refresh or CBR burst refresh mode in normal read/write cycle, 4096 cycles of distributed CBR refresh with 15.6 μs interval should be executed within 64 ms immediately after exiting from and before entering into the self refresh mode.
- 29. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.

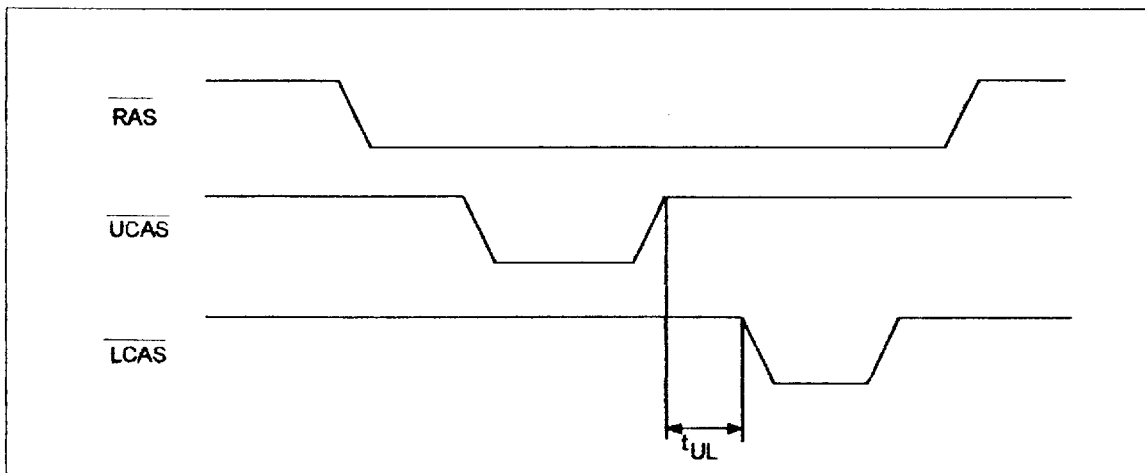
Notes concerning $\overline{2\text{CAS}}$ control

Please do not separate the $\overline{\text{UCAS}}/\overline{\text{LCAS}}$ operation timing intentionally. However skew between $\overline{\text{UCAS}}/\overline{\text{LCAS}}$ are allowed under the following conditions.

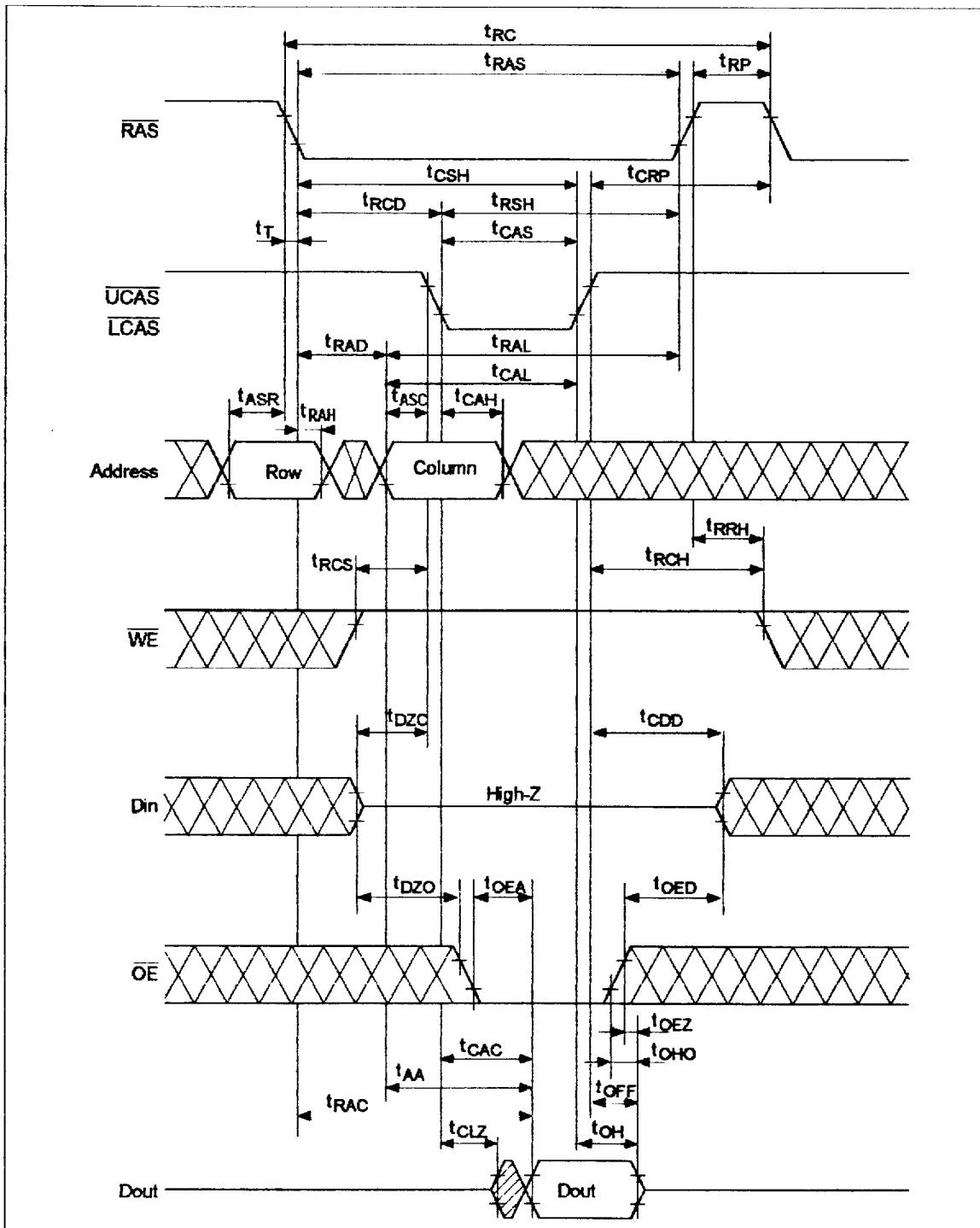
- (1) Each of the $\overline{\text{UCAS}}/\overline{\text{LCAS}}$ should satisfy the timing specifications individually.
- (2) Different operation mode for upper/lower byte is not allowed; such as following.





- (3) Closely separated upper/lower byte control is not allowed. However when the condition ($t_{CP} \leq t_{UL}$) is satisfied, fast page mode can be performed.



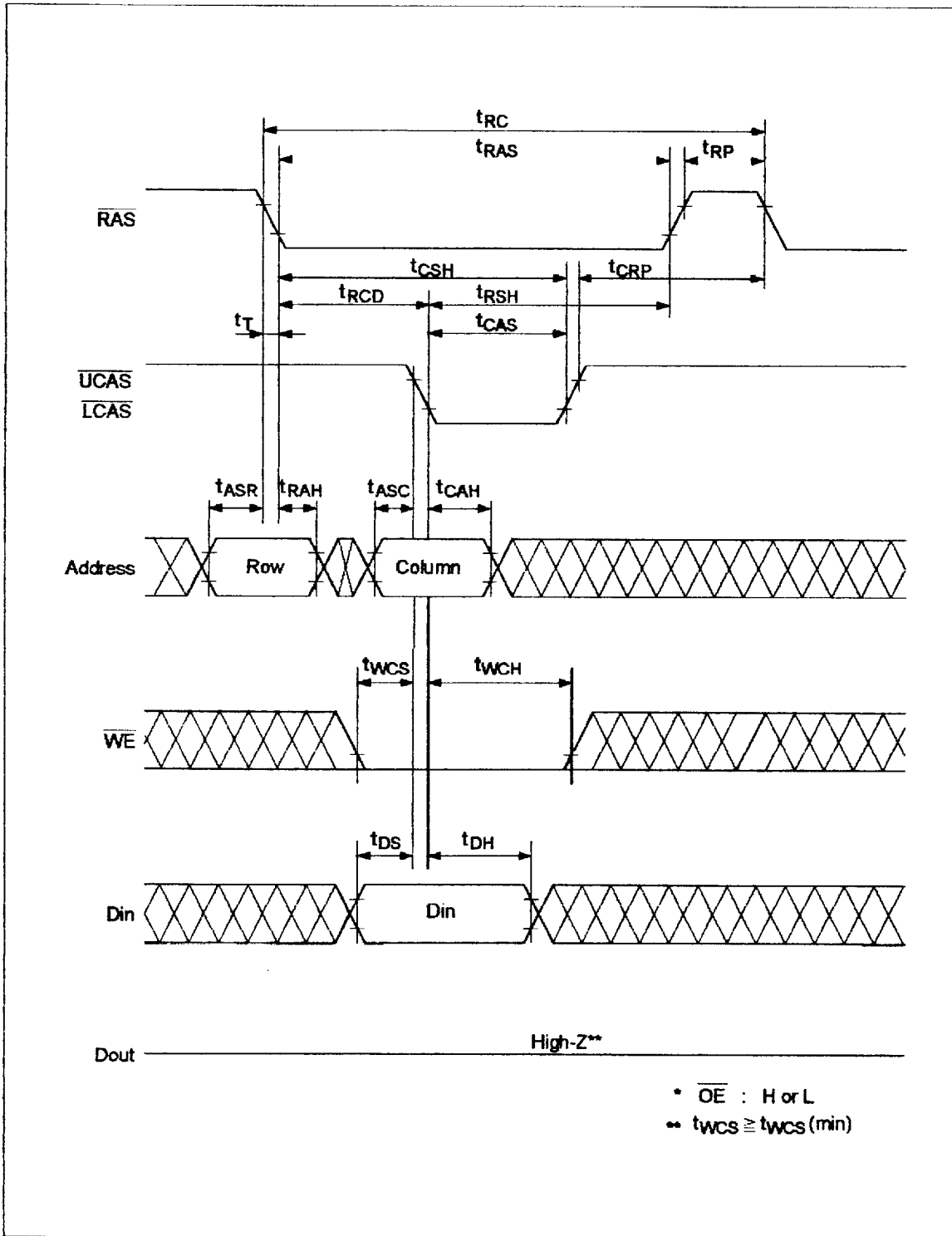
Timing Waveforms*30
Read Cycle



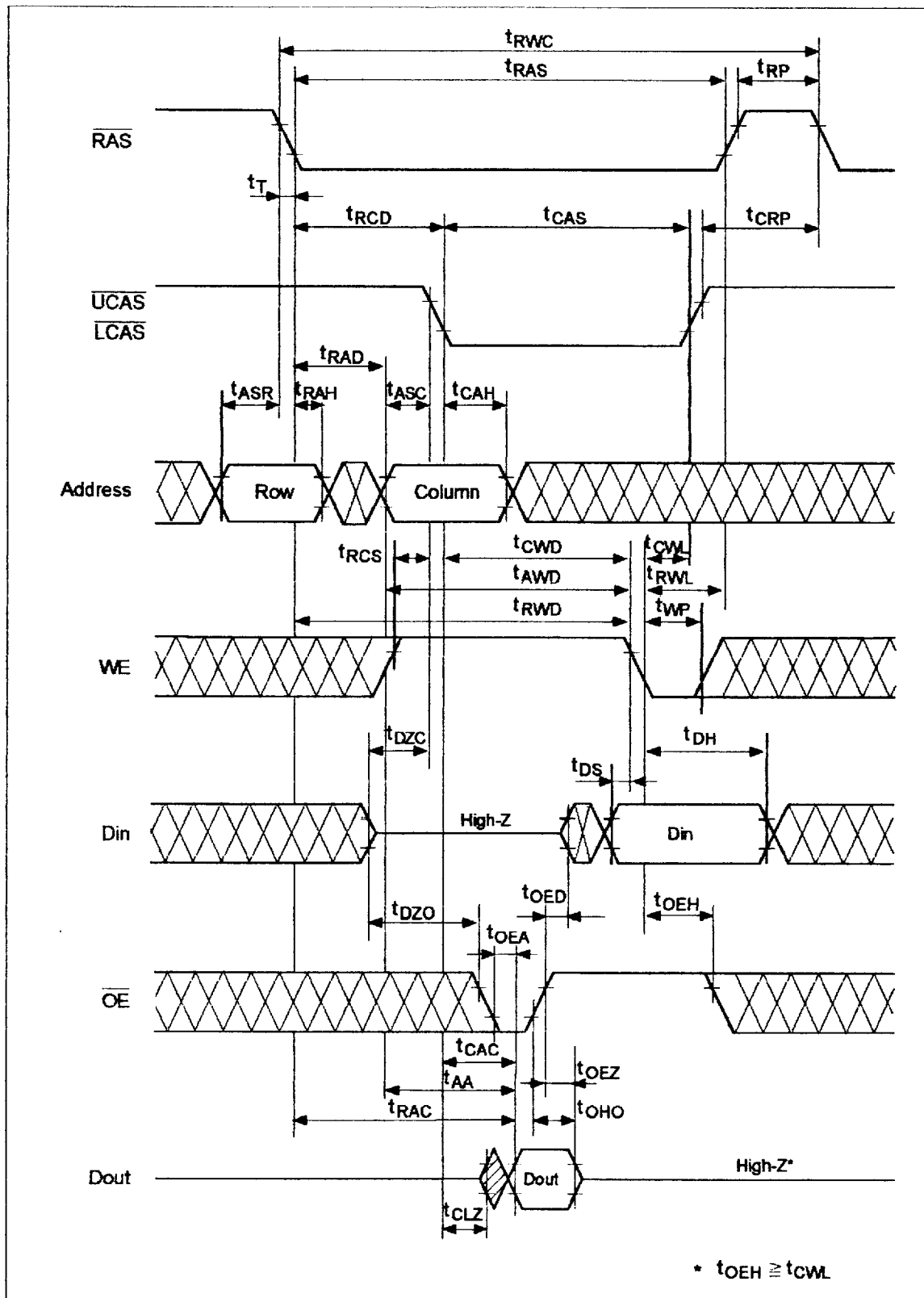
Note 30:

-  H or L (H: $V_{IH}(\min) \leq V_{IN} \leq V_{IH}(\max)$, L: $V_{IL}(\min) \leq V_{IN} \leq V_{IL}(\max)$)
-  Invalid Dout

Early Write Cycle

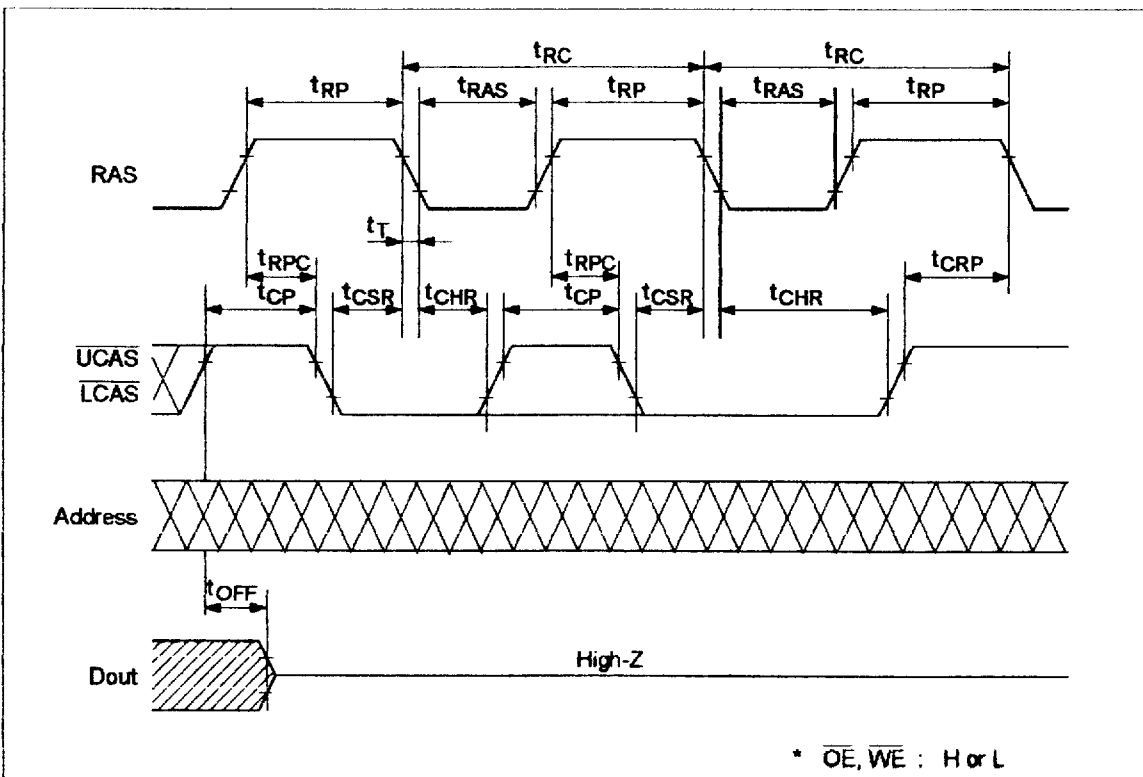
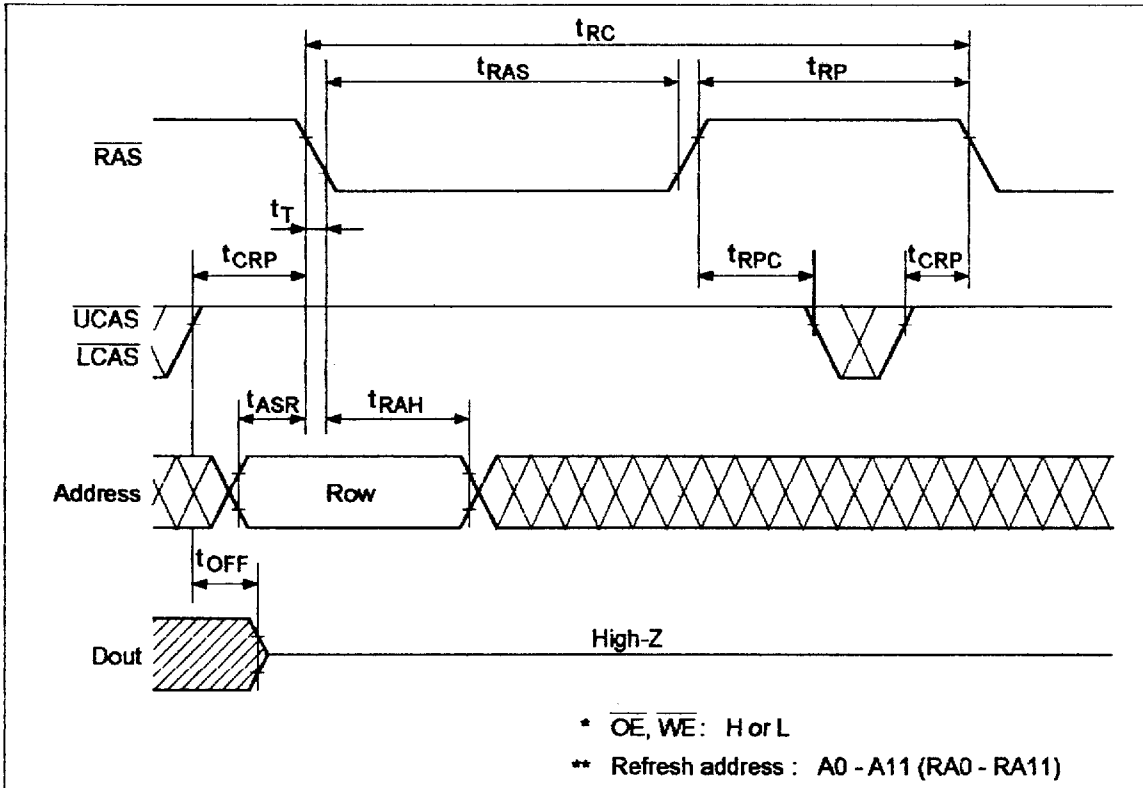


Read-Modify-Write Cycle *19

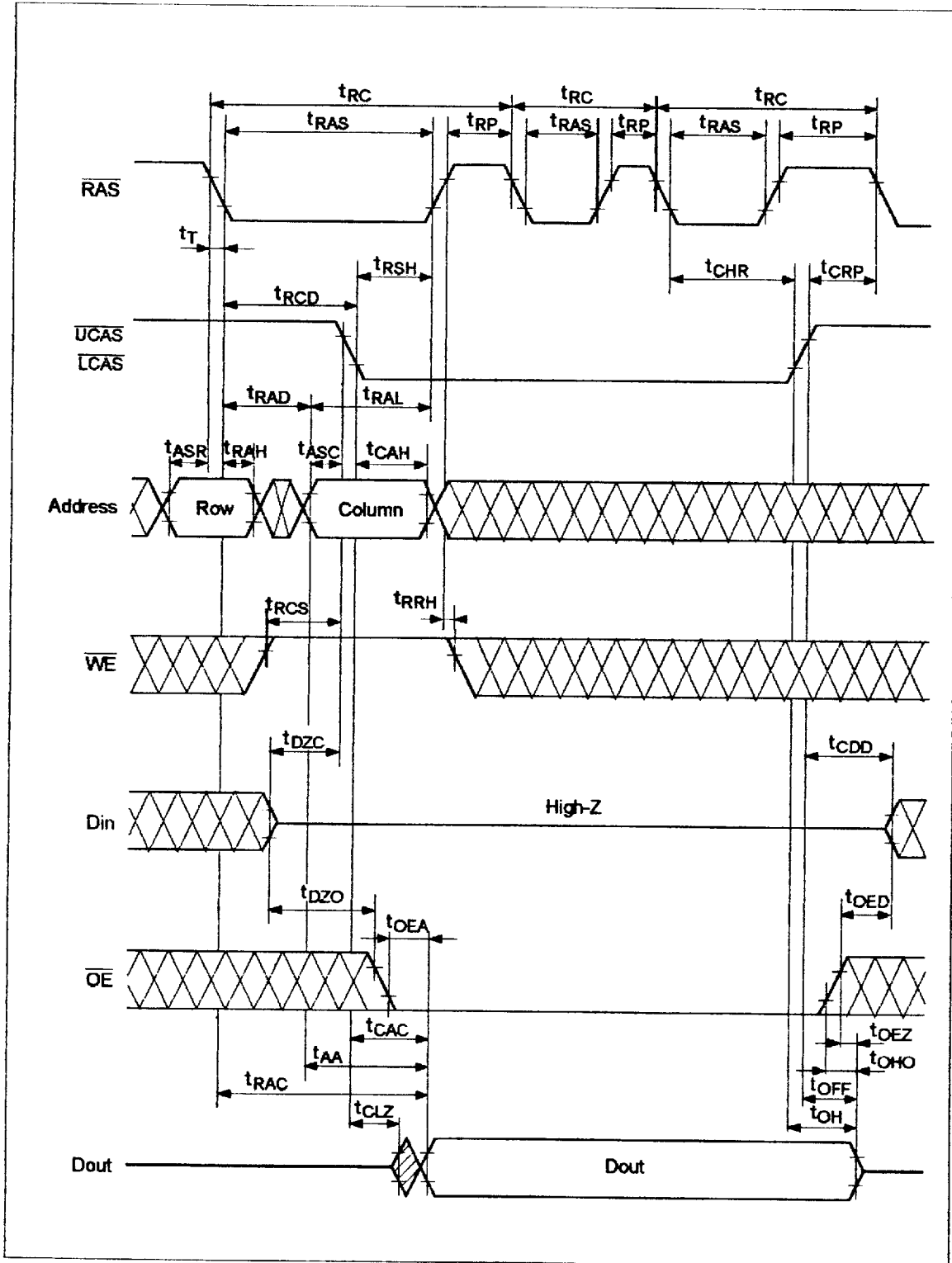


RAS-Only Refresh Cycle

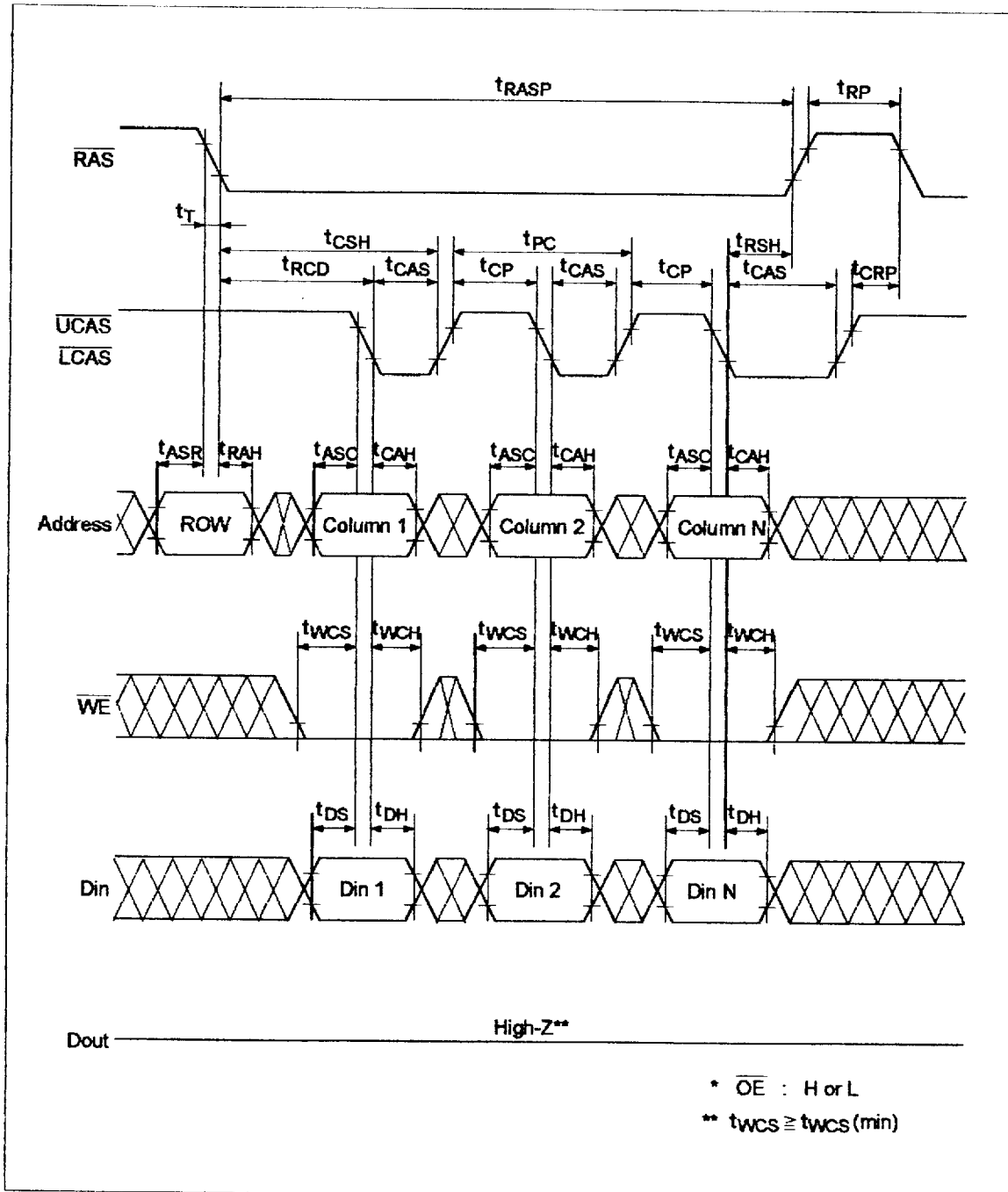
CAS-Before-RAS Refresh Cycle



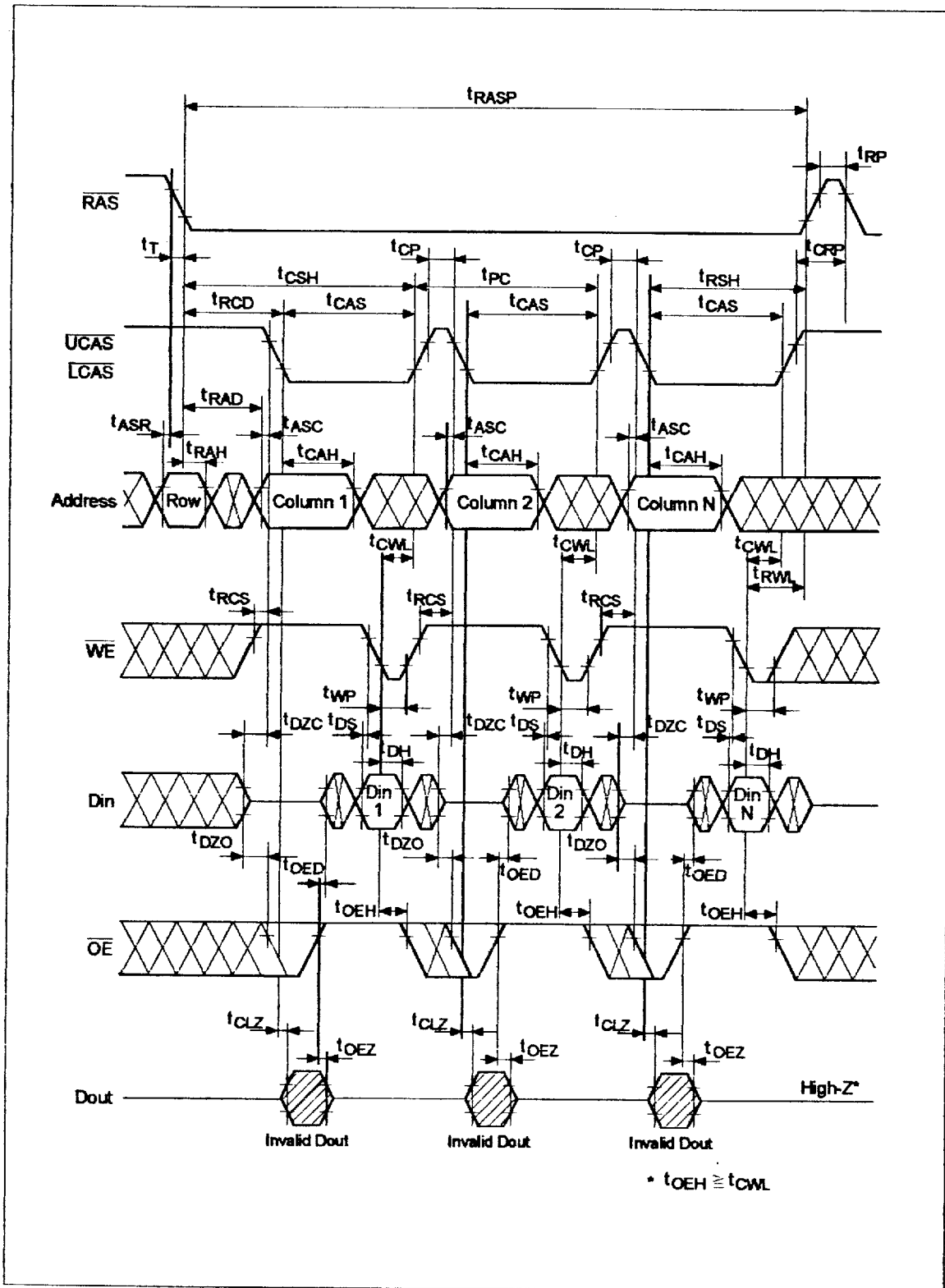
Hidden Refresh Cycle



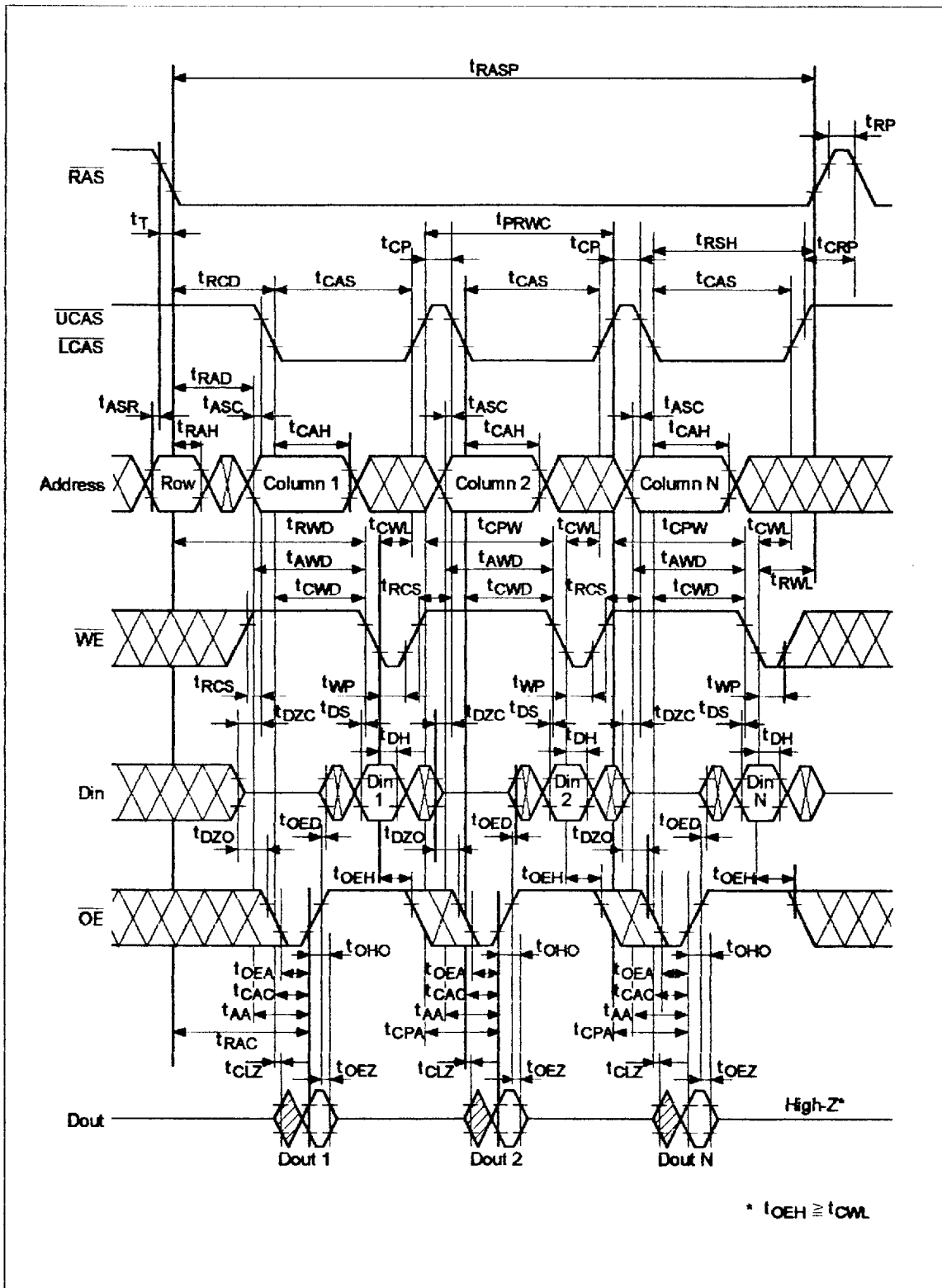
Fast Page Mode Early Write Cycle



Fast Page Mode Delayed Write Cycle *19



Fast Page Mode Read-Modify-Write Cycle *19



Self Refresh Cycle (L-version) *26, 27, 28, 29

