

PRELIMINARY
Notice: This is not a final specification.
 Some parametric limits are subject to change.

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74AS240P is a semiconductor integrated circuit consisting of two blocks of buffers with 3-state inverted outputs and independent output control for each block.

FEATURES

- In-phase output control inputs ($\overline{1OC}$, $\overline{2OC}$)
- High fan-out, 3-state output ($I_{OL}=64mA$, $I_{OH}=-15mA$)
- Wide operating temperature range ($T_a=-20\text{--}+75^\circ C$)

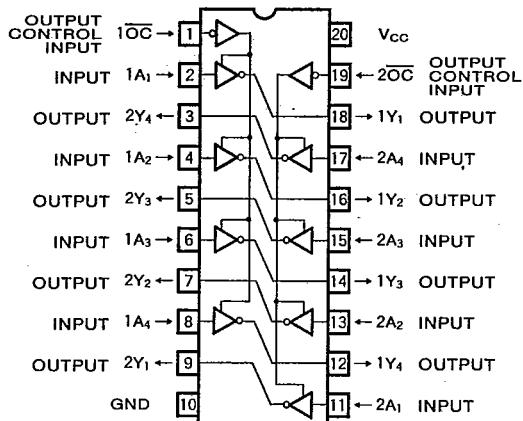
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

When output control input \overline{OC} is low-level, and if input A is low, then output Y is high, if A is high, Y is low. When \overline{OC} is high, $Y_1 \sim Y_4$ are in high-impedance state irrespective of the status of A.

The outputs of all eight buffers can be simultaneously controlled by connecting $\overline{1OC}$ and $\overline{2OC}$.

PIN CONFIGURATION (TOP VIEW)

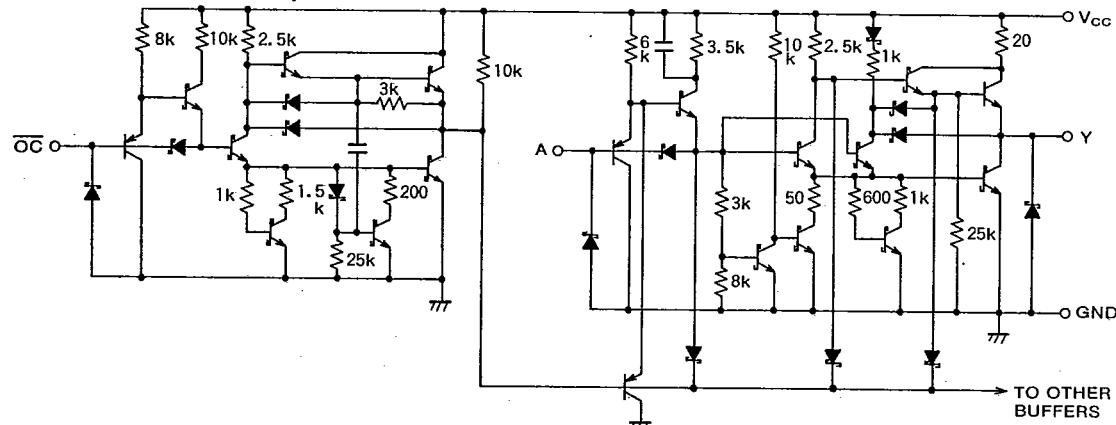
Outline 20P4

FUNCTION TABLE (Note 1)

Inputs		Output
A	\overline{OC}	Y
L	L	H
H	L	L
X	H	Z

Note 1: Z : High-impedance state

X : Irrelevant

CIRCUIT SCHEMATIC (EACH BUFFER)UNIT : Ω

MITSUBISHI ASTTLs

M74AS240P

6249827 MITSUBISHI (DGTL LOGIC)

91D 12202 DT-52-07

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (INVERTED)**ABSOLUTE MAXIMUM RATINGS** ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		-0.5 ~ +7	V
V_I	Input voltage		-0.5 ~ +7	V
V_O	Output voltage	High-level state or high-impedance state	-0.5 ~ +5.5	V
T_{opr}	Operating free-air ambient temperature range		-20 ~ +75	$^\circ\text{C}$
T_{stg}	Storage temperature range		-65 ~ +150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		-15	mA
I_{OL}	Low-level output current	0		64	mA
T_{opr}	Operating free-air ambient temperature range	-20		+75	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
V_{IC}	Input clamp voltage	$V_{CC}=4.5\text{V}, I_{IC}=-18\text{mA}$			-1.2	V
V_{OH}	High-level output voltage	$V_{CC}=4.5\text{V} \sim 5.5\text{V}, I_{OH}=-2\text{mA}$	$V_{CC}-2$			V
		$V_{CC}=4.5\text{V}$	$I_{OH}=-3\text{mA}$	2.4	3.4	
			$I_{OH}=-15\text{mA}$	2.4		
V_{OL}	Low-level output voltage	$V_{CC}=4.5\text{V}, I_{OL}=64\text{mA}$			0.55	V
I_{OZH}	Off-state high-level output current	$V_{CC}=5.5\text{V}, V_O=2.7\text{V}$			50	μA
I_{OZL}	Off-state low-level output current	$V_{CC}=5.5\text{V}, V_O=0.4\text{V}$			-50	μA
I_I	Input current at maximum voltage	$V_{CC}=5.5\text{V}, V_I=7\text{V}$			0.1	mA
I_{IH}	High-level input current	$V_{CC}=5.5\text{V}, V_I=2.7\text{V}$			20	μA
I_{IL}	Low-level input current	$V_{CC}=5.5\text{V}, V_I=0.4\text{V}$			-0.5	mA
I_O	Output current	$V_{CC}=5.5\text{V}, V_O=2.25\text{V}$	-50		-150	mA
I_{CCH}	Supply current, all outputs high	$V_{CC}=5.5\text{V}$		11	17	mA
I_{CCL}	Supply current, all outputs low	$V_{CC}=5.5\text{V}$		51	75	mA
I_{CCZ}	Supply current, all outputs disabled	$V_{CC}=5.5\text{V}$		24	38	mA

*: All typical values are at $V_{CC}=5\text{V}$, $T_a=25^\circ\text{C}$.

MITSUBISHI ASTTLs

M74AS240P

6249827 MITSUBISHI (DGTL LOGIC)

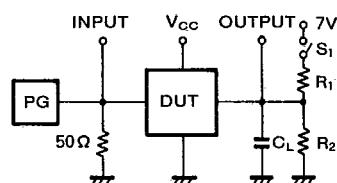
91D 12203 DT-52-07

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (INVERTED)**SWITCHING CHARACTERISTICS**

Symbol	Parameter	Test conditions/Limits						Unit	
		V _{CC} =4.5~5.5V C _L =50pF R ₁ =500Ω R ₂ =500Ω							
		T _A =0~70°C			T _A =-20~+75°C				
t _{PLH}	Propagation time	Input A	Output Y	Min 2	Typ* 6.5	Max 2	Min 7	ns	
t _{PHL}				2	5.7	2	6		
t _{PZH}	Output enable time	OC	Y	2	6.4	2	7	ns	
t _{PZL}				2	9	2	9.5		
t _{PHZ}	Output disable time	OC	Y	2	5	2	5.5	ns	
t _{PLZ}				2	9.5	2	10.5		

*: All typical values are at V_{CC}=5V, T_A=25°C.

Note 2: Measurement circuit

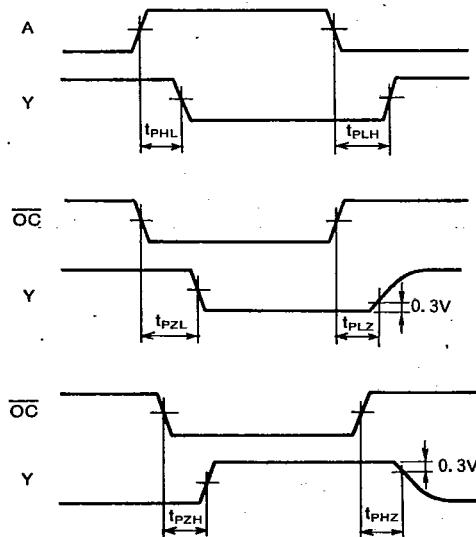


(1) The pulse generator (PG) has the following characteristics:

PRR≤1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_o=50Ω

(2) C_L includes probe and jig capacitance.

Parameter	S ₁
t _{PLH}	Open
t _{PHL}	Open
t _{PZH}	Open
t _{PZL}	Closed
t _{PHZ}	Open
t _{PLZ}	Closed

TIMING DIAGRAM (Reference level=1.3V)

PACKAGE OUTLINES

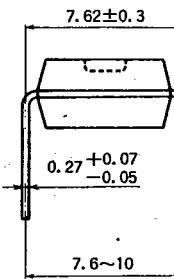
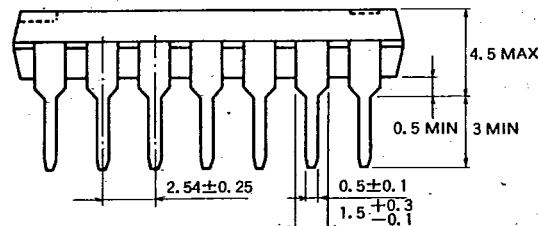
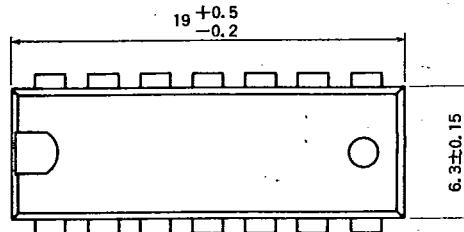
6249827 MITSUBISHI (DGTL LOGIC)

91D 12170 D

T-90-20

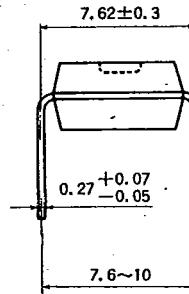
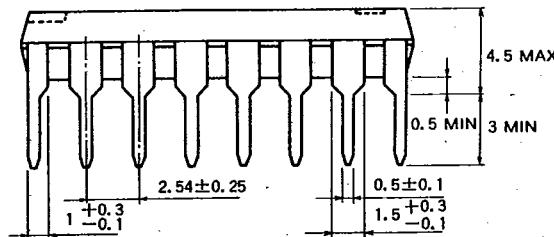
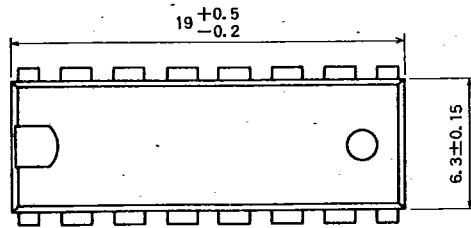
TYPE 14P4 14-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIP

Dimension in mm



PACKAGE OUTLINES

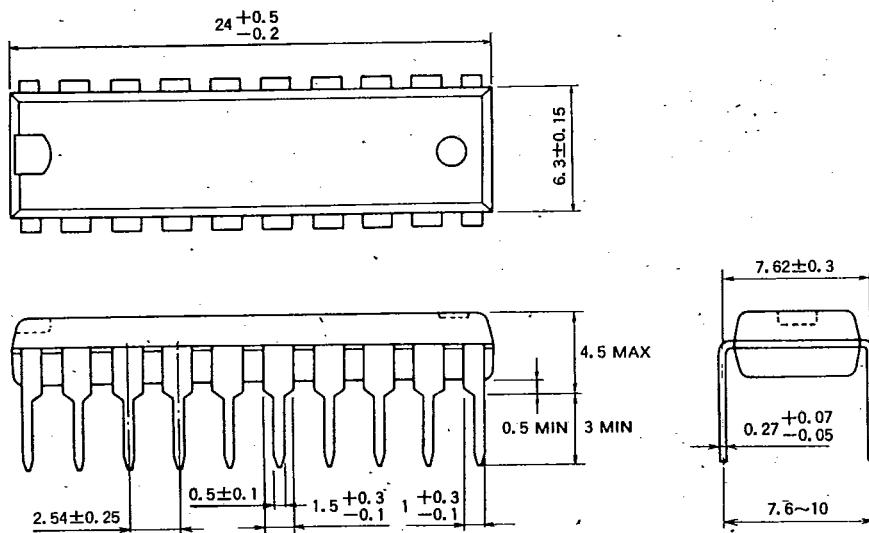
6 MITSUBISHI {DGTL LOGIC} GIC)

91D 12171 D

T-90-20

TYPE 20P4 20-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 24P4D 24-PIN MOLDED PLASTIC DIP

Dimension in mm

