FEMTOCLOCKS™ CRYSTAL-TO-LVDS FREQUENCY SYNTHESIZER

ICS844003

General Description

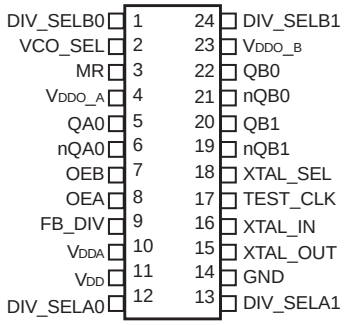
The ICS844003 is a 3 differential output LVDS Synthesizer designed to generate Ethernet reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from IDT. Using a 31.25MHz or 26.041666MHz, 18pF parallel resonant crystal, the following frequencies can be generated based on the settings of four frequency select pins (DIV_SEL[A1:A0], DIV_SEL[B1:B0]): 625MHz, 312.5MHz, 156.25MHz, and 125MHz. The ICS844003 has two output banks, Bank A with one differential LVDS output pair and Bank B with two differential LVDS output pairs.

The two banks have their own dedicated frequency select pins and can be independently set for the frequencies mentioned above. The ICS844003 uses IDT's 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Ethernet jitter requirements. The ICS844003 is packaged in a small 24-pin TSSOP package.

Features

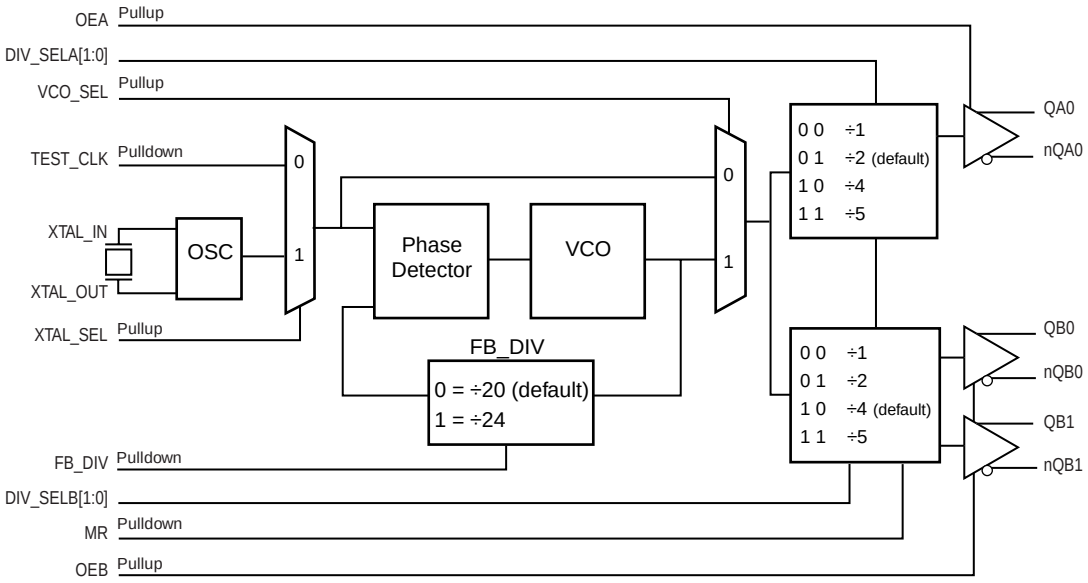
- Three LVDS outputs on two banks, A Bank with one LVDS pair and B Bank with 2 LVDS output pairs
- Using a 31.25MHz or 26.041666MHz crystal, the two output banks can be independently set for 625MHz, 312.5MHz, 156.25MHz or 125MHz
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- VCO range: 560MHz to 700MHz
- RMS phase jitter @ 156.25MHz (1.875MHz - 20MHz): 0.63ps (typical)
- 3.3V output supply mode
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS5) and lead-free (RoHS 6) packages

Pin Assignment



ICS844003
24-Lead TSSOP
4.40mm x 7.8mm x 0.92mm package body
G Package
Top View

Block Diagram



The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1 24	DIV_SELB0 DIV_SELB1	Input	Pulldown	Division select pin for Bank B. Default = Low. LVCMOS/LVTTL interface levels.
2	VCO_SEL	Input	Pullup	VCO select pin. When Low, the PLL is bypassed and the crystal reference or TEST_CLK (depending on XTAL_SEL setting) are passed directly to the output dividers. Has an internal pullup resistor so the PLL is not bypassed by default. LVCMOS/LVTTL interface levels.
3	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. Has an internal pulldown resistor so the power-up default state of outputs and dividers are enabled. LVCMOS/LVTTL interface levels.
4	V_{DDO_A}	Power		Output supply pin for Bank A outputs.
5, 6	QA0, nQA0	Ouput		Differential output pair. LVDS interface levels.
7	OEB	Input	Pullup	Output enable Bank B. Active High outputs are enable. When logic HIGH, the output pairs on Bank B are enabled. When logic LOW, the output pairs are in a high impedance state. Has an internal pullup resistor so the default power-up state of outputs are enabled. LVCMOS/LVTTL interface levels.
8	OEA	Input	Pullup	Output enable Bank A. Active High output enable. When logic HIGH, the output pair in Bank A is enabled. When logic LOW, the output pair is in a high impedance state. Has an internal pullup resistor so the default power-up state of output is enabled. LVCMOS/LVTTL interface levels.
9	FB_DIV	Input	Pulldown	Feedback divide select. When Low (default), the feedback divider is set for ÷20. When HIGH, the feedback divider is set for ÷24. LVCMOS/LVTTL interface levels.
10	V_{DDA}	Power		Analog supply pin.
11	V_{DD}	Power		Core supply pin.
12 13	DIV_SELA0 DIV_SELA1	Input	Pullup	Division select pin for Bank A. Default = HIGH. LVCMOS/LVTTL interface levels.
14	GND	Power		Power supply ground.
15, 16	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input. XTAL_IN is also the overdrive pin if you want to overdrive the crystal circuit with a single-ended reference clock.
17	TEST_CLK	Input	Pulldown	Single-ended reference clock input. Has an internal pulldown resistor to pull to low state by default. Can leave floating if using the crystal interface. LVCMOS/LVTTL interface levels.
18	XTAL_SEL	Input	Pullup	Crystal select pin. Selects between the single-ended TEST_CLK or crystal interface. Has an internal pullup resistor so the crystal interface is selected by default. LVCMOS/LVTTL interface levels.
19, 20	nQB1, QB1	Output		Differential output pair. LVDS interface levels.
21, 22	nQB0, QB0	Output		Differential output pair. LVDS interface levels.
23	V_{DDO_B}	Power		Output supply pin for Bank B outputs.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

TABLE 3A. BANK A FREQUENCY TABLE

Inputs				Feedback Divider	Bank A Output Divider	M/N Multiplication Factor	QA0/nQA0 Output Frequency (MHz)
Crystal Frequency (MHz)	DIV_SELA1	DIV_SELA0	FB_DIV				
31.25	0	0	0	20	1	20	625
31.25	0	1	0	20	2	10	312.5
31.25	1	0	0	20	4	5	156.25
31.25	1	1	0	20	5	4	125
26.041666	0	0	1	24	1	24	625
26.041666	0	1	1	24	2	12	312.5
26.041666	1	0	1	24	4	6	156.25
26.041666	1	1	1	24	5	64.8	125

TABLE 3B. BANK B FREQUENCY TABLE

Inputs				Feedback Divider	Bank B Output Divider	M/N Multiplication Factor	QB0/nQB0 Output Frequency (MHz)
Crystal Frequency (MHz)	DIV_SELB1	DIV_SELB0	FB_DIV				
31.25	0	0	0	20	1	20	625
31.25	0	1	0	20	2	10	312.5
31.25	1	0	0	20	4	5	156.25
31.25	1	1	0	20	5	4	125
26.041666	0	0	1	24	1	24	625
26.041666	0	1	1	24	2	12	312.5
26.041666	1	0	1	24	4	6	156.25
26.041666	1	1	1	24	5	4.8	125

TABLE 3C. OUTPUT BANK CONFIGURATION SELECT FUNCTION TABLE

Inputs		Outputs
DIV_SELA1	DIV_SELA0	QA
0	0	÷1
0	1	÷2
1	0	÷4
1	1	÷5

Inputs		Outputs
DIV_SELB1	DIV_SELB0	QB
0	0	÷1
0	1	÷2
1	0	÷4
1	1	÷5

TABLE 3D. FEEDBACK DIVIDER CONFIGURATION SELECT FUNCTION TABLE

Inputs	
FB_DIV	Feedback Divide
0	÷20
1	÷24

TABLE 3E. OEA SELECT FUNCTION TABLE

Inputs	Outputs	
OEA	QA0	nQA0
0	LOW	HIGH
1	Active	Active

TABLE 3F. OEB SELECT FUNCTION TABLE

Inputs	Outputs	
OEB	QB0:QB1	nQB0:nQB1
0	LOW	HIGH
1	Active	Active

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	70°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO\_A} = V_{DDO\_B}$ = 3.3V±5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	V_{DD}	V
$V_{DDO\_A, B}$	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			99		mA
I_{DDA}	Analog Supply Current			10		mA
$I_{DDO\_A, B}$	Output Supply Current			52		mA

Table 4B. LVCMOS / LVTTL DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO\_A} = V_{DDO\_B}$ = 3.3V±5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	TEST_CLK, MR, FB_DIV DIV_SELA1, DIV_SELB0	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		DIV_SELB1, DIV_SELA0, VCO_SEL, XTAL_SEL, OEA, OEB	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	TEST_CLK, MR, FB_DIV DIV_SELA1, DIV_SELB0	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		DIV_SELB1, DIV_SELA0, VCO_SEL, XTAL_SEL, OEA, OEB	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

TABLE 4C. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO\_A} = V_{DDO\_B} = 3.3V±5\%$, $T_A = T_A = 0°C$ TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			350		mV
ΔV_{OD}	V_{OD} Magnitude Change			0	40	mV
V_{OS}	Offset Voltage			1.4		V
ΔV_{OS}	V_{OS} Magnitude Change			0	50	mV

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter		Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental			
Frequency	FB_DIV = ÷20		28		35	MHz
	FB_DIV = ÷24		23.33		29.16	MHz
Equivalent Series Resistance (ESR)					50	Ω
Shunt Capacitance					7	pF
Drive Level					1	mW

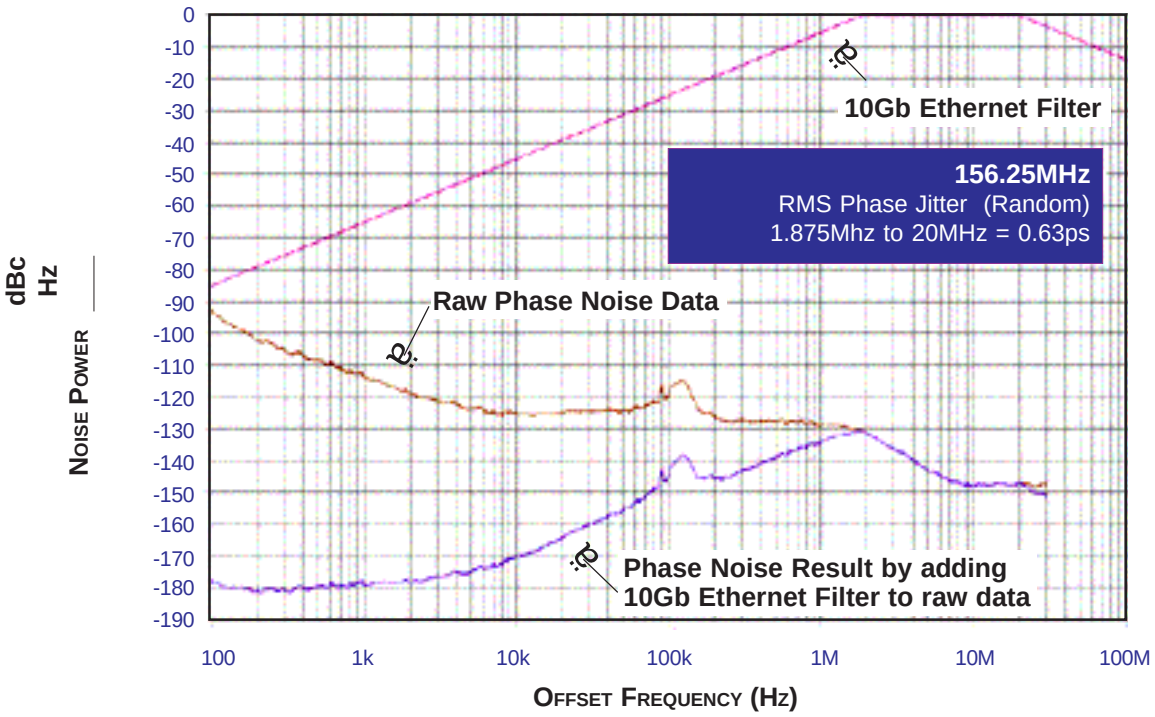
NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO\_A} = V_{DDO\_B} = 3.3V±5\%$, $T_A = 0°C$ TO 70°C

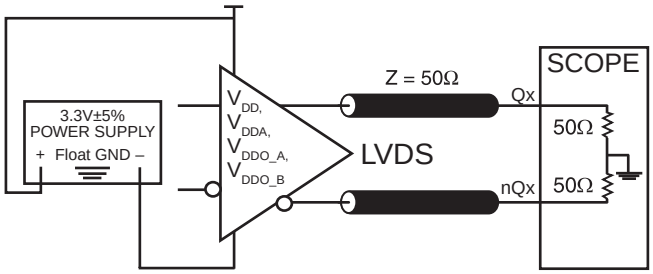
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Range	Output Divider = ÷1	560		700	MHz
		Output Divider = ÷2	280		350	MHz
		Output Divider = ÷4	140		175	MHz
		Output Divider = ÷5	112		140	MHz
*t*sk(b)	Bank Skew, NOTE 1			3		ps
*t*sk(o)	Output Skew; NOTE 2, 4	Outputs @ Same Frequency		15		ps
		Outputs @ Different Frequencies		30		ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 3	625MHz (1.875MHz - 20MHz)		0.55		ps
		312.5MHz (1.875MHz - 20MHz)		0.59		ps
		156.25MHz (1.875MHz - 20MHz)		0.63		ps
		125MHz (1.875MHz - 20MHz)		0.64		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		325		ps
odc	Output Duty Cycle			50		%

NOTE 1: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 2: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Please refer to the Phase Noise Plots.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

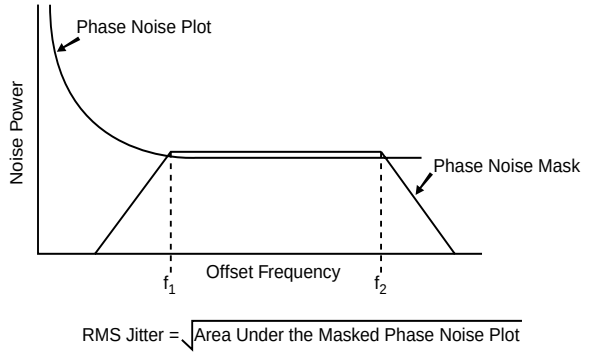
TYPICAL PHASE NOISE AT 156.25MHZ



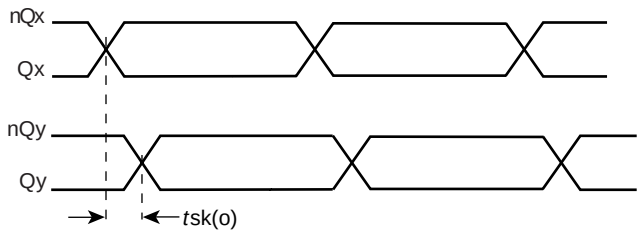
PARAMETER MEASUREMENT INFORMATION



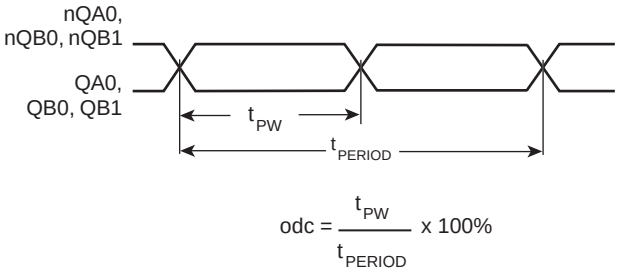
LVDS 3.3V OUTPUT LOAD AC TEST CIRCUIT



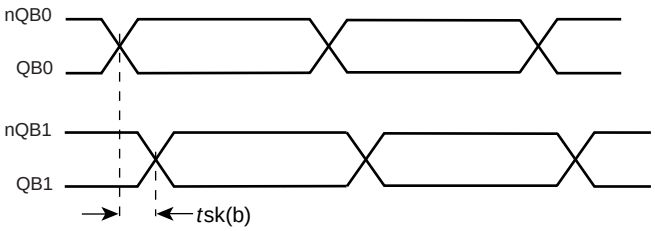
RMS PHASE JITTER



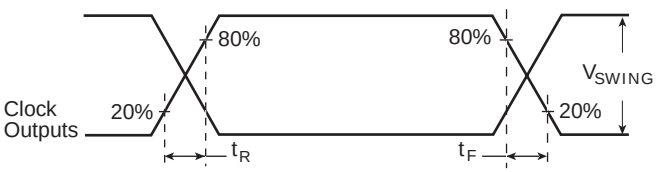
OUTPUT SKEW



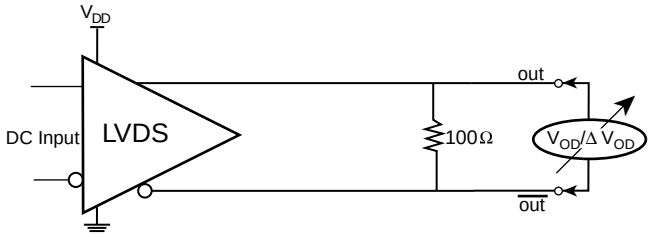
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



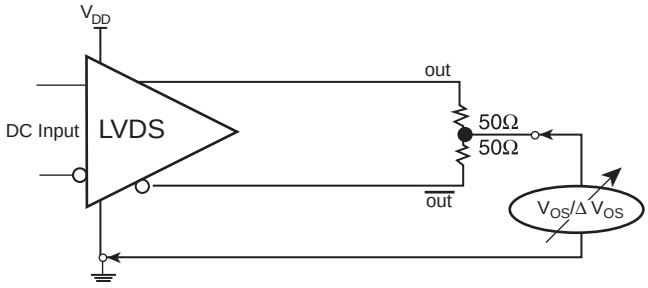
BANK SKEW



OUTPUT RISE/FALL TIME



DIFFERENTIAL OUTPUT VOLTAGE SETUP



OFFSET VOLTAGE SETUP

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS844003 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDOx} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin.

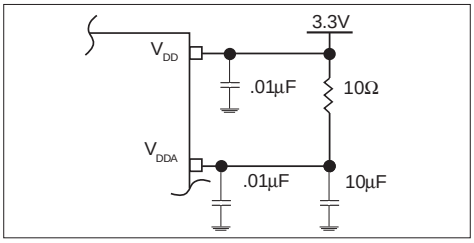


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS844003 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 31.25MHz or 26.041666MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

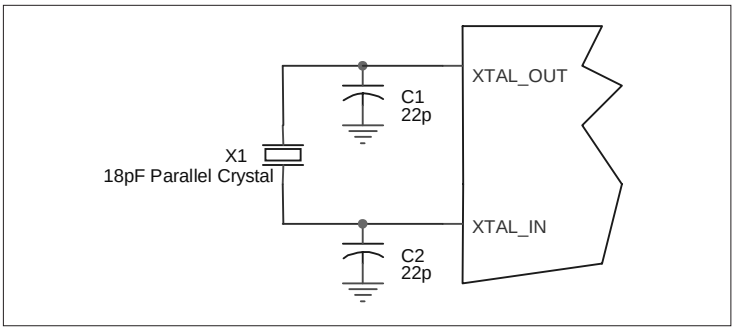


Figure 2. CRYSTAL INPUT INTERFACE

LVCMOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

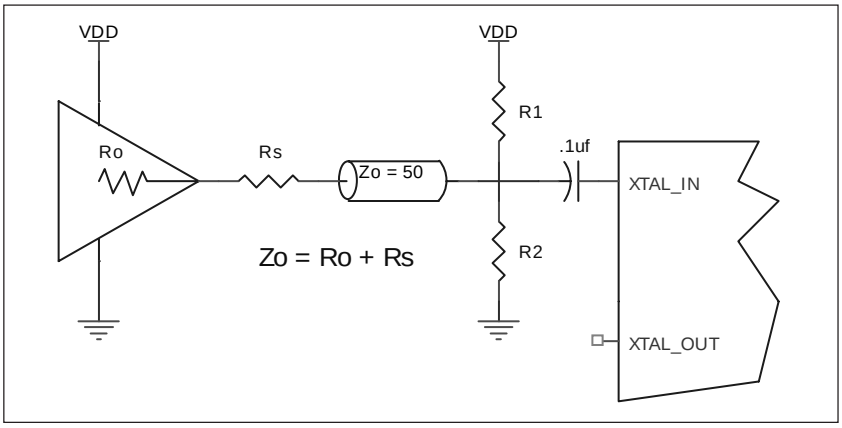


FIGURE 3. GENERAL DIAGRAM FOR LVCMOS DRIVER TO XTAL INPUT INTERFACE

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUT:
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

TEST_CLK INPUT:
For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the TEST_CLK to ground.

LVCMOS CONTROL PINS:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVDS
All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

3.3V LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input.

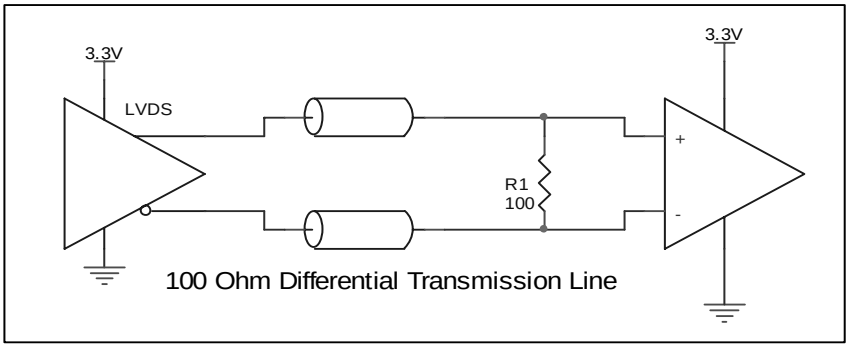


Figure 4. Typical LVDS Driver Termination

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS844003.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS844003 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power (core)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (99mA + 10mA) = **377.68mW**
- Power (outputs)$_{MAX}$ = V_{DDO_MAX} * I_{DDO_MAX} = 3.465V * 52mA = **180.18mW**

Total Power$_{_MAX}$ = 377.68mW + 180.18mW = **557.86mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 65°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.558W * 65°C/W = 105.9°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 24-LEAD TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP, EPAD

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

TRANSISTOR COUNT

The transistor count for ICS844003 is: 3394

PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

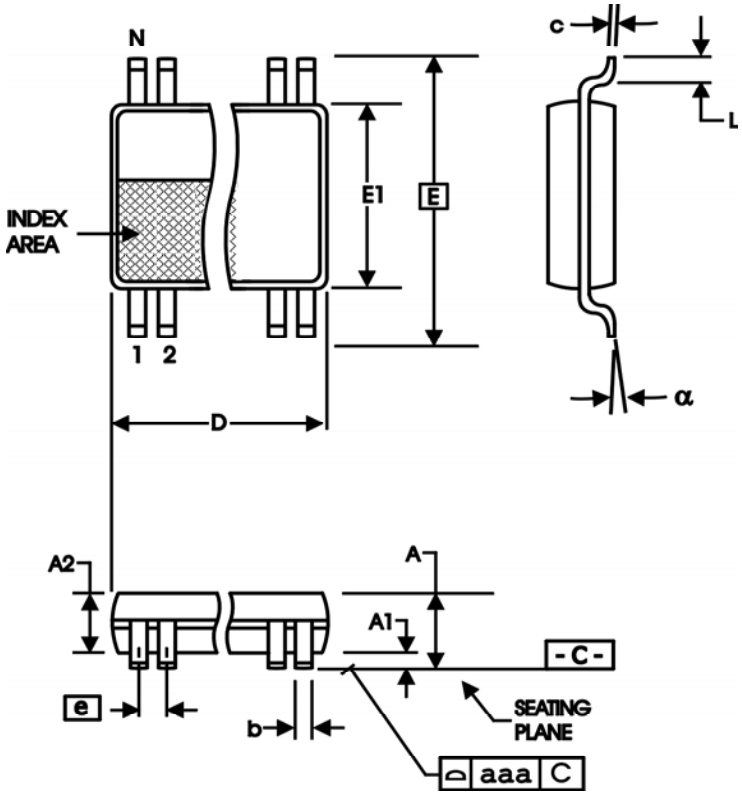


TABLE 9. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844003AG	ICS844003AG	24 Lead TSSOP	tube	0°C to 70°C
844003AGT	ICS844003AG	24 Lead TSSOP	2500 tape & reel	0°C to 70°C
844003AGLF	TBD	24 Lead "Lead-Free" TSSOP	tube	0°C to 70°C
844003AGTLF	TBD	24 Lead "Lead-Free" TSSOP	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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