54F/74F253

Dual 4-Input Multiplexer With 3-State Outputs

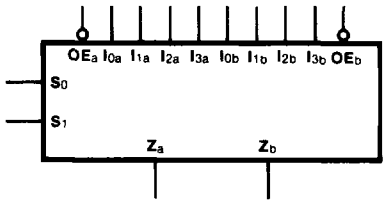
Description

The 'F253 is a dual 4-input multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems.

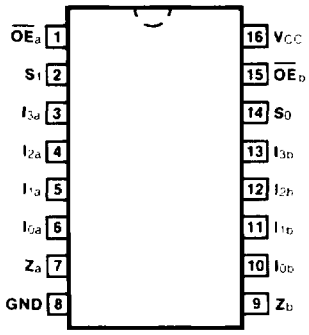
- **FAST Process for High Speed**
- **Multifunction Capability**
- **Non-Inverting 3-State Outputs**

Ordering Code: See Section 5

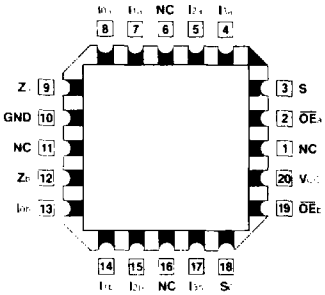
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
I_{0a}-I_{3a}	Side A Data Inputs	0.5/0.375
I_{0b}-I_{3b}	Side B Data Inputs	0.5/0.375
S_0, S_1	Common Select Inputs	0.5/0.375
$\overline{OE}_a$	Side A Output Enable Input (Active LOW)	0.5/0.375
$\overline{OE}_b$	Side B Output Enable Input (Active LOW)	0.5/0.375
Z_a, Z_b	3-State Outputs	75/15 (12.5)

Functional Description

This device contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. This device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$Z_b = \overline{OE}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

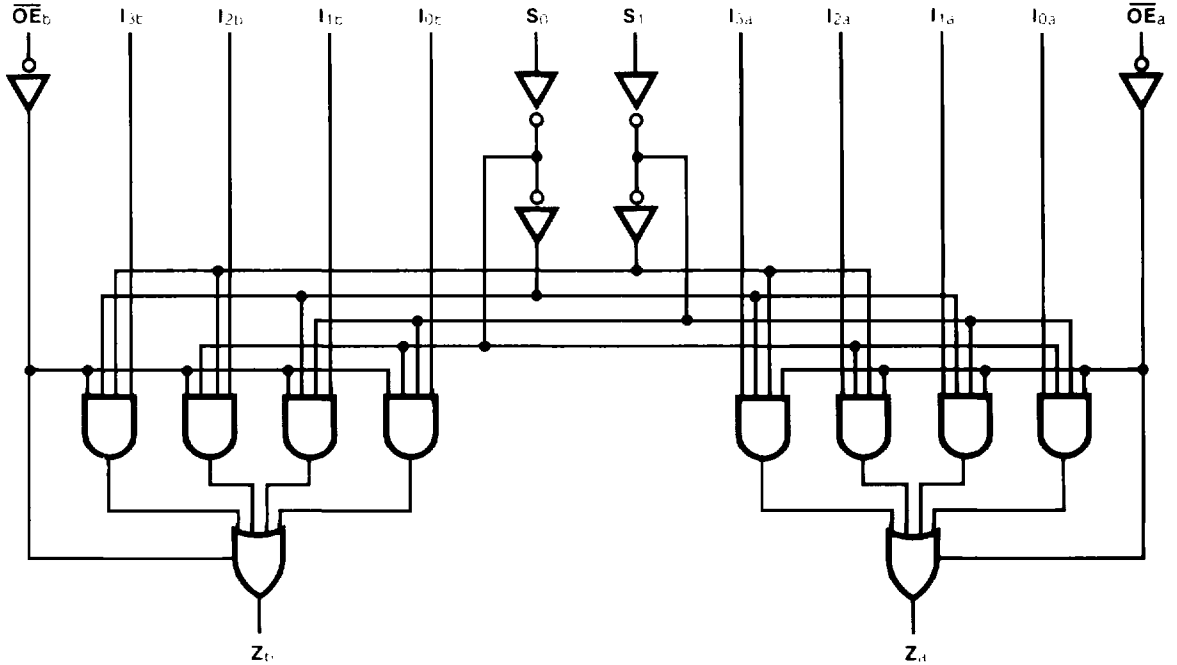
If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

Truth Table

Select Inputs		Data Inputs				Output Enable	Output
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Z
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address Inputs S_0 and S_1 are common to both sections.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCH}	Power Supply Current		11.5	16.0	mA	V_{CC} = Max, $\overline{OE}_n$ = Gnd I_3, S_n = HIGH; I_0-I_2 = Gnd
I_{CCL}			16.0	23.0		V_{CC} = Max I_n, S_n, $\overline{OE}_n$ = Gnd
I_{CCZ}			16.0	23.0		V_{CC} = Max, $\overline{OE}_n$ = HIGH I_n, S_n = Gnd

4

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			54F T_A, V_{CC} = Mil, C_L = 50 pF		74F T_A, V_{CC} = Com, C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_n to Z_n	4.5 3.0	8.5 6.5	11.5 9.0	3.5 2.5	15.0 11.0	4.5 3.0	13.0 10.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay I_n to Z_n	3.0 2.5	5.5 4.5	7.0 6.0	2.5 2.5	9.0 8.0	3.0 2.5	8.0 7.0	ns	3-1 3-4
t_{PZH} t_{PZL}	Output Enable Time	3.0 3.0	6.0 6.0	8.0 8.0	2.5 2.5	10.0 10.0	3.0 3.0	9.0 9.0	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	3.7 4.4	5.0 6.0	2.0 2.0	6.5 8.0	2.0 2.0	6.0 7.0		