INCH-POUND
MIL-M-38510/114B
20 August 2003
SUPERSEDING
MIL-M-38510/114A
09 November 1979

## MILITARY SPECIFICATION

MICROCIRCUITS, LINEAR, BI-FET OPERATIONAL AMPLIFIERS, MONOLITHIC SILICON
Reactivated after 20 August 2003 and may be used for either new or existing design acquisitions.
This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF-38535.

1. SCOPE
1.1 Scope. This specification covers the detail requirements for monolithic silicon, BI-FET operational amplifier microcircuit. Two product assurance classes and a choice of case outlines and lead finishes are provided and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.3)
1.2 Part number. The part number should be in accordance with MIL-PRF-38535, and as specified herein.
1.2.1 Device types. The device types are internally compensated and should be as follows:

Device type
01
02
03
04
05
06

Circuit
Operational amplifier, JFET input, low power Operational amplifier, JFET input, wide band Operational amplifier, JFET input, wide band, undercompensated Operational amplifier, JFET input, low power, low offset Operational amplifier, JFET input, wide band, low offset Operational amplifier, JFET input, wide band, under compensated, low offset
1.2.2 Device class. The device class should be the product assurance level as defined in MIL-PRF-38535.
1.2.3 Case outline. The case outline should be as designated in MIL-STD-1835 and as follows:

| Outline letter |  | Descriptive designator |  | Terminals |
| :---: | :--- | :--- | ---: | :--- |
|  |  |  |  | Package style |
|  |  |  |  |  |
| G |  | MACY1-X8 |  |  |
| H | GDFP1-F10 or CDFP2-F10 |  | 10 |  |
| P | GDIP1-T8 or CDIP2-T8 |  |  | Flat pack |
|  |  | 8 |  | Dual-in-line |

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, 3990 East Broad St., Columbus, OH 43216-5000, or emailed to linear@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at www.dodssp.daps.mil.

### 1.3 Absolute maximum ratings.

| Supply voltage range | $\pm 22 \mathrm{~V}$ |
| :---: | :---: |
| Input voltage range | $\pm 20 \mathrm{~V}$ 1/ |
| Differential input voltage range | $\pm 40 \mathrm{~V}$ |
| Storage temperature range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Output short-circuit duration | Unlimited ${ }^{\text {2/ }}$ |
| Lead temperature (soldering, 60 seconds) | $+300^{\circ} \mathrm{C}$. |
| Junction temperature ( $\mathrm{T}_{\mathrm{J}}$ ) | $+175^{\circ} \mathrm{C}$ 3/ |

### 1.4 Recommended operating conditions.


1.5 Power and thermal characteristics.

| Case outlines | Maximum allowable power <br> dissipation | Maximum <br> $\theta_{\mathrm{JC}}$ | Maximum <br> $\theta_{\mathrm{JA}}$ |
| :---: | :---: | :---: | :---: |
| G | 330 mW at $\mathrm{T}_{\mathrm{A}}=+125^{\circ} \mathrm{C}$ | $40^{\circ} \mathrm{C} / \mathrm{W}$ | $150^{\circ} \mathrm{C} / \mathrm{W}$ |
| H | 330 mW at $\mathrm{T}_{\mathrm{A}}=+125^{\circ} \mathrm{C}$ | $60^{\circ} \mathrm{C} / \mathrm{W}$ | $150^{\circ} \mathrm{C} / \mathrm{W}$ |
| P | 400 mW at $\mathrm{T}_{\mathrm{A}}=+125^{\circ} \mathrm{C}$ | $35^{\circ} \mathrm{C} / \mathrm{W}$ | $120^{\circ} \mathrm{C} / \mathrm{W}$ |

## 2. APPLICABLE DOCUMENTS

### 2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Departments of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

## DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.
DEPARTMENT OF DEFENSE STANDARDS

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MIL-STD-883 - Test Method Standard for Microelectronics.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.
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(Copies of these documents are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.
2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein the text of this document shall takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ The absolute maximum negative input voltage is equal to the negative power supply voltage.
$\underline{\underline{2} / S h o r t ~ c i r c u i t ~ m a y ~ b e ~ t o ~ g r o u n d ~ o r ~ e i t h e r ~ s u p p l y . ~ R a t i n g ~ a p p l i e s ~ t o ~}+125^{\circ} \mathrm{C}$ case temperature or $+75^{\circ} \mathrm{C}$ ambient temperature.
3/ For short term test (in the specific burn-in and life test configuration when required and up to 168 hours maximum), $\mathrm{T}_{\mathrm{J}}=275^{\circ} \mathrm{C}$.

## 3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.4).
3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.
3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.
3.3.1 Terminal connections. The terminal connections shall be as specified on figure 1.
3.3.2 Schematic circuits. The schematic circuits shall be maintained by the manufacturer and made available to the qualifying activity and the preparing activity (DSCC-VA) upon request.
3.3.3 Case outlines. The case outlines shall be as specified in 1.2.3.
3.4 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).
3.5 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended ambient operating temperature range, unless otherwise specified.
3.5.1 Offset null circuits. The nulling inputs shall be capable of being nulled 1 mV beyond the specified offset voltage limits for $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C}$ using the circuit of figure 2 .
3.5.2 Instability oscillations. The devices shall be free of oscillations when operated in the test circuits of this specification.
3.6 Rebonding. Rebonding shall be in accordance with MIL-PRF-38535.
3.7 Electrical test requirements. Electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.
3.8 Marking. Marking shall be in accordance with MIL-PRF-38535.
3.9 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 49 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+125^{\circ} \mathrm{C}$ <br> unless otherwise specified <br> See figure 3 | Group A subgroups | Device type | Limits |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | Min | Max |  |
| Input offset voltage | VIO | $\pm \mathrm{V}_{\mathrm{CC}}= \pm 5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=0 \mathrm{~V}$ | 1 | $\begin{gathered} \hline 01,02, \\ 03 \end{gathered}$ | -5 | 5 | mV |
|  |  |  |  | $\begin{gathered} 04,05, \\ 06 \end{gathered}$ | -2 | 2 |  |
|  |  | $\begin{aligned} & \pm \mathrm{V}_{\mathrm{CC}}= \pm 20 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{CM}}= \pm 15 \mathrm{~V}, 0 \mathrm{~V} \end{aligned}$ | 2,3 | $\begin{gathered} \hline 01,02, \\ 03 \end{gathered}$ | -7 | 7 |  |
|  |  |  |  | $\begin{gathered} 04,05, \\ 06 \end{gathered}$ | -2.5 | 2.5 |  |
| Input offset voltage temperature sensitivity | $\begin{aligned} & \Delta \mathrm{V}_{\mathrm{IO}} / \\ & \Delta \mathrm{T} \end{aligned}$ | $\pm \mathrm{V}_{\mathrm{CC}}= \pm 20 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=0 \mathrm{~V}$ | 1,2,3 | $\begin{gathered} \hline 01,02, \\ 03 \end{gathered}$ | -30 | 30 | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
|  |  |  |  | $\begin{gathered} \hline 04,05, \\ 06 \end{gathered}$ | -10 | 10 |  |
| Input offset current | ${ }_{1} \mathrm{O}$ | $\pm \mathrm{V}_{\mathrm{CC}}= \pm 20 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=0 \mathrm{~V}$ | $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ | All | -20 | 20 | pA |
|  |  |  | $\begin{gathered} \mathrm{T}_{\mathrm{J}}= \\ +125^{\circ} \mathrm{C} \end{gathered}$ |  | -20 | 20 | nA |
| Input bias current $\underline{1 / 2} /$ | ${ }^{+1} 1 \mathrm{~B}$ | $\begin{aligned} & \pm \mathrm{V}_{\mathrm{CC}}= \pm 20 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{CM}}=+15 \mathrm{~V}, \mathrm{t} \leq 25 \mathrm{~ms} \end{aligned}$ | $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ | All | -100 | 3500 | pA |
|  |  |  | $\begin{gathered} \mathrm{T}_{\mathrm{J}}= \\ +125^{\circ} \mathrm{C} \end{gathered}$ |  | -10 | 60 | nA |
|  | $-l_{\text {IB }}$ <br> 3/ | $\begin{aligned} & \pm \mathrm{V}_{\mathrm{CC}}= \pm 15 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CM}}=+10 \mathrm{~V}, \mathrm{t} \leq 25 \mathrm{~ms} \end{aligned}$ | $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ |  | -100 | 300 | pA |
|  |  |  | $\begin{gathered} \mathrm{T}_{\mathrm{J}}= \\ +125^{\circ} \mathrm{C} \end{gathered}$ |  | -10 | 50 | nA |
|  |  | $\begin{aligned} & \pm \mathrm{V}_{\mathrm{CC}}= \pm 20 \mathrm{~V} \\ & -15 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CM}} \leq 0 \mathrm{~V} \\ & \mathrm{t} \leq 25 \mathrm{~ms} \end{aligned}$ | $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ |  | -100 | 100 | pA |
|  |  |  | $\begin{gathered} \mathrm{T}_{\mathrm{J}}= \\ +125^{\circ} \mathrm{C} \end{gathered}$ |  | -10 | 50 | nA |
| Power supply rejection ratio | +PSRR | $+\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V},-\mathrm{V}_{\mathrm{CC}}=-20 \mathrm{~V}$ | 1,2,3 | All | 85 |  | dB |
|  | -PSRR | $+\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V},-\mathrm{V}_{\mathrm{CC}}=-10 \mathrm{~V}$ |  |  | 85 |  |  |
| Input voltage common 4/ mode rejection | CMR | $\begin{aligned} & \pm \mathrm{V}_{\mathrm{CC}}= \pm 20 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IN}}= \pm 15 \mathrm{~V} \end{aligned}$ | 1,2,3 | All | 85 |  | dB |
| Adjustment for input offset voltage | VIO ADJ(+) | $\pm \mathrm{V}_{\mathrm{CC}}= \pm 20 \mathrm{~V}$ | 1,2,3 | All | +8 |  | mV |
|  | VIO ADJ(-) |  |  |  |  | -8 |  |
| Output short circuit <br> current (for positive <br> output) $\underline{5} /$ | los(+) | $\begin{aligned} & \pm \mathrm{V} \mathrm{CC}= \pm 15 \mathrm{~V}, \mathrm{t} \leq 25 \mathrm{~ms} \\ & \text { (short circuit to ground) } \end{aligned}$ | 1,2,3 | All | -50 |  | mA |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+125^{\circ} \mathrm{C}$ <br> unless otherwise specified <br> See figure 3 | Group A subgroups | Device type | Limits |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | Min | Max |  |
| Output short circuit <br> current (for negative <br> output) $\underline{5} /$ | IOS(-) | $\pm \mathrm{V}_{\mathrm{CC}}= \pm 15 \mathrm{~V}, \mathrm{t} \leq 25 \mathrm{~ms}$ <br> (short circuit to ground) | 1,2,3 | All |  | 50 | mA |
| Supply current | ICC | $\pm \mathrm{V}_{\text {CC }}= \pm 15 \mathrm{~V}$ | 1,2 | 01,04 |  | 4 | mA |
|  |  |  |  | $\begin{aligned} & \hline 02,03, \\ & 05,06 \end{aligned}$ |  | 7 |  |
|  |  |  | 3 | 01,04 |  | 6 |  |
|  |  |  |  | $\begin{aligned} & \hline 02,03, \\ & 05,06 \end{aligned}$ |  | 11 |  |
| Output voltage swing (maximum) | $\mathrm{V}_{\mathrm{OP}}$ | $\pm \mathrm{V}_{\mathrm{CC}}= \pm 20 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega$ | 1,2,3 | All | $\pm 16$ |  | V |
|  |  | $\pm \mathrm{V}_{\mathrm{CC}}= \pm 20 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  | $\pm 15$ |  |  |
| Open loop voltage  <br> gain (single ended) $\underline{6} /$ | AVs(+) <br> Avs(-) | $\begin{aligned} & \pm \mathrm{V}_{\mathrm{CC}}= \pm 20 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \\ & \mathrm{~V}_{\mathrm{OUT}}= \pm 15 \mathrm{~V} \end{aligned}$ | 1 | All | 50 |  | V/mV |
|  |  |  | 2,3 |  | 25 |  |  |
| Open loop voltage gain (single ended) | Avs | $\begin{aligned} & \pm \mathrm{V}_{\mathrm{CC}}= \pm 5 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \\ & \mathrm{~V}_{\mathrm{OUT}}= \pm 2 \mathrm{~V} \end{aligned}$ | 1 | All | 10 |  | V/mV |
| Transient response, rise time | TR (tr) | $\pm \mathrm{V}_{\mathrm{CC}}= \pm 15 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ | 4,5,6 | 01,04 |  | 150 | ns |
|  |  | $\begin{aligned} & C_{L}=100 \mathrm{pF}, \mathrm{~V}_{\mathrm{IN}}=50 \mathrm{mV} \\ & A V=1, \text { see figure } 4 \end{aligned}$ |  | 02,05 |  | 100 |  |
|  |  | $\begin{aligned} & \pm \mathrm{V}_{\mathrm{CC}}= \pm 15 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \\ & C_{\mathrm{L}}=100 \mathrm{pF}, \mathrm{~V}_{\mathrm{IN}}=50 \mathrm{mV} \\ & \mathrm{AV}=5, \text { see figure } 4 \end{aligned}$ |  | 03,06 |  | 450 |  |
| Transient response, overshoot | $\mathrm{TR}_{\text {(os) }}$ | $\begin{aligned} & \pm \mathrm{V}_{\mathrm{CC}}= \pm 15 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \\ & \mathrm{C}_{\mathrm{L}}=100 \mathrm{pF}, \mathrm{~V}_{\mathrm{IN}}=50 \mathrm{mV} \\ & \mathrm{AV}=1, \text { see figure } 4 \end{aligned}$ |  | $\begin{aligned} & \hline 01,02, \\ & 04,05 \end{aligned}$ |  | 40 | \% |
|  |  | $\begin{aligned} & \pm \mathrm{V}_{\mathrm{CC}}= \pm 15 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \\ & \mathrm{C}_{\mathrm{L}}=100 \mathrm{pF}, \mathrm{~V}_{\mathrm{IN}}=50 \mathrm{mV} \\ & \mathrm{AV}=5, \text { see figure } 4 \end{aligned}$ |  | 03,06 |  | 25 |  |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+125^{\circ} \mathrm{C}$ unless otherwise specified <br> See figure 3 | Group A subgroups | Device type | Limits |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | Min | Max |  |
| Slew rate | $\mathrm{SR}(+)$ <br> and SR(-) | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}= \pm 5 \mathrm{~V}, \pm \mathrm{V}_{\mathrm{CC}}= \pm 15 \mathrm{~V} \\ & \mathrm{AV}=1, \text { see figure } 4 \end{aligned}$ | 1 | 01 | 2 |  | $\mathrm{V} / \mu \mathrm{s}$ |
|  |  |  |  | 02 | 7.5 |  |  |
|  |  |  |  | 04 | 3 |  |  |
|  |  |  |  | 05 | 10 |  |  |
|  |  |  | 2,3 | 01 | 1 |  |  |
|  |  |  |  | 02 | 5 |  |  |
|  |  |  |  | 04 | 1.5 |  |  |
|  |  |  |  | 05 | 7 |  |  |
|  |  | $\begin{aligned} & \mathrm{V} \mathrm{IN}= \pm 5 \mathrm{~V}, \pm \mathrm{V}_{\mathrm{CC}}= \pm 15 \mathrm{~V} \\ & \mathrm{AV}=5, \text { see figure } 4 \end{aligned}$ | 1 | 03 | 30 |  |  |
|  |  |  |  | 06 | 40 |  |  |
|  |  |  | 2,3 | 03 | 20 |  |  |
|  |  |  |  | 06 | 25 |  |  |
| Settling time | ts(+) <br> and ts(-) | $\pm \mathrm{V}_{\mathrm{CC}}= \pm 15 \mathrm{~V},(0.1 \% \text { error })$ | 9 | 01,04 |  | 4000 | ns |
|  |  | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{AV}=-1$, see figure 5 |  | 02,05 |  | 1500 |  |
|  |  | $\begin{aligned} & \pm \mathrm{V}_{\mathrm{CC}}= \pm 15 \mathrm{~V},(0.1 \% \text { error }) \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{AV}=-5, \end{aligned}$ <br> see figure 5 |  | 03,06 |  | 800 |  |
| Noise (referred to input) broadband | $\mathrm{N}_{l}(\mathrm{BB})$ | $\pm \mathrm{V}_{\mathrm{CC}}= \pm 20 \mathrm{~V}$ <br> bandwidth $=5 \mathrm{kHz}$ | 9 | All |  | 10 | $\mu \mathrm{Vrms}$ |
| Noise (referred to input) popcorn | $\mathrm{N}_{\mathrm{l}}(\mathrm{PC})$ | $\begin{aligned} & \pm \mathrm{V}_{\mathrm{CC}}= \pm 20 \mathrm{~V}, \\ & \text { bandwidth }=5 \mathrm{kHz} \end{aligned}$ | 9 | All |  | 80 | $\mu \mathrm{Vpk}$ |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ Bias currents are actually junction leakage currents which double (approximately) for each $10^{\circ} \mathrm{C}$ increase in junction temperature ( $T_{J}$ ). Measurement of bias current is specified at $T_{J}$ rather than $T_{A}$, since normal warm up thermal transients will affect the bias currents. The measurements for bias currents must be made within 25 ms or 5 loop time constants, whichever is greater after power is first applied to the device for test. Measurement at $T_{A}=-55^{\circ} \mathrm{C}$ is not necessary since expected values are too small for typical test systems.

2/ Bias current is sensitive to power supply voltage, common mode voltage and temperature as shown by the following typical curves:


3/ Negative l|B minimum limits reflect the characteristics of device with bias current compensation.
4/ CMR is calculated from $\mathrm{V}_{\text {IO }}$ measurements at $\mathrm{V}_{\mathrm{CM}}=+15 \mathrm{~V}$ and -15 V .
5/ Continuous limits shall be considerably lower. Protection for shorts to either supply exists providing that $\mathrm{T}_{\mathrm{J}}(\max ) \leq 175^{\circ} \mathrm{C}$.

6/ Because of thermal feedback effects from output to input, open loop gain is not guaranteed to be linear or positive over the operating range. These requirements, if needed, should be specified by the user in additional procurement documents.

TABLE II. Electrical test requirements.

| MIL-PRF-38535 <br> test requirements | Subgroups (see table III) |  |
| :--- | :---: | :---: |
|  | Class S <br> devices | Class B <br> devices |
| Interim electrical parameters | 1 | 1 |
| Final electrical test parameters | $1^{*}, 2,3,4$ | $1^{*}, 2,3,4$ |
| Group A test requirements | $1,2,3,4,5$, <br> $6,7,8,12$ | $1,2,3,4,5$, <br> 6,7 |
| Group B electrical test parameters when <br> using the method 5005 QCI option | $1,2,3$ and <br> table IV delta <br> limits | N/A |
| Group C end-point electrical <br> parameters | $1,2,3$ and <br> table IV delta <br> limits | 1 and table IV <br> delta limits |
| Additional electrical subgroups for <br> Group C periodic inspections | $\mathrm{N} / \mathrm{A}$ | 8,12 |
| Group D end-point electrical <br> parameters | $1,2,3$ | 1 |

*PDA applies to subgroup 1.

## 4. VERIFICATION.

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as function as described herein.
4.2 Screening. Screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:
a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
c. Additional screening for space level product shall be as specified in MIL-PRF-38535.

NOTE: If accelerated high-temperature test conditions are used, the device manufacturer shall ensure that at least 85 percent of the applied voltage is dropped across the device at temperature. The device is not considered functional under accelerated test conditions.
4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.
4.4 Technology Conformance inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).
4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:
a. Tests shall be as specified in table II herein
b. Subgroups 9,10 , and 11 shall be omitted.
c. Subgroup 12 shall be added to group $A$ inspection for class $S$ devices only as shown in table III herein. The sample size series number for subgroup 12 shall be 5 .
4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of MIL-PRF-38535.
4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:
a. End point electrical parameters shall be as specified in table II herein. Delta limits shall apply only to subgroup 1 of group $C$ inspection for class $B$ devices.
b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883
c. Subgroup 3 and 4 shall be added to group $C$ inspection and shall consist of group A, subgroup 8 and 12, as specified in table III herein. The sample size series number for subgroup 3 shall be 10 for class B; the sample size series number for subgroup 4 shall be 5 for class $B$.
4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of MIL-PRF-38535. End point electrical parameters shall be as specified in table II herein.
4.5 Methods of inspection. Methods of inspection shall be specified and as follows.
4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.
4.5.2 Life test cooldown procedure. When devices are measured at $+25^{\circ} \mathrm{C}$ following application of the operating life or burn-in test condition, they shall be cooled to room temperature prior to removal of the bias.


Figure 1. Terminal connections.

CASE H


Figure 1. Terminal connections - Continued.


Figure 2. Offset null circuit.


NOTES:

1. All resistors are $\pm 0.1 \%$ tolerance and all capacitors are $\pm 10 \%$ tolerance unless otherwise specified.
2. Precautions shall be taken to prevent damage to the device under test during insertion into socket and change of state of relays (i.e. disable voltage supplies, current limit $\pm \mathrm{V}_{\mathrm{CC}}$, etc).
3. Compensation capacitors should be added as required for test circuit stability. Two general methods for stability compensation exist. One method is with a capacitor for nulling amp feedback. The other method is with a capacitor in parallel with the $49.9 \mathrm{k} \Omega$ closed loop feedback resistor. Both methods should not be used simultaneously. Proper wiring procedures shall be followed to prevent unwanted coupling and oscillations, etc. Loop response and settling time shall be consistent with the test rate such that any value has settled for at least 5 loop time constants before the value is measured.
4. Adequate settling time should be allowed such that each parameter has settled to within $5 \%$ of its final value.
5. All relays are shown in the normal de-energized state.
6. The nulling amplifier shall be a M38510/10101XXX. Saturation of the nulling amplifier is not allowed on tests where $E$ (pin 5) value is measured.
7. The load resistors $2050 \Omega$ and $11.1 \mathrm{k} \Omega$ yield effective load resistances of $2 \mathrm{k} \Omega$ and $10 \mathrm{k} \Omega$ respectively.
8. Any oscillation greater than 300 mV in amplitude (peak-to-peak) shall be cause for device failure.

FIGURE 3. Test circuit for static tests.


Notes:

1. Resistors are $\pm 1.0 \%$ tolerance and capacitors are $\pm 10 \%$ tolerance.
2. This capacitance includes the actual measured value with stray and wire capacitance.
3. Precaution shall be taken to prevent damage to the device under test during insertion into socket and in applying power.
4. Pulse input and output characteristics are shown on the next page.

FIGURE 4. Test circuit for transient response and slew rate.


| Parameter symbol | Device type | Input pulse signal at $\mathrm{tr} \leq 50 \mathrm{~ns}$ | Output pulse signal | Equation |
| :---: | :---: | :---: | :---: | :---: |
| TR ( $\mathrm{tr}_{\mathrm{r}}$ ) | All | +50 mV | Waveform 1 | TR (tr) $=\Delta \mathrm{t}$ |
| TR ( $\mathrm{os}_{\text {s }}$ ) | All | +50 mV | Waveform 1 | $\begin{gathered} \text { TR (os) = } \\ 100(\Delta \mathrm{VO} / \mathrm{VO}) \% \end{gathered}$ |
| SR (+) | 01,02,04,05 | -5 V to +5 V step | Waveform 2 | $\begin{gathered} \mathrm{SR}(+)= \\ \Delta \mathrm{VO}(+) / \Delta \mathrm{t}(+) \end{gathered}$ |
|  | 03,06 | -1 V to +1 V step | Waveform 2 |  |
| SR (-) | 01,02,04,05 | +5 V to -5 V step | Waveform 3 | $\begin{gathered} \mathrm{SR}(-)= \\ \Delta \mathrm{VO}(-) / \Delta \mathrm{t}(-) \end{gathered}$ |
|  | 03,06 | -1 V to +1 V step | Waveform 3 |  |

FIGURE 4. Test circuit for transient response and slew rate - Continued.


Notes:

1. Resistors are $\pm 1.0 \%$ and capacitors are $\pm 10 \%$ unless otherwise specified.
2. Precaution shall be taken to prevent damage to the device under test during insertion into socket and In applying power.
3. For device types $01,02,04$ and $05, \mathrm{~S} 1$ is open, $\mathrm{AV}=-1$ and $\mathrm{V} \mathbb{I N}=10 \mathrm{~V}$.
4. For device types 03 and $06, \mathrm{~S} 1$ is closed, $\mathrm{AV}=-5$ and $\mathrm{V} \mathrm{IN}=2 \mathrm{~V}$.
5. Settling time, ts, measured on pin 5 , is the interval during which the summing node is not nulled relative to the specified percentage of the final output value. (See table I settling time test conditions).

FIGURE 5. Test circuit for settling time.
TABLE III．Group A inspection for all device types．

| 5 |  | $\vec{E}$＝ | ：${ }^{\text {a }}$ | ¢ | ： | ：$=$ |  | ： | ＂ |  |  |  |  |  | ¢ | を |  |  | － | 》。 | を |  | ＝ | ：$\quad$ ： | ＝$=$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \stackrel{0}{\underline{E}} \\ & \underline{\underline{\Xi}} \\ & \stackrel{\rightharpoonup}{\diamond} \end{aligned}$ | $\stackrel{\times}{\text { x }}$ | $\bigcirc$ | $\sim$ | Oio |  | 응으 | O－M |  | 은 으 | － |  |  |  | $\stackrel{\infty}{\square}$ | is | $\checkmark$ | $\wedge$ | $\wedge$ | $\stackrel{\sim}{\mathrm{N}}$ | ¢－ | 8 | \％ | 88 | 8 is | 옹 |
|  | $\stackrel{\text { c }}{\Sigma}$ | $\bigcirc$ | พ | $\div \stackrel{\circ}{9} \div$ | $\div$ | 운 운 | $\div$ |  | 운 | ก | $\infty$ | ゅ | $\infty$ |  | ¢ |  |  | $\uparrow$ | กู | 운안․ | 안 | $\bigcirc$ | 운운 | 운운 | $\bigcirc \bigcirc$ |
| $\stackrel{\stackrel{\rightharpoonup}{\mathrm{O}}}{\stackrel{\circ}{\mathrm{O}} \stackrel{0}{2}}$ |  | $\begin{aligned} & 0 \\ & 0 \\ & \dot{Z} \\ & \stackrel{\rightharpoonup}{0} \end{aligned}$ |  |  |  | ＝＝ | 㐫 | ＝ | ＝$=$ | $=$ | $=$ | ＝ |  | ＝ |  |  | $\begin{aligned} & \text { me } \\ & \text { yin } \\ & \hline \end{aligned}$ |  | $\begin{aligned} & \mathrm{O} \\ & 0 \\ & 0 \\ & 0 \\ & \dot{O} \end{aligned}$ |  | ¢ | ＝ | ：$=$ | 『 | ＝$=$ |
|  | $\cdots$ |  |  |  |  |  |  |  |  |  |  |  |  | $\mathrm{V}_{10} A D J(-)=\left(E_{3}-E_{18}\right)$ |  | $\begin{aligned} & -\infty \\ & =0 \\ & 0 \\ & 0 \end{aligned}$ |  | $\begin{aligned} & \stackrel{\circ}{\underset{\sim}{w}} \\ & \stackrel{11}{0} \\ & \stackrel{0}{>} ; \end{aligned}$ |  |  |  |  |  |  |  |
|  | $\stackrel{\square}{5}$ |  |  |  |  |  |  | ：$=$ |  |  |  | ＞ | ＞ | $>$ | 若 | 区 |  |  | ：$=$ |  | $>$ | ：$=$ | ：$=$ | ＝＝ | ＝ |
|  | $\begin{aligned} & \frac{0}{\frac{0}{n}} \\ & \frac{1}{>} \end{aligned}$ | ш | บึ พึ |  | 䦽 | யึ ய® |  | 둔 | 号 |  |  | $\stackrel{\circ}{4}$ | 勻 | $\stackrel{\infty}{\text { 山／}}$ | 工 N | $\cdots$ |  | －${ }_{\text {¢ }}$ | ¢ָّ |  | ய̛ |  | 巡 へิ |  | ¢ |
|  | $\stackrel{1}{2}$ |  |  | ＝ | ：$=$ |  |  | ：$=$ |  | － | $\bigcirc$ | $\sim \sim$ | ～ | $\bigcirc$ | $\bigcirc \bigcirc$ | ～ |  | n＝ | ＝ | \％ | $๑$ | ：$=$ | ＝ | ＝＝ | ＝$=$ |
|  |  | \％ |  | $\begin{array}{ll} \infty & 0 \\ \cline { 1 - 1 } & 0 \\ \dot{y} & 2 \end{array}$ |  | 区 | $\stackrel{\otimes}{\grave{\delta}}$ | $\stackrel{\otimes}{\check{\Sigma}}$ | ฐ゙ | $\begin{gathered} \infty \\ \\ \\ 0 \end{gathered}$ |  | $\stackrel{\otimes}{\vdots}$ |  | $\begin{aligned} & \hat{x} \\ & \underset{y}{*} \end{aligned}$ |  | $$ |  |  | ＝＝ |  | $\begin{aligned} & \infty \\ & \underline{y} \\ & \bar{z} \end{aligned}$ |  |  |  |  |
|  | $\checkmark$ | $\underset{\substack{>\\ \\ \hline}}{>}$ | $\geq 0$ | $\begin{array}{ll} > \\ \stackrel{n}{n} & \rightarrow \\ \hline \end{array}$ | $\begin{aligned} & > \\ & 0 \\ & 0 \end{aligned}$ | $\begin{array}{\|ll\|} \hline> & > \\ 0 & \stackrel{n}{1} \\ \hline \end{array}$ | $\bigcirc$ | $\begin{aligned} & \gg \\ & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & \ggg \\ & 0 \\ & 0 \end{aligned}$ | $0$ | $18$ | $0 \frac{\pi}{\frac{\pi}{0}}$ |  | > | $\begin{array}{ll} > & > \\ 0 & 0 \\ 1 & 0 \end{array}$ | $\left.\right\|_{0} ^{2}$ |  | $\underset{\sim}{\infty}$ | $\geq 0$ |  | $\underset{\sim}{\infty}$ | > | $0 \ggg \ggg>1$ | $\begin{aligned} & \ggg \\ & n \rightarrow 0 \end{aligned}$ |  |
|  | の | － |  | ＝ |  | ：$=$ |  |  |  | $\left\lvert\, \begin{gathered} \frac{0}{9} \\ \frac{9}{3} \end{gathered}\right.$ |  |  |  |  | ＝ | ＝ |  | － |  | $\begin{aligned} & \ddot{0} \\ & \stackrel{0}{0} \\ & 0 \end{aligned}$ | $\begin{array}{\|l\|} \hline \stackrel{\circ}{\mathrm{O}} \\ \hline \mathrm{O} \\ \hline \end{array}$ | ＝$=$ | ＝ | ＝＝ | ：$=$ |
|  | $\sim$ | $\gg$ | pos |  |  | $\begin{array}{ll} 2 \\ 2 \\ & 2 \\ \hline 1 \end{array}$ |  |  | $$ |  | $$ | $\stackrel{>}{>}$ |  | >̀ | $\begin{array}{ll} \gg \\ \frac{n}{1} & \stackrel{n}{7} \\ \hline \end{array}$ | $\left\lvert\, \begin{aligned} & > \\ & \\ & \hline \end{aligned}\right.$ |  | $\gg$ | > | $\underset{y}{\geq}$ | $\underset{\sim}{>}$ |  | $$ | M~~ |  |
|  | － | － | $\underset{\sim}{>}$ | $\infty$ | $\begin{array}{ll} > \\ i n & i \end{array}$ |  | is | is is | $\begin{aligned} & \gg \\ & \text { N } \\ & \end{aligned}$ | $3 \frac{\bar{z}}{\overline{0}}$ | $5 \begin{aligned} & 3 \\ & \substack{3 \\ 0 \\ 0} \end{aligned}$ | $\begin{array}{ll} > \\ \stackrel{\rightharpoonup}{\mathrm{N}} & \stackrel{\rightharpoonup}{\mathrm{c}} \end{array}$ |  | > | $$ | $\begin{aligned} & > \\ & \stackrel{n}{n} \\ & \hline \end{aligned}$ |  | ＞ | $\underset{\sim}{>}>$ | $\stackrel{\circ}{2}$ | is | is in | $$ | is $>_{0}$ in | $\begin{array}{ll} \gg \\ \text { N } \\ \text { N m } \end{array}$ |
| $\begin{aligned} & \mathscr{0} \\ & \stackrel{\text { O}}{Z} \end{aligned}$ |  | N： | ： | ＝ | ＊＊ | ：$=$ | $=$ | ：$=$ | $=:$ | ： |  |  | ल |  | บा เा |  |  | NI： | ＝ | ¢ | N | ：$=$ | ＝ | ＊＊＊ | ：$=$ |
|  |  |  | ＋ | $\bigcirc$ |  | $\infty$ | の 응 |  | ₹～ | $\stackrel{\sim}{\sim}$ | $\pm$ | $\stackrel{\square}{\square}$ | $\stackrel{\text { ㅇ }}{ }$ | $\stackrel{\infty}{\sim}$ | $\bigcirc$ | $\bar{\sim}$ |  | ๙ | ～ | \％ | へ | $\sim$ | হ | ¢ | ल |
| 官它灾䯧 |  | $\overline{\bar{\circ}}$ |  | 晾 | ; |  |  | ＝ |  | $=$ |  | ơ |  |  | $\stackrel{\rightharpoonup}{\mathrm{N}}$ | 苟 |  | $\overline{\text { ¢\％}}$－ | $==$ |  | ¢ | ＝$=$ |  | －＝ | ＝ |
| $\begin{aligned} & \hline \bar{\circ} \\ & \underset{\xi}{\circ} \\ & \text { N } \end{aligned}$ |  | $\bigcirc$ |  | $\stackrel{\underline{\square}}{+}$ |  |  | $\underline{\underline{\square}}$ |  |  |  | $0$ |  | $\sum_{0}^{\infty} \frac{0}{>}$ | $0$ |  | － |  | $\stackrel{\square}{ }$ |  | $\stackrel{\circ}{2} \stackrel{ }{4}$ | $\stackrel{\varrho}{\dagger}$ |  |  | $\underline{¢}$ |  |
|  |  | $-\quad \begin{gathered} \text { " } \\ \leftarrow \\ \stackrel{0}{\circ} \\ + \end{gathered}$ |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

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TABLE III. Group A inspection for all device types - Continued.

TABLE III. Group A inspection for all device types - Continued.

TABLE III. Group A inspection for all device types - Continued.


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TABLE III. Group A inspection - Continued.

1/ The equations take into account both the closed loop gain of 1,000 and the scale factor multiplier so that the calculated value is in table I units. The measured value units should, therefore, be used in the equation.
(For example: If $\mathrm{E}_{1}=2 \mathrm{~V}$ and $\mathrm{V}_{\mathrm{IO}}=\mathrm{E}_{1}$, then $\mathrm{V}_{\mathrm{IO}}=2 \mathrm{mV}$ ).
2/ Each device shall be tested over the common mode range as specified in table III. V ${ }_{\mathrm{CM}}$ conditions are achieved by grounding the inputs and algebraically subtracting $\mathrm{V}_{\mathrm{CM}}$ from each supply.
(For example: If $\mathrm{V}_{\mathrm{CM}}=-15 \mathrm{~V}$, then $+\mathrm{V}_{\mathrm{CC}}=+20 \mathrm{~V}-(-15 \mathrm{~V})=+35 \mathrm{~V}$ and $\left.-\mathrm{V}_{\mathrm{CC}}=-20 \mathrm{~V}-(-15 \mathrm{~V})=-5 \mathrm{~V}\right)$.
3/ Common mode rejection is calculated using the offset voltage values measured at the common mode range and end points.
4/ To minimize thermal drift the reference voltage for the gain measurement ( $E_{3}, E_{21}$ and $E_{40}$ ) shall be taken immediately prior to or after the reading corresponding to device gain ( $E_{46}, E_{47}, E_{50}, E_{51}, E_{54}$, and $\left.E_{55}\right)$.

5/ The output shall be shorted to ground for 25 ms or less.
6/ Tests 26 and 48 which require a read and record measurement plus a calculation may be omitted except when subgroups 2 and 3 are being accomplished for group $A$ sampling inspection and groups $C$ and $D$ end point measurements.

7/ Broadband noise $\mathrm{NI}(\mathrm{BB})$ shall be measured using a true RMS voltmeter with a minimum bandwidth of 10 Hz to 20 kHz . "Popcorn" noise $\mathrm{NI}(\mathrm{PC})$ shall be measured for 15 seconds.

8/ Device types $01,02,04$, and 05 are tested with $\mathrm{a}-5 \mathrm{~V}$ to +5 V step input as shown in figure 4 . The circuit gain is $1 \mathrm{~V} / \mathrm{V}$.
9/ Device types 03 and 06 are tested with $\mathrm{a}-1 \mathrm{~V}$ to +1 V step input as shown in figure 4 . The circuit gain is $5 \mathrm{~V} / \mathrm{V}$.

## 5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD personnel, these personnel need to contact the responsible packaging activity to ascertain requisite packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Department of Defense Agency, or within the Military Department's System Command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

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TABLE IV. Group C end point electrical parameters.
( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \pm \mathrm{V}_{\mathrm{CC}}= \pm 20 \mathrm{~V}$ for all device types)

| Table III test no. | Symbol | Device types | Delta limits |  | Limits |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Max | Min | Max |  |
| 3 | VIO | 01, 02, 03 | -1 | +1 | -5 | +5 | mV |
|  |  | 04, 05, 06 | -0.5 | 0.5 | -2 | 2 |  |
| 7 | +IIB | 01, 02, 03 | -50 | +50 | -100 | +100 | pA |
|  |  | 04, 05, 06 | -50 | +50 | -100 | +100 |  |
| 11 | $-_{\text {IB }}$ | 01, 02, 03 | -50 | +50 | -100 | +100 | pA |
|  |  | 04, 05, 06 | -50 | +50 | -100 | +100 |  |

## 6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.
6.2 Acquisition requirements. Acquisition documents should specify the following:
a. Title, number, and date of the specification.
b. Complete part number (see 1.2).
c. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
d. Requirements for certificate of compliance, if applicable.
e. Requirements for notification of change of product or process to acquiring activity in addition to notification of the qualifying activity, if applicable.
f. Requirements for failure analysis (including required test condition of MIL-STD-883, method 5003), corrective action and reporting of results, if applicable.
g. Requirements for product assurance options.
h. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements should not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
i. Requirements for "JAN" marking.
j. Packaging requirements (see 5.1).

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6.3 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.
6.4 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43123-1199.
6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-STD-1331.
6.6 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer length leads and lead forming should not affect the part number.
6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

| Military device type | Generic-industry type |
| :---: | :---: |
| 01 | LF 155 |
| 02 | LF 156 |
| 03 | LF 157 |
| 04 | LF 155A |
| 05 | LF 156A |
| 06 | LF 157A |

6.8 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

| Custodians: | Preparing activity: |
| :--- | :---: |
| Army - CR | DLA - CC |
| Navy - EC |  |
| Air Force -11 | Project $5962-1980$ |
| NASA - NA |  |
| DLA - CC |  |

Review activities:
Army - MI, SM
Navy - AS, CG, MC, SH, TD
Air Force - 03, 19, 99

## STANDARDIZATION DOCUMENT IMPROVEMENT PROPOSAL

## INSTRUCTIONS

1. The preparing activity must complete blocks $1,2,3$, and 8 . In block 1 , both the document number and revision letter should be given.
2. The submitter of this form must complete blocks $4,5,6$, and 7 , and send to preparing activity.
3. The preparing activity must provide a reply within 30 days from receipt of the form.

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