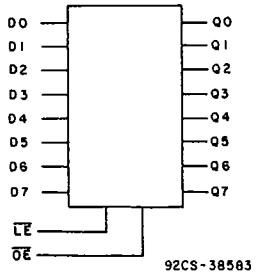
T-46-07-11

CD54/74HC373, CD54/74HCT373
CD54/74HC573, CD54/74HCT573

File Number **1679**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Octal Transparent Latch, 3-State Output

Type Features:

- *Common latch enable control*
- *Common 3-state output enable control*
- *Buffered inputs*
- *3-State outputs*
- *Bus line driving capacity*
- *Typical propagation delay = 12 ns @ V_{CC} = 5V, C_L = 15 pF, T_A = 25° C (Data to Output for HC373)*

The RCA CD54/74HC373/573 and CD54/74HCT373/573 are high speed Octal Transparent Latches manufactured with silicon gate CMOS technology. They possess the low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LSTTL devices. The CD54/74HCT373/573 are functionally as well as pin compatible with the standard 54/74LS373 and 573.

The outputs are transparent to the inputs when the latch enable ($\overline{LE}$) is high. When the latch enable ($\overline{LE}$) goes low the data is latched. The output enable ($\overline{OE}$) controls the 3-state outputs. When the output enable ($\overline{OE}$) is high the outputs are in the high impedance state. The latch operation is independent to the state of the output enable. The 373 and 573 are identical in function and differ only in their pinout arrangements.

The CD54HC/HCT373/573 are supplied in 20 lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT373/573 are supplied in a 20-lead plastic dual-in-line plastic package (E suffix) and in 20-lead surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

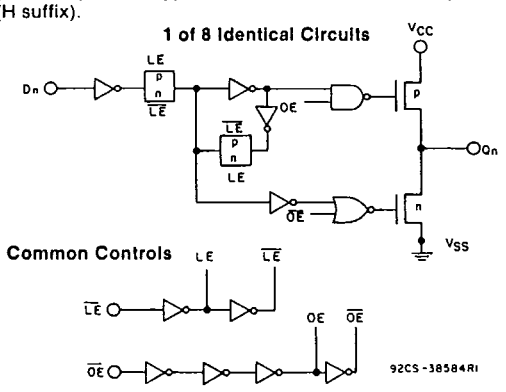


Fig. 1 - Logic diagram.

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

TRUTH TABLE

$\overline{\text{Output}}$ Enable	$\overline{\text{Latch}}$ Enable	Data	Output
L	H	H	H
L	H	L	L
L	L	l	L
L	L	h	H
H	X	X	Z

Note:
L = Low voltage level
H = High voltage level
X = Don't Care
Z = High Impedance State
l = Low voltage level one set-up time prior to the high to low latch enable transition
h = High voltage level one set-up time prior to the high to low latch enable transition

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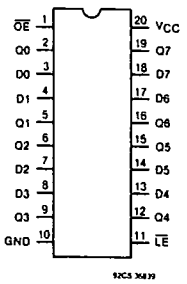
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} +0.5$ V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} +0.5$ V) ..... ±35 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC}): ..... ±70 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

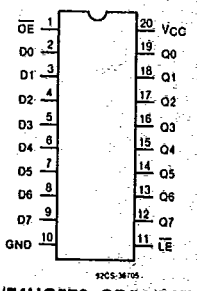
RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.



CD54/74HC373, CD54/74HCT373
TERMINAL ASSIGNMENT



CD54/74HC573, CD54/74HCT573
TERMINAL ASSIGNMENT

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CD54/74HC373, CD54/74HCT373
CD54/74HC573, CD54/74HCT573

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC373/CD54HC373 CD74HC573/CD54HC573										CD74HCT373/CD54HCT373 CD74HCT573/CD54HCT573									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA
3-State Leakage Current	V_{IL} or V_{IH}	$V_O = V_{CC}$ or Gnd	6	—	—	±0.5	—	±5	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5	—	±10	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *	
	HCT373	HCT573
$\overline{OE}$	1.5	1.25
Dn	0.4	0.3
LE	0.6	0.65

* Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 µA max. @ 25°C.

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL VALUES HC	TYPICAL VALUES HCT	UNITS
Propagation Delay					
Data to Qn Output (HC/HCT373)	t_{PLH}	15	12	13	ns
(Fig. 3)	t_{PHL}				
Data to Qn Output (HC/HCT573)	t_{PLH}	15	14	17	ns
(Fig. 3)	t_{PHL}				
$\overline{LE}$ to Qn Output	t_{PLH}	15	14	14	ns
(Fig. 4)	t_{PHL}				
Output Enabling Time	t_{PZL}	15	12	14	ns
(Fig. 6, 7)	t_{PZH}				
Output Disabling Time	t_{PLZ}	15	12	14	ns
(Fig. 6, 7)	t_{PHZ}				
Power Dissipation Capacitance (HC/HCT573, 373)	C_{PD}*	—	51	53	pF

*C_{PD} determines the no-load dynamic power consumption per latch. It is obtained by the following relationship;
P_D (total power per latch) = V_{CC}^2 f_i (C_{PD} + C_L) where f_i = input frequency,
C_L = output load capacitance, V_{CC} = supply voltage

PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		TEST CONDITIONS V_{CC} V	LIMITS 25°C HC Min.	HC Max.	HCT Min.	HCT Max.	-40°C to +85°C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
$\overline{LE}$ Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	
(Fig. 3)		4.5	16	—	16	—	20	—	20	—	24	—	24	—	ns
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Set-up Time	t_{SU}	2	50	—	—	—	65	—	—	—	75	—	—	—	
Data to $\overline{LE}$	573	4.5	10	—	13	—	13	—	16	—	15	—	20	—	ns
(Fig. 4)		6	9	—	—	—	11	—	—	—	13	—	—	—	
Set-up Time	t_{SU}	2	50	—	—	—	65	—	—	—	75	—	—	—	
Data to $\overline{LE}$	373	4.5	10	—	13	—	13	—	16	—	15	—	20	—	ns
(Fig. 4)		6	9	—	—	—	11	—	—	—	13	—	—	—	
Hold Time	t_H	2	40	—	—	—	50	—	—	—	60	—	—	—	
Data to $\overline{LE}$	573	4.5	8	—	10	—	10	—	13	—	12	—	15	—	ns
(Fig. 4)		6	7	—	—	—	9	—	—	—	10	—	—	—	
Hold Time	t_H	2	5	—	—	—	5	—	—	—	5	—	—	—	
Data to $\overline{LE}$	373	4.5	5	—	10	—	5	—	13	—	5	—	15	—	ns
(Fig. 4)		6	5	—	—	—	5	—	—	—	5	—	—	—	

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CD54/74HC373, CD54/74HCT373
CD54/74HC573, CD54/74HCT573

SWITCHING CHARACTERISTICS (Input t_r, t_f = 6 ns, C_L = 50 pF)

CHARACTERISTIC		TEST CONDITIONS V_{CC} V	LIMITS												UNITS
			25°C				-40°C to +85°C				-55°C to +125°C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
Data to Qn	t_{PHL}	4.5	—	30	—	32	—	38	—	40	—	45	—	48	ns
(Fig. 2) HC/HCT373		6	—	26	—	—	—	33	—	—	—	38	—	—	
Data to Qn	t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	
(Fig. 2)	t_{PHL}	4.5	—	35	—	35	—	44	—	44	—	53	—	53	ns
HC/HCT573		6	—	30	—	—	—	37	—	—	—	45	—	—	
$\overline{LE}$ to Qn	t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	
	t_{PHL}	4.5	—	35	—	35	—	44	—	44	—	53	—	53	ns
(Fig. 3)		6	—	30	—	—	—	37	—	—	—	45	—	—	
Output Enabling	t_{PZL}	2	—	150	—	—	—	190	—	—	—	225	—	—	
Time	t_{PZH}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	ns
(Figs. 5 & 6)		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Disabling	t_{PLZ}	2	—	150	—	—	—	190	—	—	—	225	—	—	
Time	t_{PHZ}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	ns
(Figs. 5 & 6)		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition	t_{TLH}	2	—	60	—	—	—	75	—	—	—	90	—	—	
Time	t_{THL}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	ns
(Fig. 2)		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	20	—	20	—	20	—	20	—	20	—	20	pF

CD54/74HC373, CD54/74HCT373
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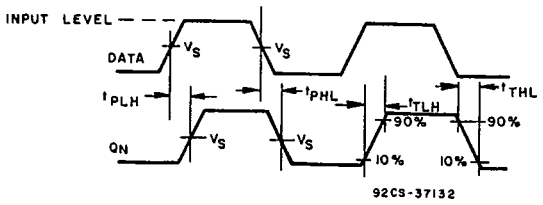
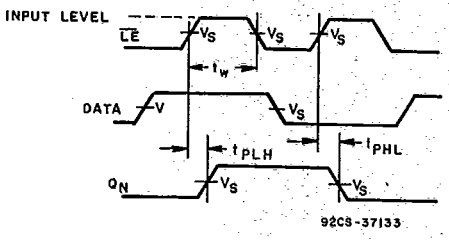


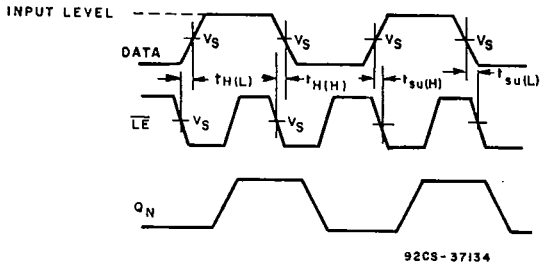
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

Fig. 2 - Data to Q_n output propagation delays and output transition times.



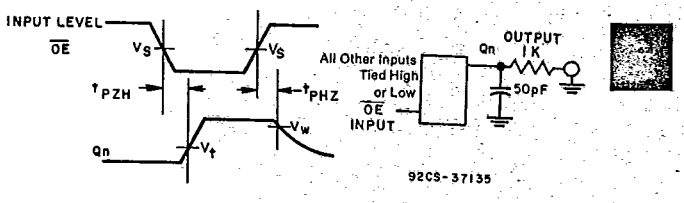
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

Fig. 3 - Latch enable propagation delays.



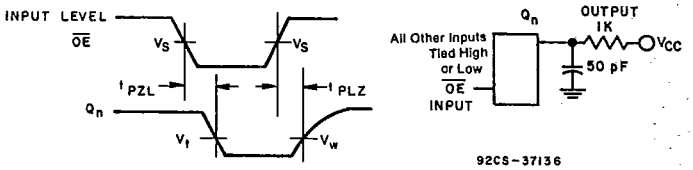
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

Fig. 4 - Latch enable prerequisite times.



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V
V_t	50% V_{CC}	1.3 V
V_w	90% V_{CC}	90% V_{CC}

Fig. 5 - Three-state propagation delays.



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V
V_t	50% V_{CC}	1.3 V
V_w	10% V_{CC}	10% V_{CC}

Fig. 6 - Three-state propagation delays.