



Integrated Device Technology, Inc.

FAST CMOS 16-BIT TRANSPARENT LATCHES

IDT54/74FCT16373T/AT/CT/ET
IDT54/74FCT162373T/AT/CT/ET

FEATURES:

- **Common features:**
 - 0.5 MICRON CMOS Technology
 - **High-speed, low-power CMOS replacement for ABT functions**
 - **Typical tsk(o) (Output Skew) < 250ps**
 - **Low input and output leakage $\leq 1\mu A$ (max.)**
 - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
 - Packages include 25 mil pitch SSOP, 19.6 mil pitch TSSOP, 15.7 mil pitch TVSOP and 25 mil pitch Cerpack
 - Extended commercial range of -40°C to +85°C
 - Vcc = 5V $\pm 10\%$
- **Features for FCT16373T/AT/CT/ET:**
 - High drive outputs (-32mA IOH, 64mA IOL)
 - Power off disable outputs permit "live insertion"
 - Typical VOLP (Output Ground Bounce) < 1.0V at Vcc = 5V, TA = 25°C
- **Features for FCT162373T/AT/CT/ET:**
 - Balanced Output Drivers: $\pm 24mA$ (commercial), $\pm 16mA$ (military)
 - Reduced system switching noise
 - Typical VOLP (Output Ground Bounce) < 0.6V at Vcc = 5V, TA = 25°C

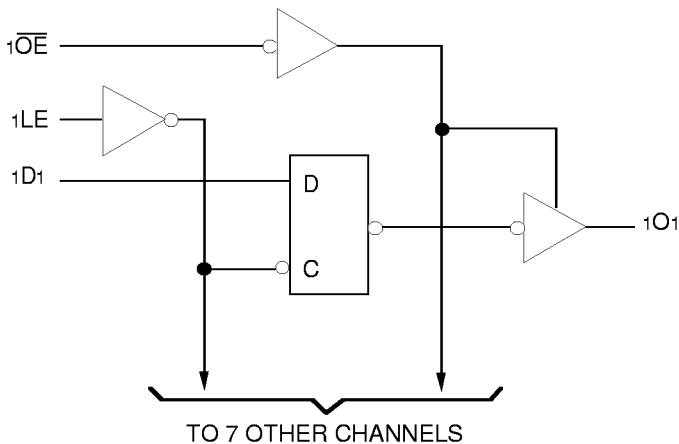
DESCRIPTION:

The FCT16373T/AT/CT/ET and FCT162373T/AT/CT/ET 16-bit transparent D-type latches are built using advanced dual metal CMOS technology. These high-speed, low-power latches are ideal for temporary storage of data. They can be used for implementing memory address latches, I/O ports, and bus drivers. The Output Enable and Latch Enable controls are organized to operate each device as two 8-bit latches, or one 16-bit latch. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

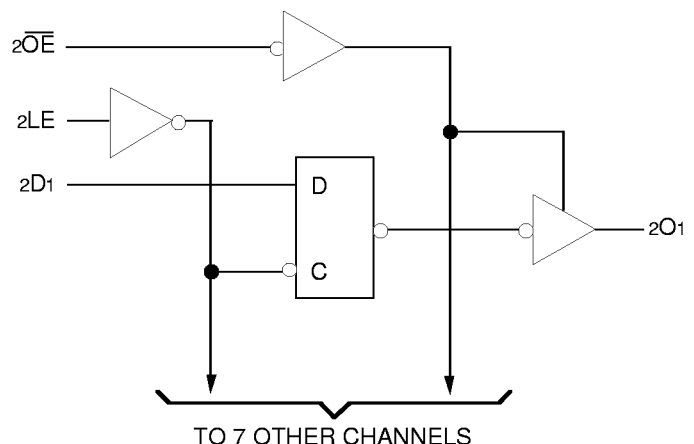
The FCT16373T/AT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

The FCT162373T/AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times—reducing the need for external series terminating resistors. The FCT162373T/AT/CT/ET are plug-in replacements for the FCT16373T/AT/CT/ET and ABT16373 for on-board interface applications.

FUNCTIONAL BLOCK DIAGRAM



2543 drw 01



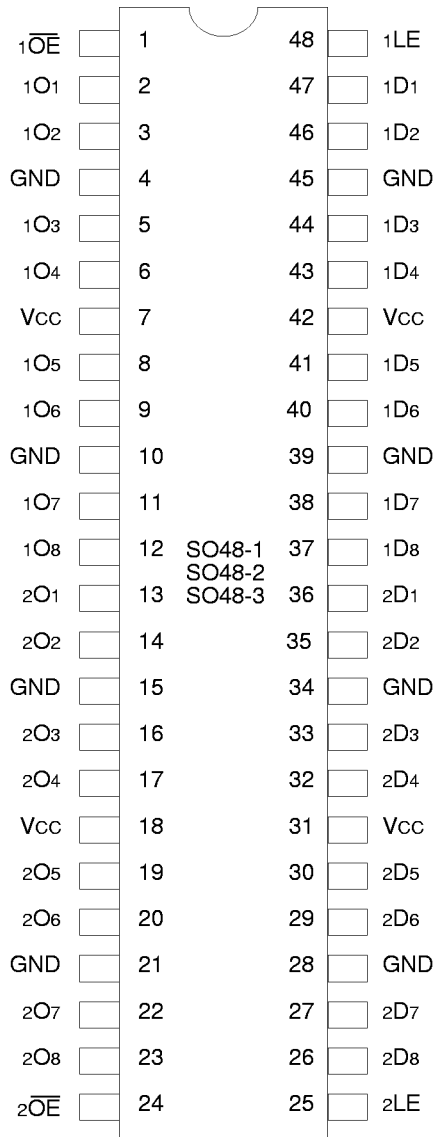
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MILITARY AND INDUSTRIAL TEMPERATURE RANGES

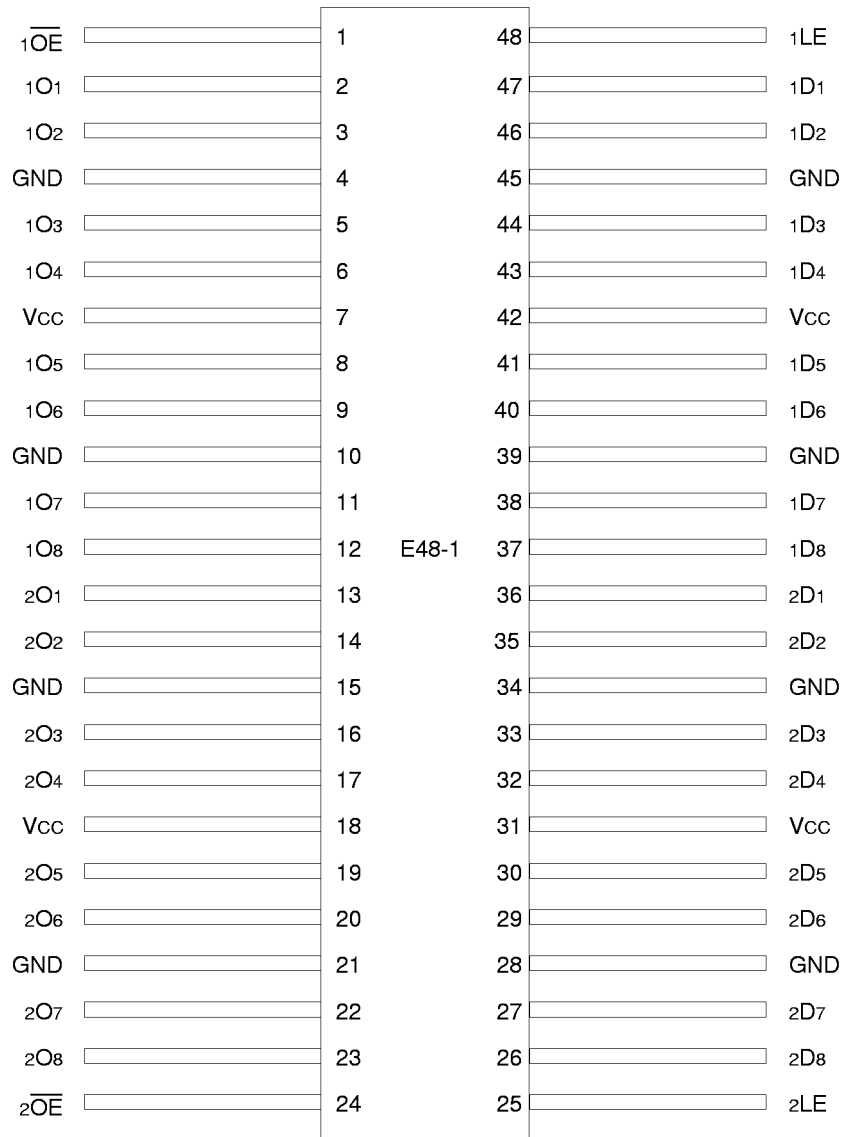
FEBRUARY 1997

PIN CONFIGURATIONS



**SSOP/
 TSSOP/TVSOP
 TOP VIEW**

2543 drw 03



**CERPACK
 TOP VIEW**

2543 drw 04

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs
xLE	Latch Enable Input (Active HIGH)
\overline{xOE}	Output Enable Input (Active LOW)
xOx	3-State Outputs

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FUNCTION TABLE⁽¹⁾

Inputs			Outputs
xDx	xLE	\overline{xOE}	xOx
H	H	L	H
L	H	L	L
X	X	H	Z

2543 tbl 02

NOTE:

- H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High-impedance

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to VCC +0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +120	mA

2543 lmk 03

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXXT Output and I/O terminals.
- Output and I/O terminals for FCT162XXXT.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	3.5	6.0	pF
COU	Output Capacitance	VOUT = 0V	3.5	8.0	pF

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NOTE:

- This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = -40°C to +85°C, VCC = 5.0V ± 10%; Military: TA = -55°C to +125°C, VCC = 5.0V ± 10%

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I _{IH}	Input HIGH Current (Input pins) ⁽⁵⁾	V _{CC} = Max.	V _I = V _{CC}	—	—	±1	μA
	Input HIGH Current (I/O pins) ⁽⁵⁾			—	—	±1	
I _{IL}	Input LOW Current (Input pins) ⁽⁵⁾		V _I = GND	—	—	±1	
	Input LOW Current (I/O pins) ⁽⁵⁾			—	—	±1	
I _{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁵⁾	V _{CC} = Max.	V _O = 2.7V	—	—	±1	μA
			V _O = 0.5V	—	—	±1	
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA		—	-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max., V _O = GND ⁽³⁾		-80	-140	-250	mA
V _H	Input Hysteresis	—		—	100	—	mV
ICCL ICCH IC CZ	Quiescent Power Supply Current	V _{CC} = Max., V _{IN} = GND or V _{CC}		—	5	500	μA

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OUTPUT DRIVE CHARACTERISTICS FOR FCT16373T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _O	Output Drive Current	V _{CC} = Max., V _O = 2.5V ⁽³⁾		-50	—	-180	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3mA	2.5	3.5	—	V
			I _{OH} = -12mA MIL. I _{OH} = -15mA COM'L.	2.4	3.5	—	V
			I _{OH} = -24mA MIL. I _{OH} = -32mA COM'L. ⁽⁴⁾	2.0	3.0	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 48mA MIL. I _{OL} = 64mA COM'L.	—	0.2	0.55	V
I _{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	V _{CC} = 0V, V _{IN} or V _O ≤ 4.5V		—	—	±1	μA

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OUTPUT DRIVE CHARACTERISTICS FOR FCT162373T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _{ODL}	Output LOW Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		60	115	200	mA
I _{ODH}	Output HIGH Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		-60	-115	-200	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -16mA MIL. I _{OH} = -24mA COM'L.	2.4	3.3	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 16mA MIL. I _{OL} = 24mA COM'L.	—	0.3	0.55	V

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NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- The test limit for this parameter is ± 5μA at TA = -55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{xOE} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	60	100	$\mu\text{A}/$ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{xOE} = \text{GND}$ $xLE = V_{CC}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.6	1.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	0.9	2.3	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{xOE} = \text{GND}$ $xLE = V_{CC}$ Sixteen Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	2.4	4.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	6.4	16.5 ⁽⁵⁾	

NOTES:

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- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} \text{DHNT} + I_{CCD} (f_{CP}N_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current } (I_{CCL}, I_{CCH} \text{ and } I_{CCZ})$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$
 $\text{DH} = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at DH}$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT16373T/162373T				FCT16373AT/162373AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay xDx to xOx	CL = 50pF RL = 500Ω	1.5	8.0	1.5	8.5	1.5	5.2	1.5	5.6	ns
tPLH tPHL	Propagation Delay xLE to xOx		2.0	13.0	2.0	15.0	2.0	8.5	2.0	9.8	ns
tPZH tPZL	Output Enable Time		1.5	12.0	1.5	13.5	1.5	6.5	1.5	7.5	ns
tPHZ tPLZ	Output Disable Time		1.5	7.5	1.5	10.0	1.5	5.5	1.5	6.5	ns
tSU	Set-up Time HIGH or LOW, xDx to xLE		2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW, xDx to xLE		1.5	—	1.5	—	1.5	—	1.5	—	ns
tw	xLE Pulse Width HIGH		6.0	—	6.0	—	5.0	—	6.0	—	ns
tSK(o)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	0.5	ns

Symbol	Parameter	Condition ⁽¹⁾	FCT16373CT/162373CT				FCT16373ET/162373ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay xDx to xOx	CL = 50pF RL = 500Ω	1.5	4.2	1.5	5.1	1.5	3.4	—	—	ns
tPLH tPHL	Propagation Delay xLE to xOx		2.0	5.5	2.0	8.0	1.5	3.7	—	—	ns
tPZH tPZL	Output Enable Time		1.5	5.5	1.5	6.3	1.5	4.4	—	—	ns
tPHZ tPLZ	Output Disable Time		1.5	5.0	1.5	5.9	1.5	3.6	—	—	ns
tSU	Set-up Time HIGH or LOW, xDx to xLE		2.0	—	2.0	—	1.0	—	—	—	ns
tH	Hold Time HIGH or LOW, xDx to xLE		1.5	—	1.5	—	1.0	—	—	—	ns
tw	xLE Pulse Width HIGH		5.0	—	6.0	—	3.0 ⁽⁴⁾	—	—	—	ns
tSK(o)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	—	ns

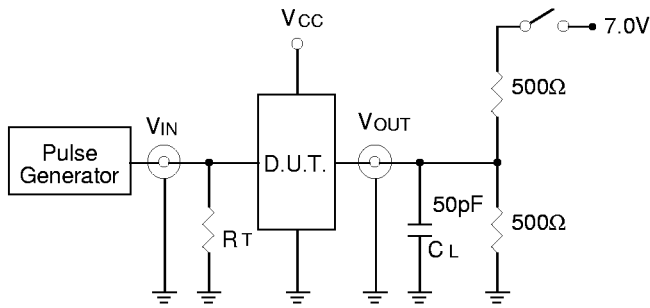
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.

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TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

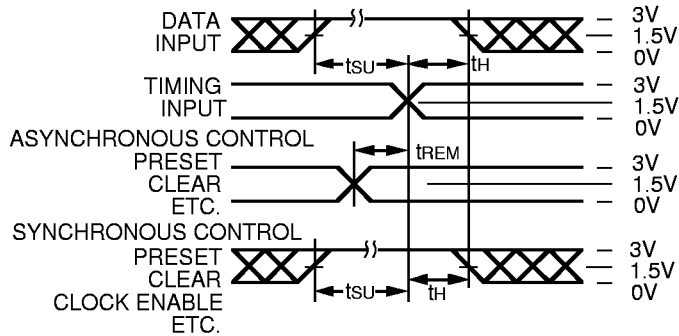
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DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

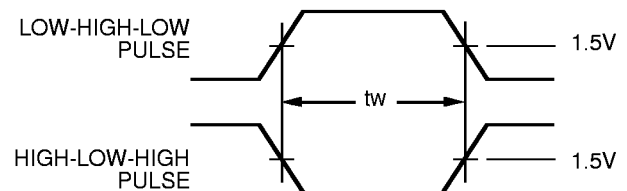
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



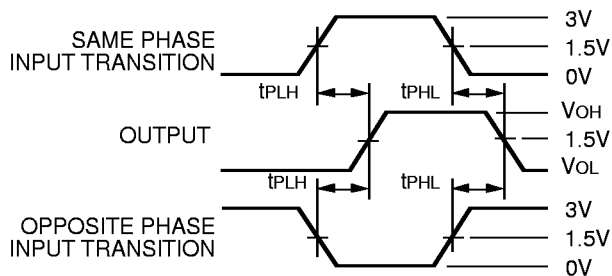
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PULSE WIDTH



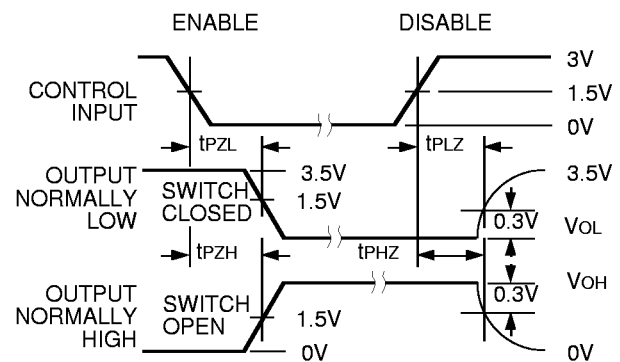
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PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

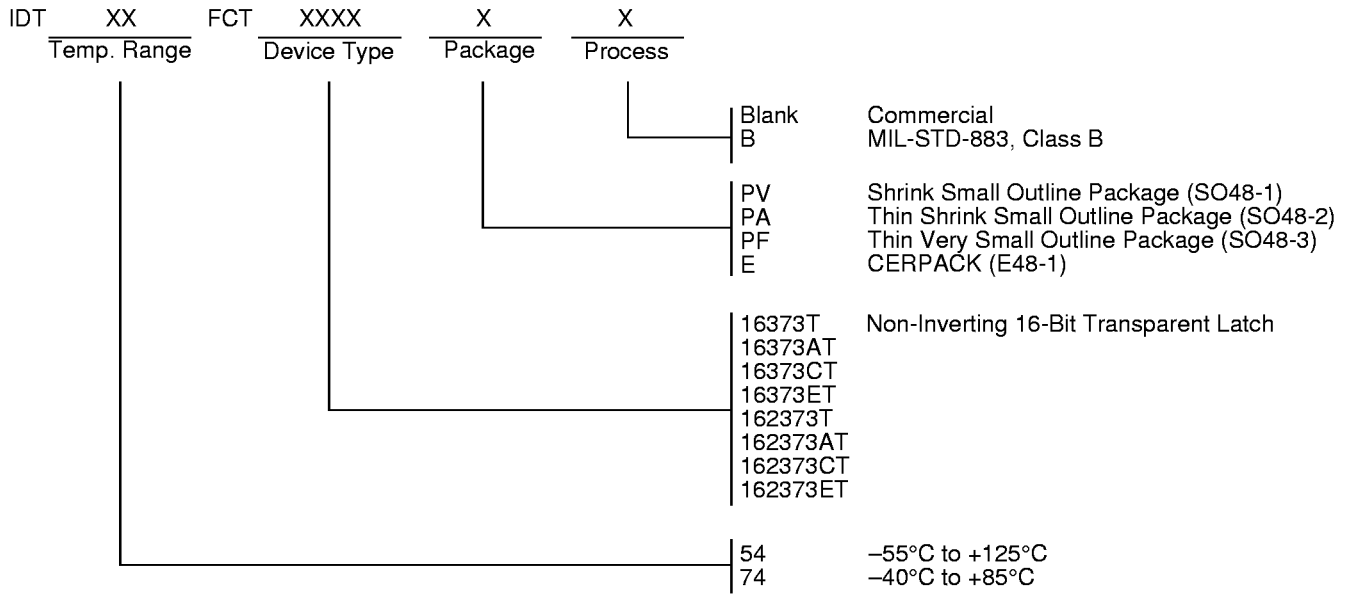


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NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate \leq 1.0MHz; $t_r \leq$ 2.5ns; $t_f \leq$ 2.5ns

ORDERING INFORMATION



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