

# DATA SHEET



## **PCK2057**

70 – 190 MHz I<sup>2</sup>C differential  
1:10 clock driver

Product data  
Supersedes data of 2001 May 09  
File under Integrated Circuits, ICL03

2001 Jun 12

70 – 190 MHz I<sup>2</sup>C differential 1:10 clock driver

## PCK2057

## FEATURES

- Optimized for clock distribution in DDR (Double Data Rate) SDRAM applications supporting DDR 200/266/300/333
- Full DDR solution provided when used with PCK2002P or PCK2002PL, and PCK2022RA
- 1-to-10 differential clock distribution
- Very low jitter (< 100 ps)
- Operation from 2.2 V to 2.7 V AV<sub>DD</sub> and 2.3 V to 2.7 V V<sub>DD</sub>
- SSTL\_2 interface clock inputs and outputs
- HCSL to SSTL\_2 input conversion
- Test mode enables buffers while disabling PLL
- Tolerant of Spread Spectrum input clock
- 3.3 V I<sup>2</sup>C support with 3.3 V V<sub>DD</sub>I<sup>2</sup>C
- 2.5 V I<sup>2</sup>C support with 2.5 V V<sub>DD</sub>I<sup>2</sup>C
- Form, fit, and function compatible with CDCV850

## DESCRIPTION

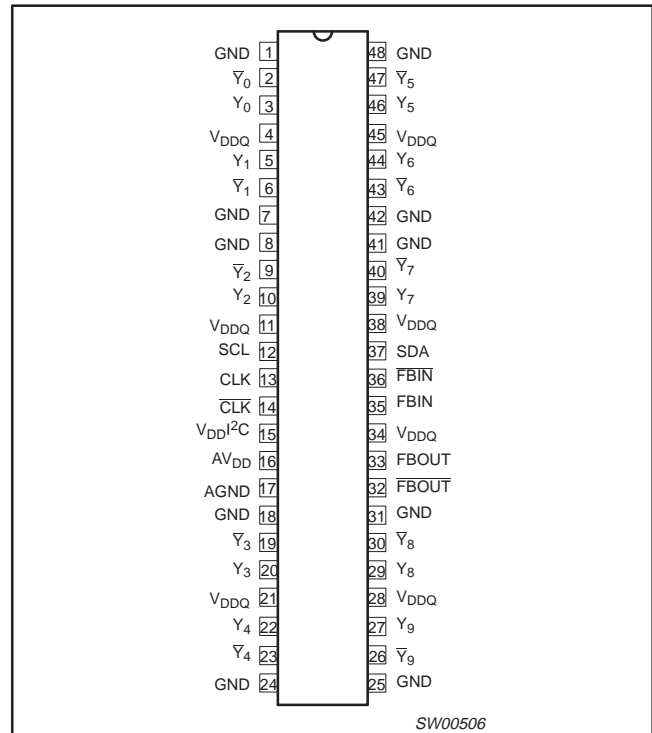
The PCK2057 is a high-performance, low-skew, low-jitter zero delay buffer that distributes a differential clock input pair (CLK,  $\overline{\text{CLK}}$ ) to ten differential pairs of clock outputs and one differential pair of feedback clock outputs. The clock outputs are controlled by the clock inputs (CLK,  $\overline{\text{CLK}}$ ), the feedback clocks (FBIN,  $\overline{\text{FBIN}}$ ), the 2-line serial interface (SDA, SCL), and the analog power input (AV<sub>DD</sub>). The two-line serial interface (I<sup>2</sup>C) can put the individual output clock pairs in a high-impedance state. When AV<sub>DD</sub> is tied to GND, the PLL is turned off and bypassed for test purposes.

The device provides a standard mode (100 kbits) I<sup>2</sup>C interface for device control. The implementation is as a slave/receiver. The serial inputs (SDA, SCL) provide integrated pull-up resistors (typically 100 k $\Omega$ ).

Two 8-bit, 2-line serial registers provide individual enable control for each output pair. All outputs default to enabled at power-up. Each output pair can be placed in a high-impedance mode, when a low-level control bit is written to the control register. The registers must be accessed in sequential order (i.e., random access of the registers is not supported). The I<sup>2</sup>C interface circuit can be supplied with either 2.5 V or 3.3 V (V<sub>DD</sub>I<sup>2</sup>C).

Since the PCK2057 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power-up.

## PIN CONFIGURATION



## PIN DESCRIPTION

| PINS  | SYMBOL   | DESCRIPTION  |
|---|--|--|
| 1, 7, 8, 18, 24, 25, 31, 41, 42, 48   | GND  | Ground   |
| 2, 3, 5, 6, 9, 10, 19, 20, 22, 23, 26, 27, 29, 30, 32, 33, 39, 40, 43, 44, 46, 47 | Y <sub>n</sub> , $\overline{\text{Y}}_n$ ,<br>FBOU, $\overline{\text{FBOU}}$ | Buffered output copies of input clock, CLK                       |
| 4, 11, 21, 28, 34, 38, 45   | V <sub>DDQ</sub>   | 2.5 V supply   |
| 13, 14, 35, 36  | CLK, $\overline{\text{CLK}}$ ,<br>FBIN, $\overline{\text{FBIN}}$             | Differential clock inputs and feedback differential clock inputs |
| 16  | AV <sub>DD</sub>   | Analog power   |
| 17  | AGND   | Analog ground  |
| 37  | SDA  | Serial data  |
| 12  | SCL  | Serial clock   |
| 15  | V <sub>DD</sub> I <sup>2</sup> C   | I <sup>2</sup> C power   |

## ORDERING INFORMATION

| PACKAGES             | TEMPERATURE RANGE | ORDER CODE | DRAWING NUMBER |
|----------------------|-------------------|------------|----------------|
| 48-Pin Plastic TSSOP | 0 to +70 °C       | PCK2057DGG | SOT362-1       |

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## FUNCTION TABLE

| INPUTS           |     |     | OUTPUTS <sup>1</sup> |   |       |       | PLL ON/OFF   |
|------------------|-----|-----|----------------------|---|-------|-------|--------------|
| AV <sub>DD</sub> | CLK | CLK | Y                    | Ȳ | FBOUȲ | FBOUȲ |              |
| GND              | L   | H   | L                    | H | L     | H     | Bypassed/OFF |
| GND              | H   | L   | H                    | L | H     | L     | Bypassed/OFF |
| 2.5 V (nom.)     | L   | H   | L                    | H | L     | H     | ON           |
| 2.5 V (nom.)     | H   | L   | H                    | L | H     | L     | ON           |

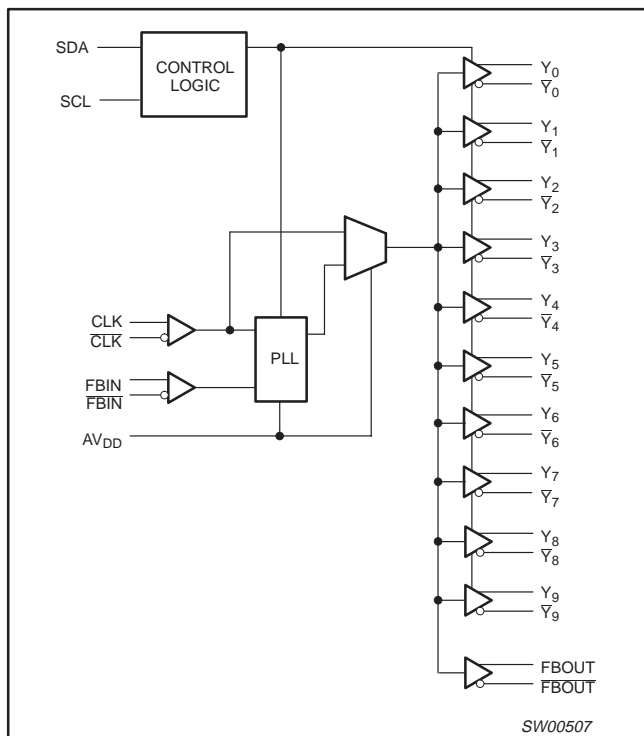
### NOTES:

H = HIGH voltage level

L = LOW voltage level

1. Each output pair (except FBOUȲ and FBOUȲ) can be put into a high-impedance state through the 2-line serial interface.

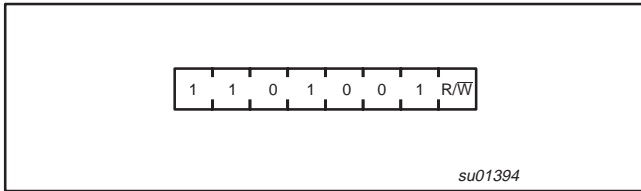
## BLOCK DIAGRAM



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## I<sup>2</sup>C ADDRESS



## I<sup>2</sup>C CONSIDERATIONS

I<sup>2</sup>C has been chosen as the serial bus interface to control the PCK2057. I<sup>2</sup>C was chosen to support the JEDEC proposal JC-42.5 168 Pin Unbuffered SDRAM DIMM. All vendors are required to determine the legal issues associated with the manufacture of I<sup>2</sup>C devices.

1) Address assignment: The clock driver in this specification uses the single, 7-bit address shown below. All devices can use the address if only one master clock driver is used in a design. The address can be re-used for the CKBF device if no other conflicting I<sup>2</sup>C clock driver is used in the system.

The following address was confirmed by Philips on 09/04/96.

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
|----|----|----|----|----|----|----|-----|
| 1  | 1  | 0  | 1  | 0  | 0  | 1  | 0   |

**NOTE:** The R/W bit is used by the I<sup>2</sup>C controller as a data direction bit. A 'zero' indicates a transmission (WRITE) to the clock device. A 'one' indicates a request for data (READ) from the clock driver. Since the definition of the clock buffer only allows the controller to WRITE data; the R/W bit of the address will always be seen as 'zero'. Optimal address decoding of this bit is left to the vendor.

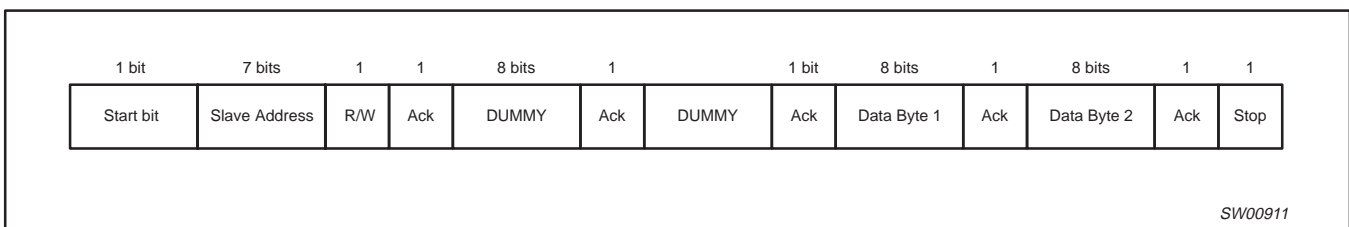
2) Data Transfer Rate: 100 kbits/s (standard mode) is the base functionality required. Fast mode (400 kbits/s) functionality is optional.

3) Logic Levels: I<sup>2</sup>C logic levels are based on a percentage of V<sub>DD</sub> for the controller and other devices on the bus. Assume all devices are based on a 3.3 Volt supply.

4) Data Byte Format: Byte format is 8 Bits as described in the following appendices.

5) Data Protocol: To simplify the clock I<sup>2</sup>C interface, the clock driver serial protocol was specified to use only block writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. Indexed bytes are not allowed. However, the SMBus controller has a more specific format than the generic I<sup>2</sup>C protocol.

The clock driver must meet this protocol which is more rigorous than previously stated I<sup>2</sup>C protocol. Treat the description from the viewpoint of controller. The controller "writes" to the clock driver.



**NOTE:** The acknowledgement bit is returned by the slave/receiver (the clock driver).

6) Electrical Characteristics: All electrical characteristics must meet the standard mode specifications found in section 15 of the I<sup>2</sup>C specification.

a) Pull-Up Resistors: Any internal resistors pull-ups on the SDATA and SCLOCK inputs must be stated in the individual datasheet. The use of internal pull-ups on these pins of below 100 kΩ is discouraged. Assume that the board designer will use a single external pull-up resistor for each line and that these values are in the 5–6 kΩ range. Assume one I<sup>2</sup>C device per DIMM (serial presence detect), one I<sup>2</sup>C controller, one clock driver plus one/two more I<sup>2</sup>C devices on the platform for capacitive loading purposes.

(b) Input Glitch Filters: Only fast mode I<sup>2</sup>C devices require input glitch filters to suppress bus noise. The clock driver is specified as a standard mode device and is not required to support this feature.

For specific I<sup>2</sup>C information, consult the Philips I<sup>2</sup>C Peripherals Data Handbook IC12 (1997).

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**SERIAL CONFIGURATION MAP**

The serial bits will be read by the clock buffer in the following order:

Byte 0 – Bits 7, 6, 5, 4, 3, 2, 1, 0

Byte 1 – Bits 7, 6, 5, 4, 3, 2, 1, 0

All unused register bits (Reserved and “—”) should be designed as “Don’t Care”. It is expected that the controller will force all of these bits to a “0” level.

All register bits labeled “Initialize to 0” must be written to zero during initialization. Failure to do so may result in a higher than normal operating current.

**Byte 0: Active/inactive register**

1 = enable; 0 = disable

| BIT | PIN#   | NAME                            | INITIAL VALUE | DESCRIPTION            |
|-----|--------|---------------------------------|---------------|------------------------|
| 7   | 2, 3   | $\overline{\text{CLK0}}$ , CLK0 | 1             | Enable/Disable Outputs |
| 6   | 5, 6   | $\overline{\text{CLK1}}$ , CLK1 | 1             | Enable/Disable Outputs |
| 5   | 9, 10  | $\overline{\text{CLK2}}$ , CLK2 | 1             | Enable/Disable Outputs |
| 4   | 19, 20 | $\overline{\text{CLK3}}$ , CLK3 | 1             | Enable/Disable Outputs |
| 3   | 22, 23 | $\overline{\text{CLK4}}$ , CLK4 | 1             | Enable/Disable Outputs |
| 2   | 47, 46 | $\overline{\text{CLK5}}$ , CLK5 | 1             | Enable/Disable Outputs |
| 1   | 44, 43 | $\overline{\text{CLK6}}$ , CLK6 | 1             | Enable/Disable Outputs |
| 0   | 40, 39 | $\overline{\text{CLK7}}$ , CLK7 | 1             | Enable/Disable Outputs |

**NOTE:**

- Inactive means outputs are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.

**Byte 1: Active/inactive register**

1 = enable; 0 = disable

| BIT | PIN#   | NAME                            | INITIAL VALUE | DESCRIPTION                    |
|-----|--------|---------------------------------|---------------|--------------------------------|
| 7   | 30, 29 | $\overline{\text{CLK8}}$ , CLK8 | 1             | Enable/Disable Outputs         |
| 6   | 27, 26 | $\overline{\text{CLK9}}$ , CLK9 | 1             | Enable/Disable Outputs         |
| 5   | —      | —                               | 0             | Reserved                       |
| 4   | —      | —                               | 0             | Reserved                       |
| 3   | —      | —                               | 0             | Reserved                       |
| 2   | —      | —                               | 0             | Reserved                       |
| 1   | —      | —                               | 0             | Power-Down Mode Disable/Enable |
| 0   | —      | —                               | 0             | HCSL Enable/Disable            |

**NOTE:**

- Inactive means outputs are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.

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**ABSOLUTE MAXIMUM RATINGS (see Note 1)**

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| SYMBOL                             | PARAMETER                                     |                    | TEST CONDITIONS   | LIMITS |  | UNIT |
|------------------------------------|---|--------------------|---|--------|--|------|
|                                    |   |                    |   | MIN    | MAX                                    |      |
| V <sub>DDQ</sub> /AV <sub>DD</sub> | Supply voltage range                          |                    |   | 0.5    | 3.6                                    | V    |
| V <sub>DD</sub> I <sup>2</sup> C   | I <sup>2</sup> C supply voltage range         |                    |   | 0.5    | 4.6                                    | V    |
| V <sub>I</sub>                     | Input voltage range                           | except SCL and SDA | see Notes 2 and 3                                       | -0.5   | V <sub>DDQ</sub> + 0.5                 | V    |
|                                    |   | SCL and SDA        | see Notes 2 and 3                                       | -0.5   | V <sub>DD</sub> I <sup>2</sup> C + 0.5 | V    |
| V <sub>O</sub>                     | Output voltage range                          |                    | see Notes 2 and 3                                       | -0.5   | V <sub>DDQ</sub> + 0.5                 | V    |
| I <sub>IK</sub>                    | Input clamp current                           |                    | V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>DDQ</sub> | —      | ±50                                    | mA   |
| I <sub>OK</sub>                    | Output clamp current                          |                    | V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>DDQ</sub> | —      | ±50                                    | mA   |
| I <sub>O</sub>                     | Continuous output current                     |                    | V <sub>O</sub> = 0 to V <sub>DDQ</sub>                  | —      | ±50                                    | mA   |
|                                    | Continuous current to GND or V <sub>DDQ</sub> |                    |   | —      | ±100                                   | mA   |
| T <sub>stg</sub>                   | Storage temperature range                     |                    |   | -65    | +150                                   | °C   |

**NOTES:**

- Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- This value is limited to 3.6 V maximum.

**RECOMMENDED OPERATING CONDITIONS (see Note 1)**

| SYMBOL           | PARAMETER                             |   | TEST CONDITIONS | LIMITS                                      |      |   | UNIT |
|------------------|---------------------------------------|---|-----------------|---|------|---|------|
|                  |                                       |   |                 | MIN   | TYP  | MAX   |      |
|                  | Supply voltage                        | V <sub>DDQ</sub>                                |                 | 2.3   | —    | 2.7   | V    |
|                  |                                       | AV <sub>DD</sub>                                |                 | 2.2   | —    | 2.7   | V    |
|                  |                                       | V <sub>DD</sub> I <sup>2</sup> C                | see Note 2      | 2.3   | —    | 3.6   | V    |
| V <sub>IL</sub>  | LOW-level input voltage               | CLK, $\overline{\text{CLK}}$ , HCSL buffer only |                 | —   | 0    | 0.24  | V    |
|                  |                                       | CLK, $\overline{\text{CLK}}$                    |                 | -0.3  | —    | V <sub>DDQ</sub> - 0.4                      | V    |
|                  |                                       | FBIN, $\overline{\text{FBIN}}$                  |                 | —   | —    | V <sub>DDQ</sub> /2 - 0.18                  | V    |
|                  |                                       | SDA, SCL  |                 | —   | —    | 0.3 × V <sub>DD</sub> I <sup>2</sup> C      | V    |
| V <sub>IH</sub>  | HIGH-level input voltage              | CLK, $\overline{\text{CLK}}$ , HCSL buffer only |                 | 0.66  | 0.71 | —   | V    |
|                  |                                       | CLK, $\overline{\text{CLK}}$                    |                 | 0.4   | —    | V <sub>DDQ</sub> + 0.3                      | V    |
|                  |                                       | FBIN, $\overline{\text{FBIN}}$                  |                 | V <sub>DDQ</sub> /2 + 0.18                  | —    | —   | V    |
|                  |                                       | SDA, SCL  |                 | 0.7 × V <sub>DD</sub> I <sup>2</sup> C      | —    | —   | V    |
|                  | DC input signal voltage               |   | see Note 3      | -0.3  | —    | V <sub>DDQ</sub> + 0.3                      | V    |
| V <sub>ID</sub>  | Differential input signal voltage     | DC: CLK, FBIN                                   | see Note 4      | 0.36  | —    | V <sub>DDQ</sub> + 0.6                      | V    |
|                  |                                       | AC: CLK, FBIN                                   | see Note 4      | 0.2   | —    | V <sub>DDQ</sub> + 0.6                      | V    |
| V <sub>IX</sub>  | Input differential pair cross-voltage |   | see Note 5      | 0.45 × (V <sub>IH</sub> - V <sub>IL</sub> ) | —    | 0.55 × (V <sub>IH</sub> - V <sub>IL</sub> ) | V    |
| I <sub>OH</sub>  | HIGH-level output current             |   |                 | —   | —    | -12   | mA   |
| I <sub>OL</sub>  | LOW-level output current              |   |                 | —   | —    | 12  | mA   |
|                  |                                       | SDA   |                 | —   | —    | 3   | mA   |
| SR               | Input slew rate                       |   | see Figure 3    | 1   | —    | 4   | V/ns |
|                  | SSC modulation frequency              |   |                 | 30  | —    | 33.3  | kHz  |
|                  | SSC clock input frequency deviation   |   |                 | 0   | —    | -0.50                                       | %    |
| T <sub>amb</sub> | Operating free-air temperature        |   |                 | 0   | —    | +70   | °C   |

**NOTES:**

- Unused inputs must be held HIGH or LOW to prevent them from floating.
- All devices on the I<sup>2</sup>C-bus, with input levels related to V<sub>DD</sub>I<sup>2</sup>C, must have one common supply line to which the pull-up resistor is connected.
- DC input signal voltage specifies the allowable DC execution of differential input.
- Differential input signal voltage specifies the differential voltage |V<sub>TR</sub> - V<sub>CP</sub>| required for switching, where V<sub>TR</sub> is the true input level, and V<sub>CP</sub> is the complementary input level.
- Differential cross-point voltage is expected to track variations of V<sub>DD</sub> and is the voltage at which the differential signals must be crossing.

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**DC ELECTRICAL CHARACTERISTICS**

Over recommended operating conditions.

| SYMBOL                        | PARAMETER   |            | TEST CONDITIONS  | LIMITS   |                     |                           | UNIT |
|-------------------------------|---|------------|--|--|---------------------|---------------------------|------|
|                               |   |            |  | MIN  | TYP <sup>1</sup>    | MAX                       |      |
| V <sub>IK</sub>               | Input voltage   | All inputs | V <sub>DDQ</sub> = 2.3 V; I <sub>I</sub> = -18 mA                  | —  | —                   | -1.2                      | V    |
| V <sub>OH</sub>               | HIGH-level output voltage                                 |            | V <sub>DDQ</sub> = min to max; I <sub>OH</sub> = -1 mA             | V <sub>DDQ</sub> - 0.1                                       | —                   | —                         | V    |
|                               |   |            | V <sub>DDQ</sub> = 2.3 V; I <sub>OH</sub> = -12 mA                 | 1.7  | —                   | —                         | V    |
| V <sub>OL</sub>               | LOW-level output voltage                                  |            | V <sub>DDQ</sub> = min to max; I <sub>OL</sub> = 1 mA              | —  | —                   | 0.1                       | V    |
|                               |   |            | V <sub>DDQ</sub> = 2.3 V; I <sub>OL</sub> = 12 mA                  | —  | —                   | 0.6                       | V    |
|                               |   |            | SDA  | V <sub>DDI<sup>2</sup>C = 3.0 V; I<sub>OL</sub> = 3 mA</sub> | —                   | —                         | 0.4  |
| V <sub>OX</sub>               | Output differential cross voltage                         |            |  | V <sub>DDQ</sub> /2 - 0.2                                    | V <sub>DDQ</sub> /2 | V <sub>DDQ</sub> /2 + 0.2 | V    |
| I <sub>I</sub>                | Input current   | CLK, FBIN  | V <sub>DDQ</sub> = 2.7 V; V <sub>I</sub> = 0 V to 2.7 V            | —  | —                   | ±10                       | μA   |
| I <sub>OZ</sub>               | High impedance state output current                       |            | V <sub>DDQ</sub> = 2.7 V; V <sub>O</sub> = V <sub>DDQ</sub> or GND | —  | —                   | ±10                       | μA   |
| I <sub>DDPD</sub>             | Power-down current on V <sub>DDQ</sub> + AV <sub>DD</sub> |            | CLK at 0 MHz; Σ of I <sub>DD</sub> and AI <sub>DD</sub>            | —  | 150                 | 250                       | μA   |
|                               | Power-down current on V <sub>DDI<sup>2</sup>C</sub>       |            | CLK at 0 MHz; V <sub>DDQ</sub> = 3.6 V                             | —  | 3                   | 20                        | μA   |
| I <sub>DD</sub>               | Dynamic current on V <sub>DDQ</sub>                       |            | f <sub>O</sub> = 100 MHz   | —  | 205                 | 230                       | mA   |
| AI <sub>DD</sub>              | Supply current on AV <sub>DD</sub>                        |            | f <sub>O</sub> = 100 MHz   | —  | 4                   | 6                         | mA   |
| I <sub>DDI<sup>2</sup>C</sub> | Supply current on V <sub>DDI<sup>2</sup>C</sub>           |            | V <sub>DDI<sup>2</sup>C</sub> = 3.6 V;<br>SCL and SDA = 3.6V       | —  | 1                   | 2                         | mA   |
| C <sub>I</sub>                | Input capacitance   |            | V <sub>DDQ</sub> = 2.5 V; V <sub>I</sub> = V <sub>DDQ</sub> or GND | 2  | 2.8                 | 3                         | pF   |

**NOTES:**1. All typical values are at respective nominal V<sub>DDQ</sub>.**TIMING REQUIREMENTS**

Over recommended ranges of supply voltage and operating free-air temperature.

| SYMBOL           | PARAMETER                       | LIMITS |     | UNIT |
|------------------|---------------------------------|--------|-----|------|
|                  |                                 | MIN    | MAX |      |
| f <sub>CLK</sub> | Clock frequency                 | 70     | 190 | MHz  |
|                  | Input clock duty cycle          | 40     | 60  | %    |
|                  | Stabilization time <sup>1</sup> | —      | 100 | μs   |

**NOTE:**

1. Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

**TIMING REQUIREMENTS FOR THE I<sup>2</sup>C INTERFACE**Over recommended ranges of operating free-air temperature and V<sub>DDI<sup>2</sup>C</sub> from 3.3 V to 3.6 V..

| SYMBOL              | PARAMETER  | STANDARD-MODE I <sup>2</sup> C-BUS |      | UNIT |
|---------------------|--|------------------------------------|------|------|
|                     |  | MIN                                | MAX  |      |
| f <sub>SCL</sub>    | SCL clock frequency  | —                                  | 100  | kHz  |
| t <sub>BUF</sub>    | Bus free time between a STOP and START condition                                       | 4.7                                | —    | μs   |
| t <sub>SU;STA</sub> | Set-up time for a repeated START condition   | 4.7                                | —    | μs   |
| t <sub>HD;STA</sub> | Hold time (repeated) START condition. After this period, the first clock is generated. | 4.0                                | —    | μs   |
| t <sub>LOW</sub>    | LOW period of the SCL clock  | 4.7                                | —    | μs   |
| t <sub>HIGH</sub>   | HIGH period of the SCL clock   | 4.0                                | —    | μs   |
| t <sub>r</sub>      | Rise time of both SDA and SCL signals  | —                                  | 1000 | ns   |
| t <sub>f</sub>      | Fall time of both SDA and SCL signals  | —                                  | 300  | ns   |
| t <sub>SU;DAT</sub> | DATA set-up time   | 250                                | —    | ns   |
| t <sub>HD;DAT</sub> | DATA hold time   | 0                                  | —    | ns   |
| t <sub>SU;STO</sub> | Set-up time for STOP condition   | 4                                  | —    | μs   |

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AC CHARACTERISTICS

| SYMBOL                 | PARAMETER                                | TEST CONDITIONS                         | LIMITS |                  |       | UNIT |
|------------------------|--|---|--------|------------------|-------|------|
|                        |  |   | MIN    | TYP              | MAX   |      |
| t <sub>PD</sub>        | Propagation delay time                   | Test mode/CLK to any output             | —      | 3.7              | —     | ns   |
| t <sub>PHL</sub>       | HIGH-to-LOW level propagation delay time | SCL to SDA (acknowledge)                | —      | 500 <sup>1</sup> | —     | ns   |
| t <sub>en</sub>        | Output enable time                       | Test mode/SDA to Y output               | —      | 85               | —     | ns   |
| t <sub>dis</sub>       | Output disable time                      | Test mode/SDA to Y output               | —      | 35               | —     | ns   |
| t <sub>jit(per)</sub>  | Jitter (period); see Figure 4            | 100 MHz to 167 MHz                      | -75    | —                | 75    | ps   |
| t <sub>jit(cc)</sub>   | Jitter (cycle-to-cycle); see Figure 5    | 100 MHz to 167 MHz                      | -75    | —                | 75    | ps   |
| t <sub>jit(hper)</sub> | Half-period jitter; see Figure 6         | 100 MHz to 167 MHz                      | -90    | —                | 90    | ps   |
| t <sub>∅</sub>         | Static phase offset; see Figure 1        | 133 MHz/V <sub>ID</sub> on CLK = 0.71 V | 220    | —                | 450   | ps   |
|                        |  | 167 MHz/V <sub>ID</sub> on CLK = 0.71 V | 140    | —                | 270   | ps   |
| t <sub>slr(o)</sub>    | Output clock slew rate; see Figure 3     | terminated with 120 Ω/14 pF             | 1      | —                | 2     | V/ns |
| t <sub>sk(o)</sub>     | Output skew; see Figure 2                |   | —      | —                | 75    | ps   |
|                        | SSC modulation frequency                 |   | 30     | —                | 33.3  | kHz  |
|                        | SSC clock input frequency deviation      |   | 0.00   | —                | -0.50 | %    |

NOTE:

1. This time is for a PLL frequency of 100 MHz.

AC WAVEFORMS

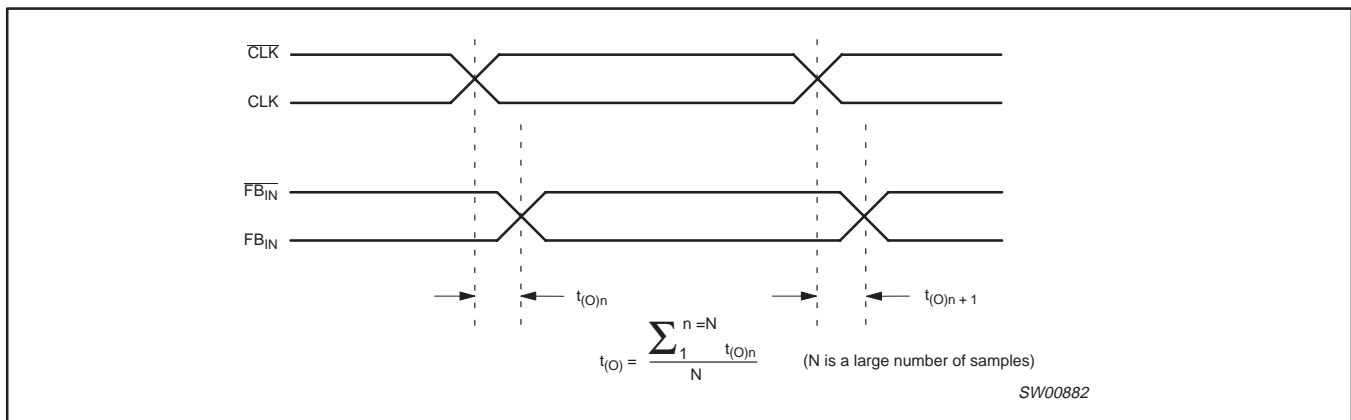


Figure 1. Static phase offset

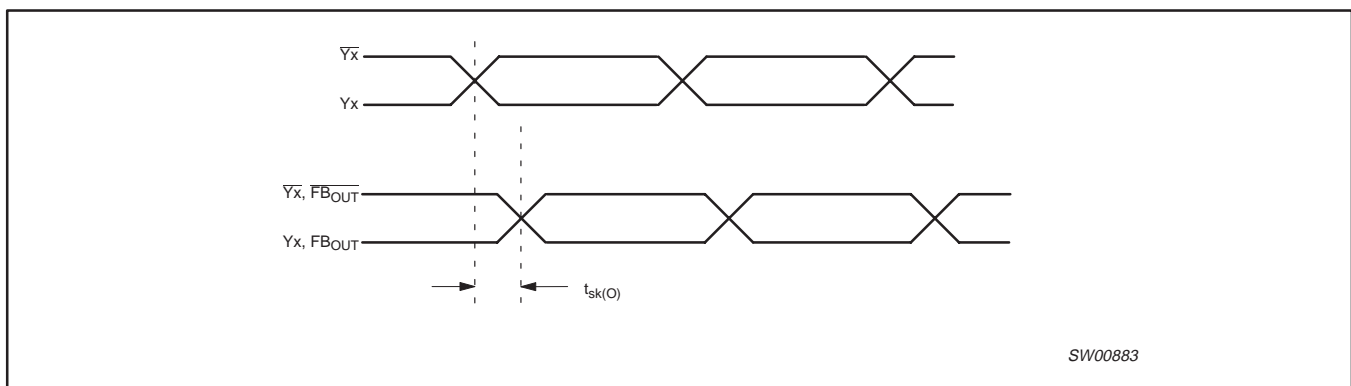


Figure 2. Output skew



70 – 190 MHz I<sup>2</sup>C differential 1:10 clock driver

PCK2057

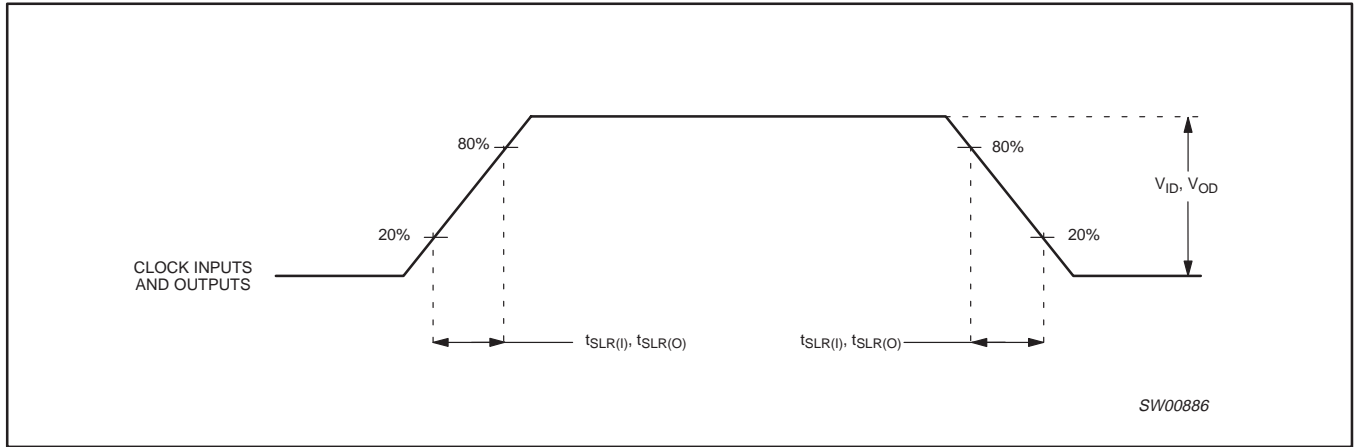


Figure 3. Input and output slew rates

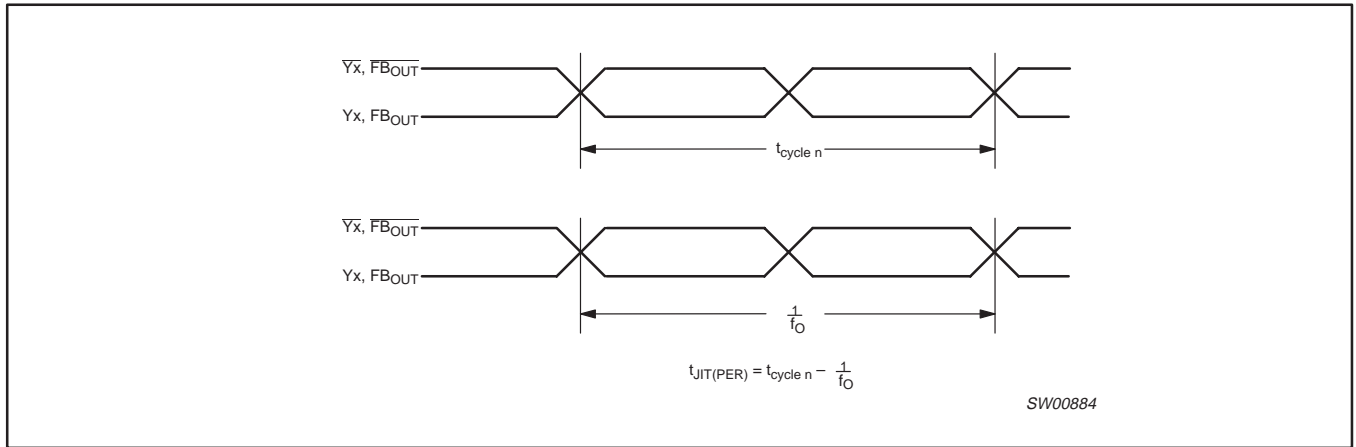


Figure 4. Period jitter

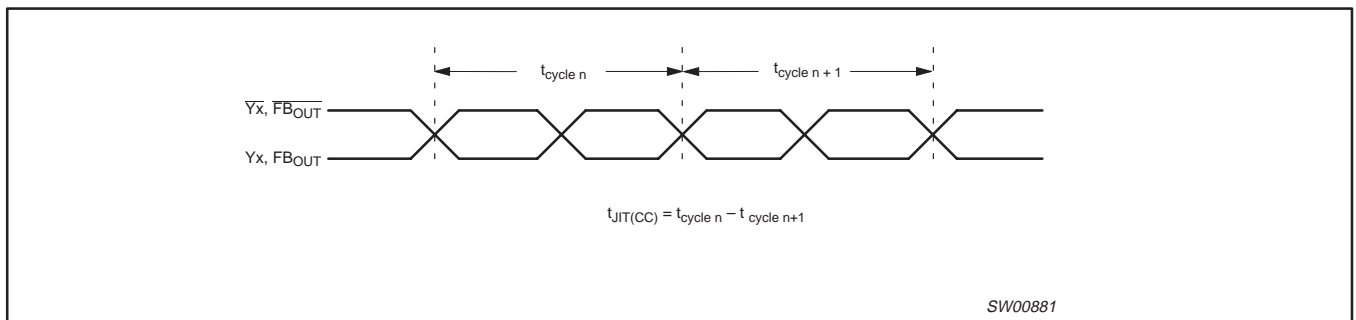


Figure 5. Cycle-to-cycle jitter

# 70 – 190 MHz I<sup>2</sup>C differential 1:10 clock driver

# PCK2057

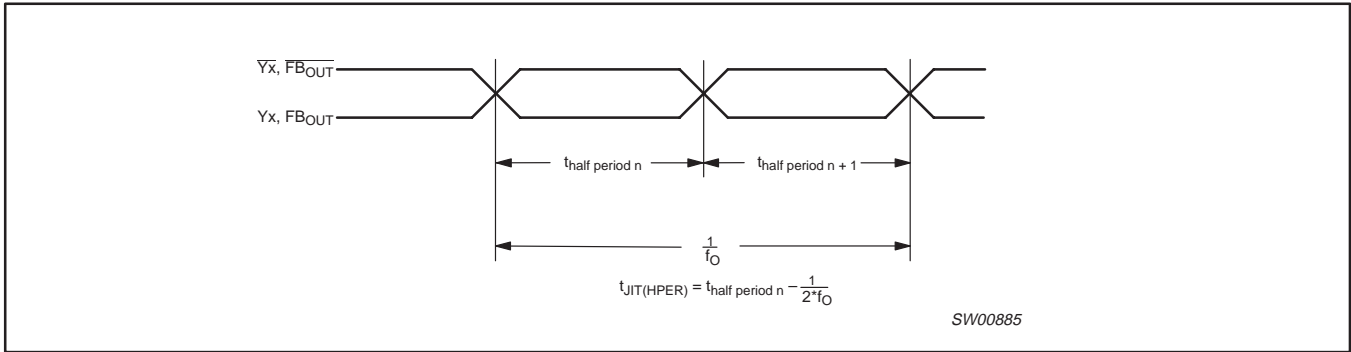


Figure 6. Half-period jitter

## TEST CIRCUIT

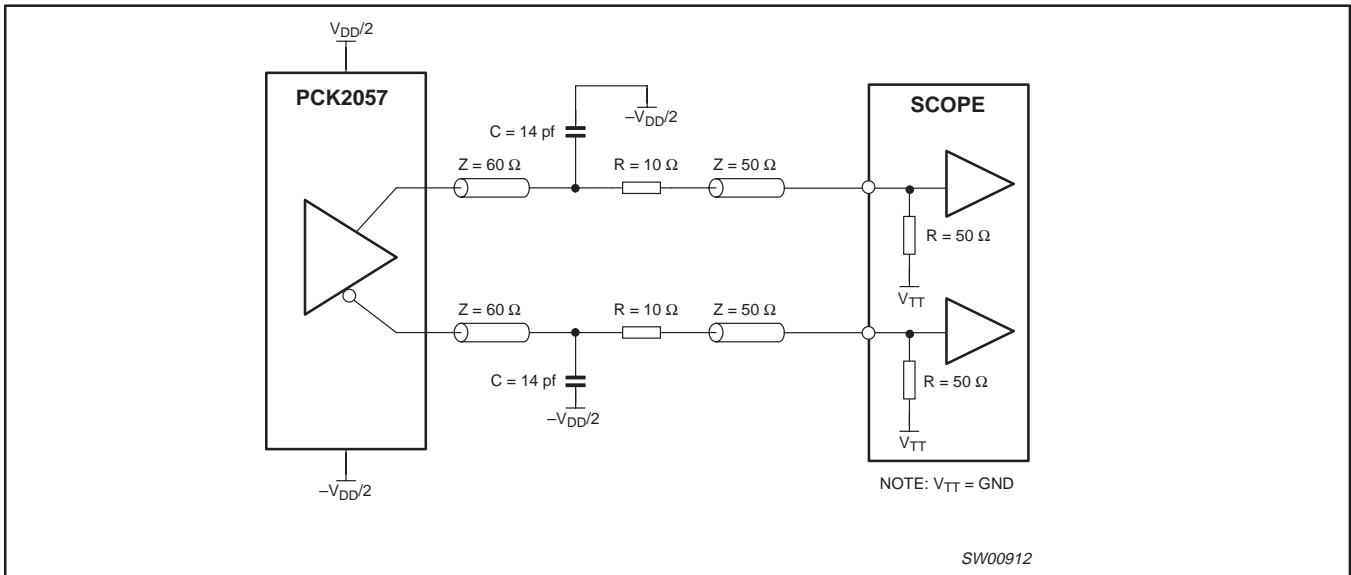


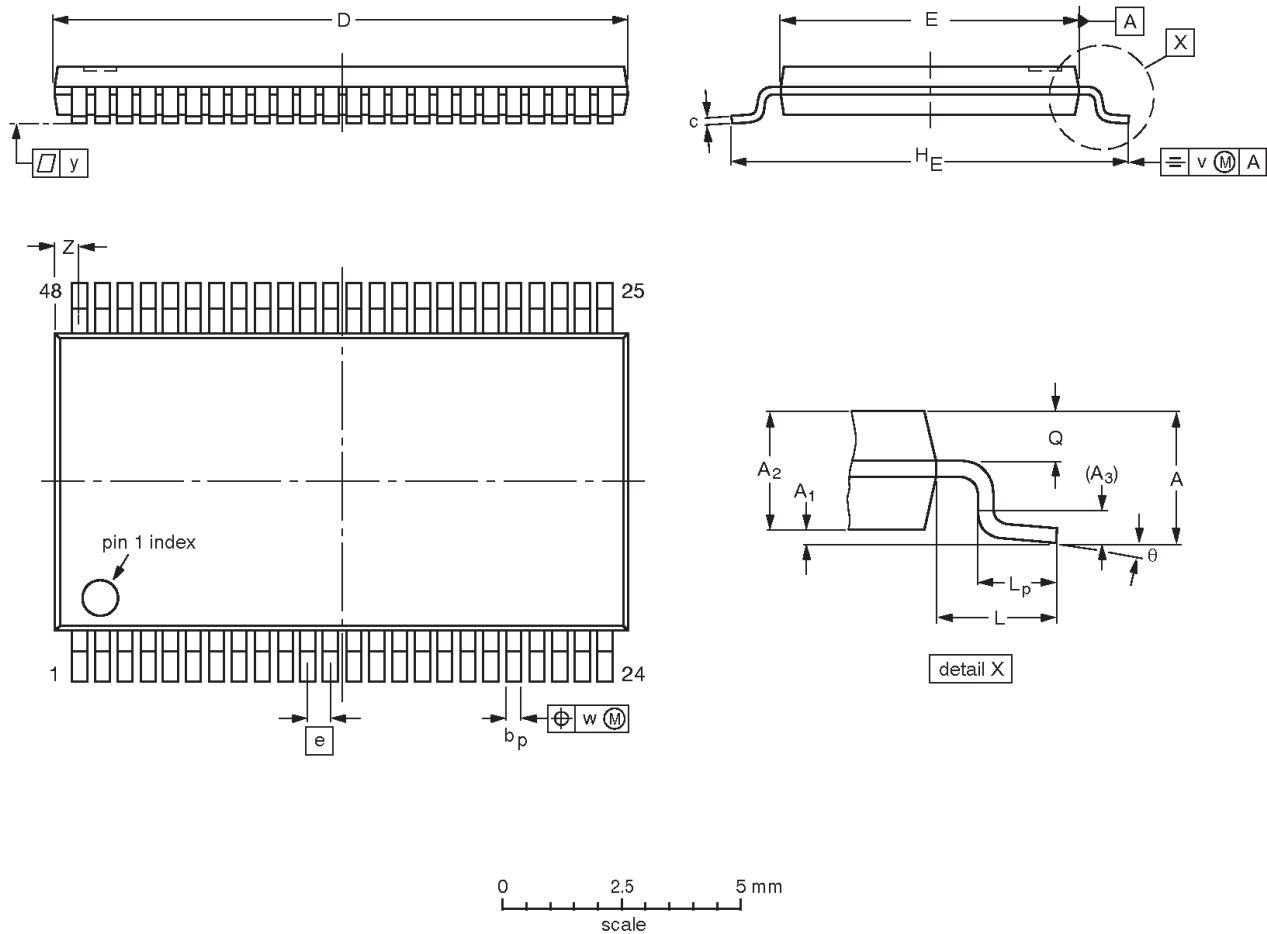
Figure 7. Output load test measurement

70 – 190 MHz I<sup>2</sup>C differential 1:10 clock driver

PCK2057

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



**DIMENSIONS (mm are the original dimensions).**

| UNIT | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c          | D <sup>(1)</sup> | E <sup>(2)</sup> | e   | H <sub>E</sub> | L | L <sub>p</sub> | Q            | v    | w    | y   | Z          | θ        |
|------|--------|----------------|----------------|----------------|----------------|------------|------------------|------------------|-----|----------------|---|----------------|--------------|------|------|-----|------------|----------|
| mm   | 1.2    | 0.15<br>0.05   | 1.05<br>0.85   | 0.25           | 0.28<br>0.17   | 0.2<br>0.1 | 12.6<br>12.4     | 6.2<br>6.0       | 0.5 | 8.3<br>7.9     | 1 | 0.8<br>0.4     | 0.50<br>0.35 | 0.25 | 0.08 | 0.1 | 0.8<br>0.4 | 8°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |        |      |  | EUROPEAN PROJECTION | ISSUE DATE            |
|-----------------|------------|--------|------|--|---------------------|-----------------------|
|                 | IEC        | JEDEC  | EIAJ |  |                     |                       |
| SOT362-1        |            | MO-153 |      |  |                     | -95-02-10<br>99-12-27 |

70 – 190 MHz I<sup>2</sup>C differential 1:10 clock driver

PCK2057



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|----------------------------------|-------------------------------|--|
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