

# SN54ALS651 THRU SN54ALS654, SN54AS651, SN54AS652 SN74ALS651 THRU SN74ALS654, SN74AS651, SN74AS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

D2661, DECEMBER 1983—REVISED MAY 1986

- Bus Transceivers/Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True and Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs to A Bus
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

| DEVICE          | A OUTPUT       | B OUTPUT | LOGIC     |
|-----------------|----------------|----------|-----------|
| 'ALS651, 'AS651 | 3-State        | 3-State  | Inverting |
| 'ALS652, 'AS652 | 3-State        | 3-State  | True      |
| 'ALS653         | Open-Collector | 3-State  | Inverting |
| 'ALS654         | Open-Collector | 3-State  | True      |

## description

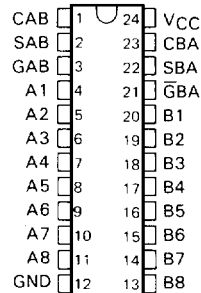
These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and GBA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and GBA. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

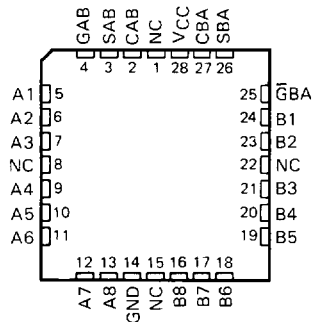
The -1 versions of the SN74ALS651 through SN74ALS654 are identical to the standard versions except that the recommended maximum  $I_{OL}$  is increased to 48 milliamperes. There are no -1 versions of the SN54ALS651 through SN54ALS654.

The SN54' family is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74' family is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS', SN54AS' . . . JT PACKAGE  
SN74ALS', SN74AS' . . . DW OR NT PACKAGE  
(TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE  
SN74ALS', SN74AS' . . . FN PACKAGE  
(TOP VIEW)

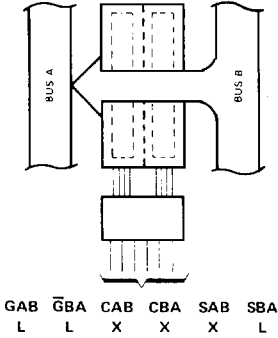


NC No internal connection

**SN54ALS651 THRU SN54ALS654, SN54AS651, SN54AS652  
 SN74ALS651 THRU SN74ALS654, SN74AS651, SN74AS652  
 OCTAL BUS TRANSCEIVERS AND REGISTERS**

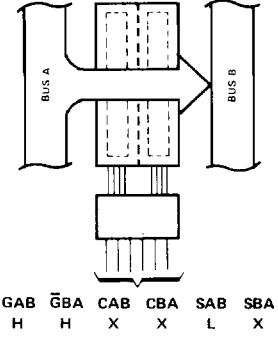
**2**

**ALS and AS Circuits**



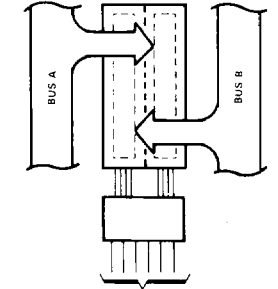
**REAL-TIME TRANSFER  
 BUS B TO BUS A**

|     |             |     |     |     |     |
|-----|-------------|-----|-----|-----|-----|
| GAB | $\bar{G}BA$ | CAB | CBA | SAB | SBA |
| L   | L           | X   | X   | X   | L   |



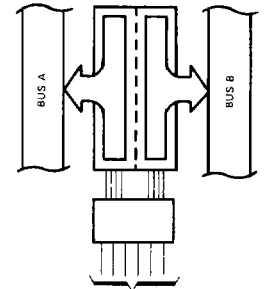
**REAL-TIME TRANSFER  
 BUS A TO BUS B**

|     |             |     |     |     |     |
|-----|-------------|-----|-----|-----|-----|
| GAB | $\bar{G}BA$ | CAB | CBA | SAB | SBA |
| H   | H           | X   | X   | L   | X   |



**STORAGE FROM  
 A AND/OR B**

|     |             |     |     |     |     |
|-----|-------------|-----|-----|-----|-----|
| GAB | $\bar{G}BA$ | CAB | CBA | SAB | SBA |
| X   | H           | ↑   | X   | X   | X   |
| L   | X           | X   | ↑   | X   | X   |
| L   | H           | ↑   | ↑   | X   | X   |



**TRANSFER  
 STORED DATA  
 TO A AND/OR B**

|     |             |        |        |     |     |
|-----|-------------|--------|--------|-----|-----|
| GAB | $\bar{G}BA$ | CAB    | CBA    | SAB | SBA |
| H   | L           | H or L | H or L | H   | H   |

# SN54ALS651 THRU SN54ALS654, SN54AS651, SN54AS652 SN74ALS651 THRU SN74ALS654, SN74AS651, SN74AS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

FUNCTION TABLE

| INPUTS |             |        |        |                | DATA I/O       |                          | OPERATION OR FUNCTION    |  |  |
|--------|-------------|--------|--------|----------------|----------------|--------------------------|--------------------------|--|--|
| GAB    | $\bar{G}BA$ | CAB    | CBA    | SAB            | SBA            | A1 THRU A8               | B1 THRU B8               | 'ALS651, 'ALS653<br>'AS651   | 'ALS652, 'ALS654<br>'AS652                           |
| L      | H           | H or L | H or L | X              | X              | Input                    | Input                    | Isolation  | Isolation  |
| L      | H           | -      | *      | X              | X              | Input                    | Input                    | Store A and B Data   | Store A and B Data                                   |
| X      | H           | -      | H or L | X              | X              | Input                    | Unspecified <sup>†</sup> | Store A, Hold B  | Store A, Hold B                                      |
| H      | H           | -      | *      | X <sup>‡</sup> | X              | Input                    | Output                   | Store A in both registers  | Store A in both registers                            |
| L      | X           | H or L | *      | X              | X              | Unspecified <sup>†</sup> | Input                    | Hold A, Store B  | Hold A, Store B                                      |
| L      | L           | -      | †      | X              | X <sup>‡</sup> | Output                   | Input                    | Store B in both registers  | Store B in both registers                            |
| L      | L           | X      | X      | X              | L              | Output                   | Input                    | Real-Time $\bar{B}$ Data to A Bus                                    | Real-Time B Data to A Bus                            |
| L      | L           | X      | H or L | X              | H              | Output                   | Input                    | Stored $\bar{B}$ Data to A Bus                                       | Stored B Data to A Bus                               |
| H      | H           | X      | X      | L              | X              | Input                    | Output                   | Real-Time A Data to B Bus  | Real-Time A Data to B Bus                            |
| H      | H           | H or L | X      | H              | X              | Input                    | Output                   | Stored A Data to B Bus   | Stored A Data to B Bus                               |
| H      | L           | H or L | H or L | H              | H              | Output                   | Output                   | Stored $\bar{A}$ Data to B Bus and<br>Stored $\bar{B}$ Data to A Bus | Stored A Data to B Bus and<br>Stored B Data to A Bus |

<sup>†</sup>The data output functions may be enabled or disabled by various signals at the GAB or  $\bar{G}BA$  inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

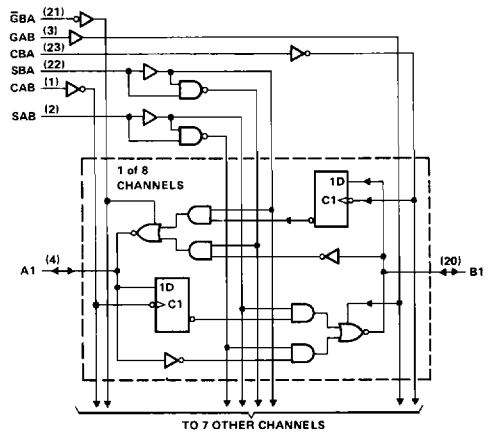
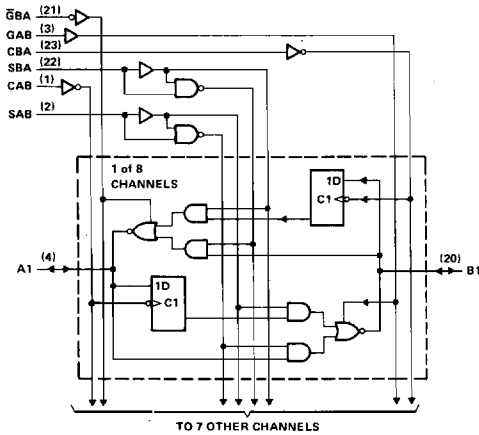
<sup>‡</sup>Select control = L: clocks can occur simultaneously.

Select control = H: clocks must be staggered in order to load both registers.

### logic diagram (positive logic)

'ALS651, 'AS651, 'ALS653

'ALS652, 'AS652, 'ALS654



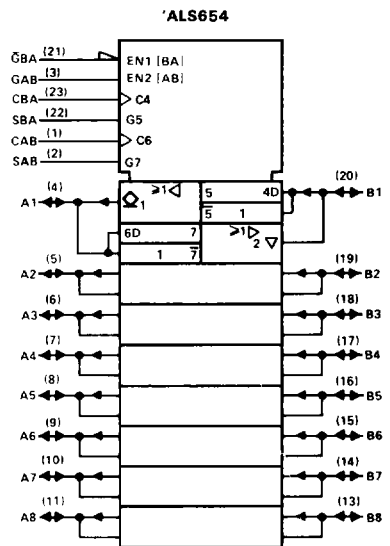
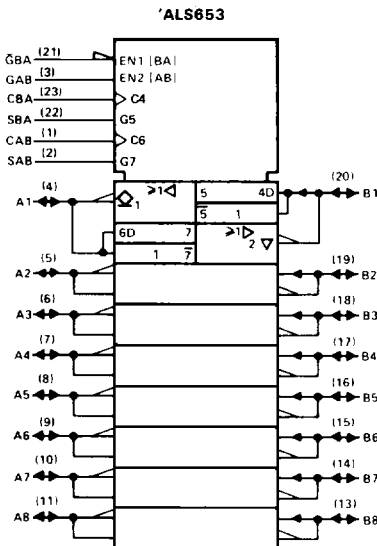
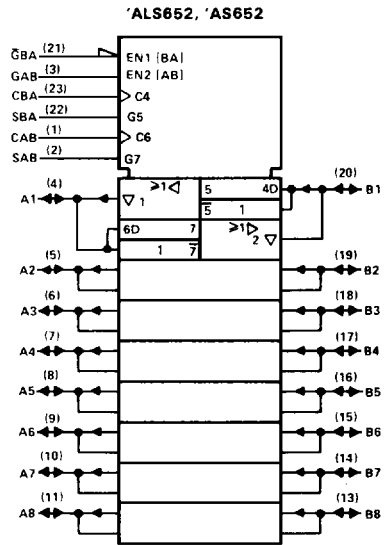
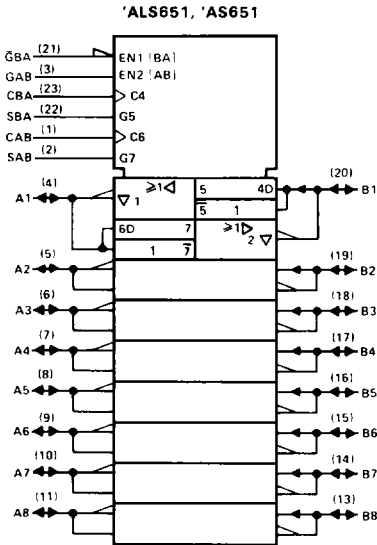
Pin numbers shown are for DW, JT, and NT packages.

**SN54ALS651 THRU SN54ALS654, SN54AS651, SN54AS652  
SN74ALS651 THRU SN74ALS654, SN74AS651, SN74AS652  
OCTAL BUS TRANSCEIVERS AND REGISTERS**

logic symbols†

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†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.



# SN54ALS651, SN54ALS652, SN74ALS651, SN74ALS652

## OCTAL BUS TRANSCEIVERS AND REGISTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS   | SN54ALS651<br>SN54ALS652                        |                  | SN74ALS651<br>SN74ALS652 |      | UNIT |               |    |
|------------|---|---|------------------|--------------------------|------|------|---------------|----|
|            |   | MIN   | MAX              | MIN                      | TYP† |      | MAX           |    |
| $V_{IK}$   | $V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$                     |   | -1.2             |                          |      | -1.2 | V             |    |
| $V_{OH}$   | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $I_{OH} = -0.4\text{ mA}$ | $V_{CC} - 2$                                    |                  | $V_{CC} - 2$             |      |      | V             |    |
|            | $V_{CC} = 4.5\text{ V}$ , $I_{OH} = -3\text{ mA}$                   | 2.4   | 3.2              | 2.4                      | 3.2  |      |               |    |
|            | $V_{CC} = 4.5\text{ V}$ , $I_{OH} = -12\text{ mA}$                  | 2   |                  |                          |      |      |               |    |
|            | $V_{CC} = 4.5\text{ V}$ , $I_{OH} = -15\text{ mA}$                  |   |                  | 2                        |      |      |               |    |
| $V_{OL}$   | $V_{CC} = 4.5\text{ V}$ , $I_{OL} = 12\text{ mA}$                   | 0.25  | 0.4              | 0.25                     | 0.4  |      | V             |    |
|            | $V_{CC} = 4.5\text{ V}$ , $I_{OL} = 24\text{ mA}$                   |   |                  | 0.35                     | 0.5  |      |               |    |
|            | $V_{CC} = 4.75\text{ V}$ , $I_{OL} = 48\text{ mA}$ (-1 versions)    |   |                  |                          |      |      |               |    |
| $I_I$      | Control inputs  | $V_{CC} = 5.5\text{ V}$ , $V_I = 7\text{ V}$    |                  | 0.1                      |      | 0.1  | mA            |    |
|            | A or B ports  | $V_{CC} = 5.5\text{ V}$ , $V_I = 5.5\text{ V}$  |                  | 0.1                      |      | 0.1  |               |    |
| $I_{IH}$   | Control inputs  | $V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$  |                  | 20                       |      | 20   | $\mu\text{A}$ |    |
|            | A or B ports†   |   |                  | 20                       |      | 20   |               |    |
| $I_{IL}$   | Control inputs  | $V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$  |                  | -0.2                     |      | -0.2 | mA            |    |
|            | A or B ports†   |   |                  | -0.2                     |      | -0.2 |               |    |
| $I_O^{\S}$ | B ports   | $V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$ | -30              | -112                     | -30  | -112 | mA            |    |
| $I_{CC}$   | 'ALS651   | $V_{CC} = 5.5\text{ V}$                         | Outputs high     | 42                       | 68   | 42   | 68            | mA |
|            |   |   | Outputs low      | 52                       | 82   | 52   | 82            |    |
|            |   |   | Outputs disabled | 52                       | 82   | 52   | 82            |    |
|            |   |   | Outputs high     | 47                       | 76   | 47   | 76            |    |
|            |   |   | Outputs low      | 55                       | 88   | 55   | 88            |    |
|            |   |   | Outputs disabled | 55                       | 88   | 55   | 88            |    |
| 'ALS652    | $V_{CC} = 5.5\text{ V}$   |   | Outputs high     | 47                       | 76   | 47   | 76            | mA |
|            |   |   | Outputs low      | 55                       | 88   | 55   | 88            |    |
|            |   |   | Outputs disabled | 55                       | 88   | 55   | 88            |    |
|            |   |   | Outputs high     | 47                       | 76   | 47   | 76            |    |
|            |   |   | Outputs low      | 55                       | 88   | 55   | 88            |    |
|            |   |   | Outputs disabled | 55                       | 88   | 55   | 88            |    |

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

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# SN54ALS651, SN54ALS652, SN74ALS651, SN74ALS652

## OCTAL BUS TRANSCEIVERS AND REGISTERS

### ALS651 switching characteristics (see Note 1)

| PARAMETER        | FROM (INPUT)                                  | TO (OUTPUT) | V <sub>CC</sub> = 5 V,<br>C <sub>L</sub> = 50 pF,<br>R1 = 500 Ω,<br>R2 = 500 Ω,<br>T <sub>A</sub> = 25 °C |     |     | V <sub>CC</sub> = 4.5 V to 5.5 V,<br>C <sub>L</sub> = 50 pF,<br>R1 = 500 Ω,<br>R2 = 500 Ω,<br>T <sub>A</sub> = MIN to MAX |     |            | UNIT |     |  |    |  |    |    |    |
|------------------|---|-------------|---|-----|-----|---|-----|------------|------|-----|--|----|--|----|----|----|
|                  |   |             | ALS651  |     |     | SN54ALS651  |     | SN74ALS651 |      |     |  |    |  |    |    |    |
|                  |   |             | MIN   | TYP | MAX | MIN   | MAX | MIN        |      | MAX |  |    |  |    |    |    |
| f <sub>max</sub> |   |             | 50  |     |     | 35  |     | 40         |      | MHz |  |    |  |    |    |    |
| t <sub>PLH</sub> | CBA or CAB                                    | A or B      | 20  |     |     | 10  |     | 38         |      | 10  |  | 32 |  | ns |    |    |
| t <sub>PHL</sub> |   |             | 11  |     |     | 5   |     | 21         |      | 5   |  | 17 |  |    |    |    |
| t <sub>PLH</sub> | A or B  | B or A      | 9   |     |     | 4   |     | 20         |      | 4   |  | 18 |  | ns |    |    |
| t <sub>PHL</sub> |   |             | 5   |     |     | 2   |     | 12         |      | 2   |  | 10 |  |    |    |    |
| t <sub>PLH</sub> | SBA or SAB <sup>†</sup><br>(with A or B low)  | A or B      | 24  |     |     | 13  |     | 45         |      | 13  |  | 38 |  | ns |    |    |
| t <sub>PHL</sub> |   |             | 13  |     |     | 7   |     | 25         |      | 7   |  | 21 |  |    |    |    |
| t <sub>PLH</sub> | SBA or SAB <sup>†</sup><br>(with A or B high) | A or B      | 15  |     |     | 8   |     | 30         |      | 8   |  | 25 |  | ns |    |    |
| t <sub>PHL</sub> |   |             | 13  |     |     | 18  |     | 7          |      | 25  |  | 7  |  |    | 21 |    |
| t <sub>PZH</sub> | $\overline{\text{G}}\text{BA}$                | A           | 12  |     |     | 5   |     | 22         |      | 5   |  | 20 |  | ns |    |    |
| t <sub>PZL</sub> |   |             | 11  |     |     | 15  |     | 5          |      | 21  |  | 5  |  |    | 18 |    |
| t <sub>PHZ</sub> | $\overline{\text{G}}\text{BA}$                | A           | 4   |     |     | 7   |     | 2          |      | 10  |  | 2  |  | 9  |    | ns |
| t <sub>PLZ</sub> |   |             | 7   |     |     | 10  |     | 3          |      | 16  |  | 3  |  | 12 |    |    |
| t <sub>PZH</sub> | GAB   | B           | 14  |     |     | 19  |     | 7          |      | 25  |  | 7  |  | 22 |    | ns |
| t <sub>PZL</sub> |   |             | 13  |     |     | 18  |     | 7          |      | 25  |  | 7  |  | 21 |    |    |
| t <sub>PHZ</sub> | GAB   | B           | 5   |     |     | 10  |     | 2          |      | 14  |  | 2  |  | 12 |    | ns |
| t <sub>PLZ</sub> |   |             | 7   |     |     | 10  |     | 2          |      | 20  |  | 2  |  | 14 |    |    |

### ALS652 switching characteristics (see Note 1)

| PARAMETER        | FROM (INPUT)                                  | TO (OUTPUT) | V <sub>CC</sub> = 5 V,<br>C <sub>L</sub> = 50 pF,<br>R1 = 500 Ω,<br>R2 = 500 Ω,<br>T <sub>A</sub> = 25 °C |     |     | V <sub>CC</sub> = 4.5 V to 5.5 V,<br>C <sub>L</sub> = 50 pF,<br>R1 = 500 Ω,<br>R2 = 500 Ω,<br>T <sub>A</sub> = MIN to MAX |     |            | UNIT |     |  |    |  |    |  |    |
|------------------|---|-------------|---|-----|-----|---|-----|------------|------|-----|--|----|--|----|--|----|
|                  |   |             | ALS652  |     |     | SN54ALS652  |     | SN74ALS652 |      |     |  |    |  |    |  |    |
|                  |   |             | MIN   | TYP | MAX | MIN   | MAX | MIN        |      | MAX |  |    |  |    |  |    |
| f <sub>max</sub> |   |             | 50  |     |     | 35  |     | 40         |      | MHz |  |    |  |    |  |    |
| t <sub>PLH</sub> | CBA or CAB                                    | A or B      | 20  |     |     | 25  |     | 10         |      | 35  |  | 10 |  | 30 |  | ns |
| t <sub>PHL</sub> |   |             | 11  |     |     | 15  |     | 5          |      | 20  |  | 5  |  | 17 |  |    |
| t <sub>PLH</sub> | A or B  | B or A      | 11  |     |     | 15  |     | 5          |      | 20  |  | 5  |  | 18 |  | ns |
| t <sub>PHL</sub> |   |             | 8   |     |     | 10  |     | 3          |      | 15  |  | 3  |  | 12 |  |    |
| t <sub>PLH</sub> | SBA or SAB <sup>†</sup><br>(with A or B low)  | A or B      | 24  |     |     | 32  |     | 15         |      | 40  |  | 15 |  | 35 |  | ns |
| t <sub>PHL</sub> |   |             | 13  |     |     | 17  |     | 6          |      | 23  |  | 6  |  | 20 |  |    |
| t <sub>PLH</sub> | SBA or SAB <sup>†</sup><br>(with A or B high) | A or B      | 17  |     |     | 22  |     | 8          |      | 30  |  | 8  |  | 25 |  | ns |
| t <sub>PHL</sub> |   |             | 13  |     |     | 17  |     | 5          |      | 24  |  | 5  |  | 20 |  |    |
| t <sub>PZH</sub> | $\overline{\text{G}}\text{BA}$                | A           | 10  |     |     | 15  |     | 3          |      | 20  |  | 3  |  | 17 |  | ns |
| t <sub>PZL</sub> |   |             | 10  |     |     | 14  |     | 5          |      | 22  |  | 5  |  | 18 |  |    |
| t <sub>PHZ</sub> | $\overline{\text{G}}\text{BA}$                | A           | 6   |     |     | 8   |     | 1          |      | 12  |  | 1  |  | 10 |  | ns |
| t <sub>PLZ</sub> |   |             | 10  |     |     | 13  |     | 2          |      | 20  |  | 2  |  | 16 |  |    |
| t <sub>PZH</sub> | GAB   | B           | 15  |     |     | 20  |     | 8          |      | 25  |  | 8  |  | 22 |  | ns |
| t <sub>PZL</sub> |   |             | 12  |     |     | 16  |     | 6          |      | 21  |  | 6  |  | 18 |  |    |
| t <sub>PHZ</sub> | GAB   | B           | 6   |     |     | 8   |     | 1          |      | 12  |  | 1  |  | 10 |  | ns |
| t <sub>PLZ</sub> |   |             | 10  |     |     | 13  |     | 2          |      | 21  |  | 2  |  | 16 |  |    |

<sup>†</sup>These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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ALS and AS Circuits





## SN54ALS653, SN54ALS654, SN74ALS653, SN74ALS654 OCTAL BUS TRANSCEIVERS AND REGISTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                   |                           | TEST CONDITIONS   | SN54ALS653<br>SN54ALS654 |                      | SN74ALS653<br>SN74ALS654 |                      | UNIT |    |    |
|-----------------------------|---------------------------|---|--------------------------|----------------------|--------------------------|----------------------|------|----|----|
|                             |                           |   | MIN                      | TYP <sup>†</sup> MAX | MIN                      | TYP <sup>†</sup> MAX |      |    |    |
| V <sub>IK</sub>             |                           | V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA                | -1.2                     |                      | -1.2                     |                      | V    |    |    |
| V <sub>OH</sub>             | B ports                   | V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = -0.4 mA     | V <sub>CC</sub> -2       |                      | V <sub>CC</sub> -2       |                      | V    |    |    |
|                             |                           | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA                | 2.4                      | 3.2                  | 2.4                      | 3.2                  |      |    |    |
|                             |                           | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -12 mA               | 2                        |                      |                          |                      |      |    |    |
|                             |                           | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -15 mA               |                          |                      | 2                        |                      |      |    |    |
| I <sub>OH</sub>             | A ports                   | V <sub>CC</sub> = 4.5 V, V <sub>OH</sub> = 5.5 V                | 0.1                      |                      | 0.1                      |                      | mA   |    |    |
| V <sub>OL</sub>             |                           | V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 12 mA                | 0.25                     | 0.4                  | 0.25                     | 0.4                  | V    |    |    |
|                             |                           | V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 24 mA                |                          |                      | 0.35                     | 0.5                  |      |    |    |
|                             |                           | V <sub>CC</sub> = 4.75 V, I <sub>OL</sub> = 48 mA (-1 versions) |                          |                      |                          |                      |      |    |    |
| I <sub>I</sub>              | Control inputs            | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V                   | 0.1                      |                      | 0.1                      |                      | mA   |    |    |
|                             | A or B ports              | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 5.5 V                 | 0.1                      |                      | 0.1                      |                      |      |    |    |
| I <sub>IH</sub>             | Control inputs            | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V                 | 20                       |                      | 20                       |                      | μA   |    |    |
|                             | A or B ports <sup>‡</sup> |   | 20                       |                      | 20                       |                      |      |    |    |
| I <sub>IL</sub>             | Control inputs            | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V                 | -0.2                     |                      | -0.2                     |                      | mA   |    |    |
|                             | A or B ports <sup>‡</sup> |   | -0.2                     |                      | -0.2                     |                      |      |    |    |
| I <sub>O</sub> <sup>§</sup> | B ports                   | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V                | -30                      | -112                 | -30                      | -112                 | mA   |    |    |
| I <sub>CC</sub>             | 'ALS653                   | V <sub>CC</sub> = 5.5 V   | Outputs high             |                      | 47                       | 76                   | 47   | 76 | mA |
|                             |                           |   | Outputs low              |                      | 55                       | 88                   | 55   | 88 |    |
|                             |                           |   | Outputs disabled         |                      | 55                       | 88                   | 55   | 88 |    |
|                             | 'ALS654                   |   | Outputs high             |                      | 47                       | 76                   | 47   | 76 |    |
|                             |                           |   | Outputs low              |                      | 55                       | 88                   | 55   | 88 |    |
|                             |                           |   | Outputs disabled         |                      | 55                       | 88                   | 55   | 88 |    |

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>‡</sup> For I/O ports, the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

<sup>§</sup> The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I<sub>OS</sub>.

N

ALS and AS Circuits

# SN54ALS653, SN54ALS654, SN74ALS653, SN74ALS654

## OCTAL BUS TRANSCEIVERS AND REGISTERS

switching characteristics (see Note 1)

| PARAMETER        | FROM (INPUT)     | TO (OUTPUT) | V <sub>CC</sub> = 5 V,<br>C <sub>L</sub> = 50 pF,<br>R <sub>L</sub> = 680 Ω (A outputs),<br>R <sub>1</sub> = R <sub>2</sub> = 500 Ω (B outputs),<br>T <sub>A</sub> = 25°C |     |     | V <sub>CC</sub> = 4.5 V to 5.5 V,<br>C <sub>L</sub> = 50 pF,<br>R <sub>L</sub> = 680 Ω (A outputs),<br>R <sub>2</sub> = R <sub>2</sub> = 500 Ω (B outputs),<br>T <sub>A</sub> = MIN to MAX |     |                          |     | UNIT |
|------------------|------------------|-------------|---|-----|-----|--|-----|--------------------------|-----|------|
|                  |                  |             | ALS653<br>ALS654  |     |     | SN54ALS653<br>SN54ALS654   |     | SN74ALS653<br>SN74ALS654 |     |      |
|                  |                  |             | MIN   | TYP | MAX | MIN  | MAX | MIN                      | MAX |      |
| f <sub>max</sub> |                  |             |   | 40  |     | 25   |     | 35                       |     | MHz  |
| t <sub>PLH</sub> | CBA              | A           |   | 30  | 50  | 16   | 71  | 16                       | 64  | ns   |
| t <sub>PHL</sub> |                  |             |   | 11  | 15  | 6  | 24  | 6                        | 22  |      |
| t <sub>PLH</sub> | CAB              | B           |   | 20  | 25  | 10   | 35  | 10                       | 30  | ns   |
| t <sub>PHL</sub> |                  |             |   | 11  | 15  | 5  | 20  | 5                        | 17  |      |
| t <sub>PLH</sub> | A                | B           |   | 11  | 15  | 5  | 20  | 5                        | 18  | ns   |
| t <sub>PHL</sub> |                  |             |   | 10  | 13  | 2  | 18  | 2                        | 15  |      |
| t <sub>PLH</sub> | B                | A           |   | 20  | 44  | 12   | 63  | 12                       | 56  | ns   |
| t <sub>PHL</sub> |                  |             |   | 10  | 13  | 2  | 18  | 2                        | 15  |      |
| t <sub>PLH</sub> | SBA <sup>†</sup> | A           |   | 35  | 50  | 19   | 68  | 19                       | 62  | ns   |
| t <sub>PHL</sub> | (with B low)     |             |   | 15  | 22  | 5  | 27  | 5                        | 25  |      |
| t <sub>PLH</sub> | SBA <sup>†</sup> | A           |   | 35  | 50  | 19   | 68  | 19                       | 62  | ns   |
| t <sub>PHL</sub> | (with B high)    |             |   | 15  | 22  | 5  | 27  | 5                        | 25  |      |
| t <sub>PLH</sub> | SAB <sup>†</sup> | B           |   | 24  | 32  | 12   | 40  | 15                       | 35  | ns   |
| t <sub>PHL</sub> | (with A low)     |             |   | 13  | 18  | 6  | 25  | 6                        | 22  |      |
| t <sub>PLH</sub> | SAB <sup>†</sup> | B           |   | 18  | 22  | 8  | 30  | 8                        | 25  | ns   |
| t <sub>PHL</sub> | (with A high)    |             |   | 13  | 19  | 6  | 25  | 6                        | 22  |      |
| t <sub>PLH</sub> | G <sub>B</sub> A | A           |   | 17  | 23  | 6  | 35  | 6                        | 30  | ns   |
| t <sub>PHL</sub> |                  |             |   |     | 14  | 20   | 6   | 27                       | 6   |      |
| t <sub>PZH</sub> | GAB              | B           |   | 15  | 20  | 8  | 25  | 8                        | 22  | ns   |
| t <sub>PZL</sub> |                  |             |   |     | 13  | 17   | 6   | 25                       | 6   |      |
| t <sub>PHZ</sub> | GAB              | B           |   | 8   | 12  | 1  | 16  | 1                        | 14  | ns   |
| t <sub>PLZ</sub> |                  |             |   |     | 10  | 13   | 2   | 21                       | 2   |      |

<sup>†</sup> These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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ALS and AS Circuits

# SN54AS651, SN54AS652, SN74AS651, SN74AS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|  |                  |
|--|------------------|
| Supply voltage, $V_{CC}$ .....                                   | 7 V              |
| Input voltage: Control inputs .....                              | 7 V              |
| I/O ports .....  | 5.5 V            |
| Operating free-air temperature range: SN54AS651, SN54AS652 ..... | -55°C C to 125°C |
| SN74AS651, SN74AS652 .....                                       | 0°C to 70°C      |
| Storage temperature range .....                                  | -65°C to 150°C   |

## recommended operating conditions

|             |  | SN54AS651<br>SN54AS652 |     |     | SN74AS651<br>SN74AS652 |     |     | UNIT |
|-------------|--|------------------------|-----|-----|------------------------|-----|-----|------|
|             |  | MIN                    | NOM | MAX | MIN                    | NOM | MAX |      |
| $V_{CC}$    | Supply voltage                                     | 4.5                    | 5   | 5.5 | 4.5                    | 5   | 5.5 | V    |
| $V_{IH}$    | High-level input voltage                           | 2                      |     |     | 2                      |     |     | V    |
| $V_{IL}$    | Low-level input voltage                            |                        |     | 0.8 |                        |     | 0.8 | V    |
| $I_{OH}$    | High-level output current                          |                        |     | -12 |                        |     | -15 | mA   |
| $I_{OL}$    | Low-level output current                           |                        |     | 32  |                        |     | 48  | mA   |
| $f_{clock}$ | Clock frequency                                    | 0                      |     | 75  | 0                      |     | 90  | MHz  |
| $t_w$       | Pulse duration                                     | CBA or CAB high        |     | 6   | 5                      |     |     | ns   |
|             |  | CBA or CAB low         |     | 7   | 6                      |     |     |      |
| $t_{su}$    | Setup time before CAB $\uparrow$ or CBA $\uparrow$ | A or B                 |     | 7   | 6                      |     |     | ns   |
| $t_h$       | Hold time after CAB $\uparrow$ or CBA $\uparrow$   | A or B                 |     | 0   | 0                      |     |     | ns   |
| $T_A$       | Operating free-air temperature $^{\dagger}$        | -55                    |     | 125 | 0                      |     | 70  | °C   |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER     |                         | TEST CONDITIONS            |                   | SN54AS651<br>SN54AS652 |                | SN74AS651<br>SN74AS652 |      | UNIT  |                |     |
|---------------|-------------------------|----------------------------|-------------------|------------------------|----------------|------------------------|------|-------|----------------|-----|
|               |                         |                            |                   | MIN                    | TYP $\uparrow$ | MAX                    | MIN  |       | TYP $\uparrow$ | MAX |
| $V_{IK}$      |                         | $V_{CC} = 4.5$ V,          | $I_I = -18$ mA    |                        |                | -1.2                   |      | -1.2  | V              |     |
| $V_{OH}$      |                         | $V_{CC} = 4.5$ V to 5.5 V, | $I_{OH} = -2$ mA  | $V_{CC} - 2$           |                | $V_{CC} - 2$           |      |       | V              |     |
|               |                         | $V_{CC} = 4.5$ V,          | $I_{OH} = -3$ mA  | 2.4                    | 3.2            | 2.4                    | 3.2  |       |                |     |
|               |                         | $V_{CC} = 4.5$ V,          | $I_{OH} = -12$ mA | 2                      |                |                        |      |       |                |     |
|               |                         | $V_{CC} = 4.5$ V,          | $I_{OH} = -15$ mA |                        |                | 2                      |      |       |                |     |
| $V_{OL}$      |                         | $V_{CC} = 4.5$ V,          | $I_{OL} = 32$ mA  | 0.25                   | 0.50           |                        |      |       | V              |     |
|               |                         | $V_{CC} = 4.5$ V,          | $I_{OL} = 48$ mA  |                        |                | 0.35                   | 0.50 |       |                |     |
| $I_I$         | Control inputs          | $V_{CC} = 5.5$ V,          | $V_I = 7$ V       |                        |                | 0.1                    |      | 0.1   | mA             |     |
|               | A or B ports            | $V_{CC} = 5.5$ V,          | $V_I = 5.5$ V     |                        |                | 0.1                    |      | 0.1   |                |     |
| $I_{IH}$      | Control inputs          | $V_{CC} = 5.5$ V,          | $V_I = 2.7$ V     |                        |                | 20                     |      | 20    | $\mu$ A        |     |
|               | A or B ports $\ddagger$ |                            |                   |                        |                | 70                     |      | 70    |                |     |
| $I_{IL}$      | Control inputs          | $V_{CC} = 5.5$ V,          | $V_I = 0.4$ V     |                        |                | -0.5                   |      | -0.5  | mA             |     |
|               | A or B ports $\ddagger$ |                            |                   |                        |                | -0.75                  |      | -0.75 |                |     |
| $I_O$ $^{\S}$ |                         | $V_{CC} = 5.5$ V,          | $V_O = 2.25$ V    | -30                    |                | -112                   |      | -30   | -112           | mA  |
| $I_{CC}$      | 'AS651                  | $V_{CC} = 5.5$ V           | Outputs high      |                        | 110            | 185                    |      | 110   | 185            | mA  |
|               |                         |                            | Outputs low       |                        | 120            | 195                    |      | 120   | 195            |     |
|               |                         |                            | Outputs disabled  |                        | 130            | 195                    |      | 130   | 195            |     |
|               | 'AS652                  |                            | Outputs high      |                        | 120            | 195                    |      | 120   | 195            |     |
|               |                         |                            | Outputs low       |                        | 130            | 211                    |      | 130   | 211            |     |
|               |                         |                            | Outputs disabled  |                        | 130            | 211                    |      | 130   | 211            |     |

$\uparrow$  All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ$ C.

$\ddagger$  For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

$\S$  The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

# SN54AS651, SN54AS652, SN74AS651, SN74AS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

AS651 switching characteristics (see Note 1)

| PARAMETER        | FROM<br>(INPUT)         | TO<br>(OUTPUT) | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$<br>$C_L = 50 \text{ pF,}$<br>$R_1 = 500 \Omega,$<br>$R_2 = 500 \Omega,$<br>$T_A = \text{MIN to MAX}$ |     |           |     | UNIT |
|------------------|-------------------------|----------------|--|-----|-----------|-----|------|
|                  |                         |                | SN54AS651  |     | SN74AS651 |     |      |
|                  |                         |                | MIN  | MAX | MIN       | MAX |      |
| $f_{\text{max}}$ |                         |                | 75   |     | 90        |     | MHz  |
| $t_{\text{PLH}}$ | CBA or CAB              | A or B         | 2  | 9.5 | 2         | 8.5 | ns   |
| $t_{\text{PHL}}$ |                         |                | 2  | 10  | 2         | 9   |      |
| $t_{\text{PLH}}$ | A or B                  | B or A         | 2  | 9   | 2         | 8   | ns   |
| $t_{\text{PHL}}$ |                         |                | 1  | 8   | 1         | 7   |      |
| $t_{\text{PLH}}$ | SBA or SAB <sup>†</sup> | A or B         | 2  | 12  | 2         | 11  | ns   |
| $t_{\text{PHL}}$ |                         |                | 2  | 10  | 2         | 9   |      |
| $t_{\text{PZH}}$ | $\bar{G}$ BA            | A              | 2  | 11  | 2         | 10  | ns   |
| $t_{\text{PZL}}$ |                         |                | 3  | 18  | 3         | 16  |      |
| $t_{\text{PHZ}}$ | $\bar{G}$ BA            | A              | 2  | 10  | 2         | 9   | ns   |
| $t_{\text{PLZ}}$ |                         |                | 2  | 10  | 2         | 9   |      |
| $t_{\text{PZH}}$ | GAB                     | B              | 3  | 12  | 3         | 11  | ns   |
| $t_{\text{PZL}}$ |                         |                | 3  | 20  | 3         | 16  |      |
| $t_{\text{PHZ}}$ | GAB                     | B              | 2  | 11  | 2         | 10  | ns   |
| $t_{\text{PLZ}}$ |                         |                | 2  | 12  | 2         | 11  |      |

AS652 switching characteristics (see Note 1)

| PARAMETER        | FROM<br>(INPUT)         | TO<br>(OUTPUT) | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$<br>$C_L = 50 \text{ pF,}$<br>$R_1 = 500 \Omega,$<br>$R_2 = 500 \Omega,$<br>$T_A = \text{MIN to MAX}$ |     |           |     | UNIT |
|------------------|-------------------------|----------------|--|-----|-----------|-----|------|
|                  |                         |                | SN54AS652  |     | SN74AS652 |     |      |
|                  |                         |                | MIN  | MAX | MIN       | MAX |      |
| $f_{\text{max}}$ |                         |                | 75   |     | 90        |     | MHz  |
| $t_{\text{PLH}}$ | CBA or CAB              | A or B         | 2  | 9.5 | 2         | 8.5 | ns   |
| $t_{\text{PHL}}$ |                         |                | 2  | 10  | 2         | 9   |      |
| $t_{\text{PLH}}$ | A or B                  | B or A         | 2  | 11  | 2         | 9   | ns   |
| $t_{\text{PHL}}$ |                         |                | 1  | 8   | 1         | 7   |      |
| $t_{\text{PLH}}$ | SBA or SAB <sup>†</sup> | A or B         | 2  | 12  | 2         | 11  | ns   |
| $t_{\text{PHL}}$ |                         |                | 2  | 10  | 2         | 9   |      |
| $t_{\text{PZH}}$ | $\bar{G}$ BA            | A              | 2  | 11  | 2         | 10  | ns   |
| $t_{\text{PZL}}$ |                         |                | 3  | 18  | 3         | 16  |      |
| $t_{\text{PHZ}}$ | $\bar{G}$ BA            | A              | 2  | 10  | 2         | 9   | ns   |
| $t_{\text{PLZ}}$ |                         |                | 2  | 10  | 2         | 9   |      |
| $t_{\text{PZH}}$ | GAB                     | B              | 3  | 12  | 3         | 11  | ns   |
| $t_{\text{PZL}}$ |                         |                | 3  | 20  | 3         | 16  |      |
| $t_{\text{PHZ}}$ | GAB                     | B              | 2  | 11  | 2         | 10  | ns   |
| $t_{\text{PLZ}}$ |                         |                | 2  | 12  | 2         | 11  |      |

<sup>†</sup> These parameters are measured with the internal output state of the storage register opposite to that of the bus input.  
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2 ALS and AS Circuits