

RC5040

Programmable Synchronous DC-DC Converter

Features

- 85% efficiency
- 350uA quiescent current in shutdown
- 4 Bit DAC for voltage selection
- On-board Power Good function
- Over-Voltage Protection
- Output voltage range from 2V to 3.5V
- Factory trimmed zero TC reference voltage
- Adjustable oscillator frequency to 1MHz
- Drives N-Channel MOSFETs

- 20 pin SOIC package
- Meets Intel VRM specification

Applications

- Programmable power supply for Pentium Pro™ based CPU motherboards
- VRM module for Pentium Pro™ CPU
- Programmable power supply

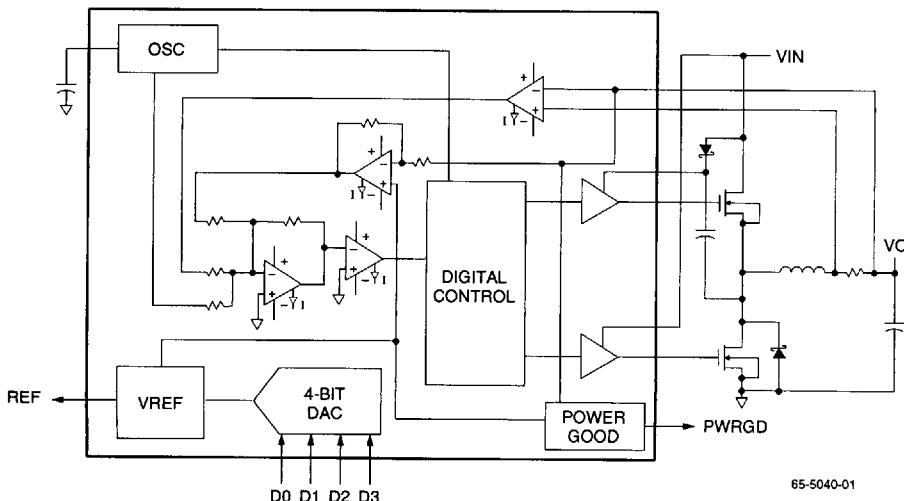
Description

The RC5040 is a synchronous mode DC-DC controller IC dedicated to providing a 5V programmable conversion (2.1V to 3.5V) for Pentium Pro™ CPU power. It can be configured in both the synchronous and non-synchronous modes and with the proper applications circuitry can be used to deliver load current greater than 12 Amps. The RC5040 is designed to operate in a standard PWM control mode under heavy load conditions and as a PFM controller in light load conditions. Its highly accurate zero TC reference eliminates the need for precision external components in order to achieve

tight tolerance voltage regulation. Through the use of the on-board DAC, the RC5040 can generate accurate output voltages from 2.1V up to 3.5V in 0.1V increments. An integrated Power Good function constantly monitors the output voltage and produces a low-going interrupt signal to the Pentium Pro CPU in the event of a out-of-tolerance voltage situation, thereby protecting the CPU. The programmable oscillator can operate from 200KHz to greater than 1MHz to provide for flexibility in choosing external components such as inductors, capacitors, and Power MOSFETs.

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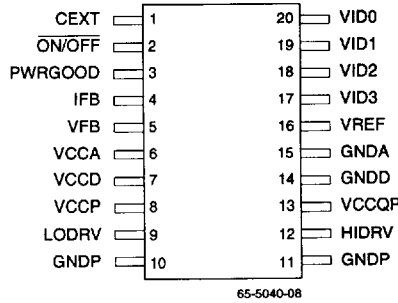
Block Diagram



Rev. 0.9.8

PRELIMINARY INFORMATION describes products that are not in full production at the time of printing. Specifications are based on design goals and limited characterization. They may change without notice. Contact Raytheon for current information.

Pin Assignments



Pin Definitions

Pin Name	Pin Number	Pin Function Description
CEXT	1	External Capacitor for setting oscillator frequency
On/Off	2	A low level on this pin will power down; tie to VCCD if not used
Pwrgood	3	A 3.0V logic level indicated power is within limits
IFB	4	Current Feedback Input
VFB	5	Voltage Feedback Input
VCCA	6	Analog VCC
VCCD	7	Digital VCC
VCCP	8	VCC for synchronous FET output driver
LODRV	9	Synchronous FET driver output
GNDP	10, 11	Power ground for high current drivers
HIDRV	12	High side FET driver output
VCCQP	13	VCC for High side FET output driver
GNDD	14	Digital ground
GNDA	15	Analog ground
VREF	16	Reference voltage output
VID3-VID0	17-20	Voltage identification code input

Note: 0 = Processor pin connected to VSS. 1 = Open.

Absolute Maximum Ratings

(beyond which the device may be damaged)¹

Parameter	Conditions	Min	Typ	Max	Units
V _{IN}	Input Voltage			13	V
V _{CCP}	Driver Voltage			13	V
V _{CCQP}	High FET Driver Supply			13	V
T _J	Junction Temperature			175	°C
T _A	Ambient Operating Temperature	0		70	°C
T _S	Storage Temperature	-65		150	°C
T _L	Lead Soldering Temperature	10 seconds		300	°C

Notes:

1. Functional operation under any of these conditions is NOT implied.

Preliminary Information

Operating Conditions

Parameter		Conditions	Min	Typ	Max	Units
VCC	Supply Voltage		4.5	5	7	V
VCCP	Drivers Supply Voltage		4.5	5	12	V
V _{IH}	Input Voltage, Logic HIGH		2			V
V _{IL}	Input Voltage, Logic LOW				0.8	V

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage	See Voltage Identification Code Table, T _A = 0–70°C	2.1		3.5	V
Output Current			10		A
Set Point Accuracy	I _{LOAD} = 1A includes ripple		0.25	1.5	%
Output Voltage Tempco			40		ppm/°C
Load Regulation	I _{load} = 0.5 to 10A		1		%V _o
Line Regulation	Input Voltage = 4.75 to 5.25V, I _{load} = 10A (See Figure 1)		0.14		%V _o
Output Voltage Ripple			30		mV
Cumulative Accuracy ¹	T _A = 0–70°C		2	5	%
Efficiency	I _{load} = 10A	80	85		%
Power Dissipation			0.1	0.2	W
Output Current Driver		0.5	0.7		A

Notes:

1. Output Voltage Accuracy, Tempco, Load Regulation, Line Regulation, Ripple, & Transient Performance determine the Cumulative Accuracy.

P6 Pins				VDC	Set Point +Ripple ¹ (±mV)	Total Room Temperature Accuracy ² (±mV)	Total System Accuracy ³ (±mV)
VID3	VID2	VID1	VID0				
1	1	1	1	No CPU	-	-	-
1	1	1	0	2.1	32	74	105
1	1	0	1	2.2	33	77	110
1	1	0	0	2.3	35	81	115
1	0	1	1	2.4	36	84	120
1	0	1	0	2.5	37	88	125
1	0	0	1	2.6	39	91	130
1	0	0	0	2.7	41	95	135
0	1	1	1	2.8	42	98	140
0	1	1	0	2.9	44	102	145
0	1	0	1	3.0	45	105	150
0	1	0	0	3.1	47	109	155
0	0	1	1	3.2	48	112	160

P6 Pins				VDC	Set Point +Ripple ¹ (±mV)	Total Room Temperature Accuracy ² (±mV)	Total System Accuracy ³ (±mV)
VID3	VID2	VID1	VID0				
0	0	1	0	3.3	50	116	165
0	0	0	1	3.4	51	119	170
0	0	0	0	3.5	53	123	175

Notes:

1. Includes initial accuracy plus ripple. (±mV).
2. Includes set point accuracy + line reg + load reg + transient (±mV).
3. Includes temperature effects to total accuracy (±mV).

AC Electrical Characteristics¹

T_A = +25°C unless otherwise noted). Refer to Figure 1.

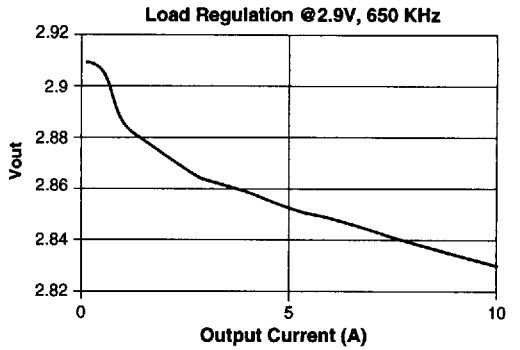
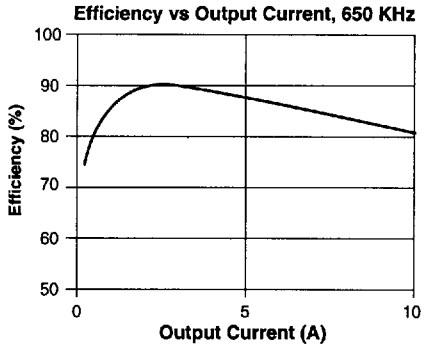
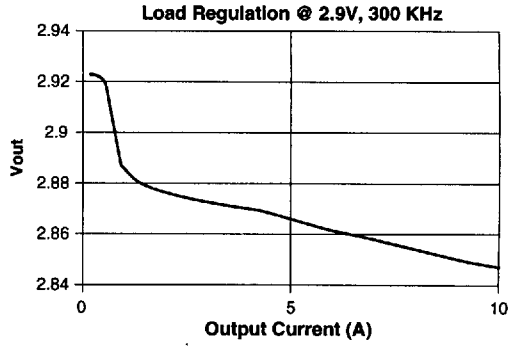
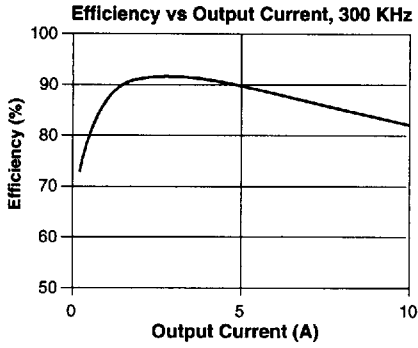
Parameter	Min	Typ	Max	Units
Response Time Sleep-to-Full Load		10		µs
Oscillator Frequency Range	.2		1.2	MHz
Oscillator Frequency Precision		10		%
Maximum Duty Cycle in PWM Mode	90	95		%
Minimum Duty Cycle in PFM Mode			100	ns
IMAX Circuit Detection (Comparator Threshold)		30		mV
Short Circuit Protection/Coil Saturation Detection		80		mV
Response Time to IMAX and Short Circuit Protection		15	30	ns
Soft Start during Power-Up and Power-Down		10		µs

Notes:

1. Guaranteed by design, not tested 100%.

Preliminary Information

Typical Operating Characteristics

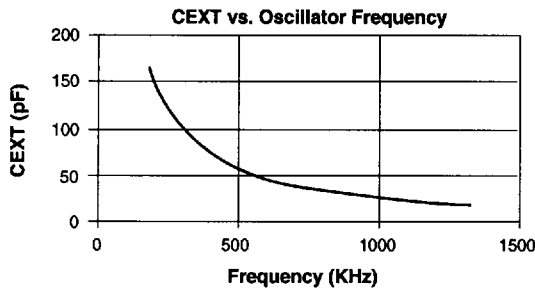
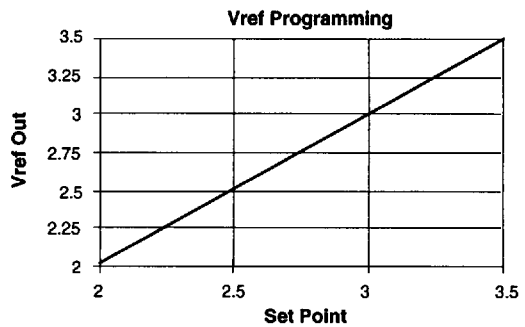
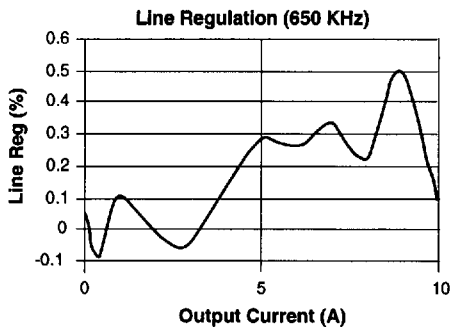
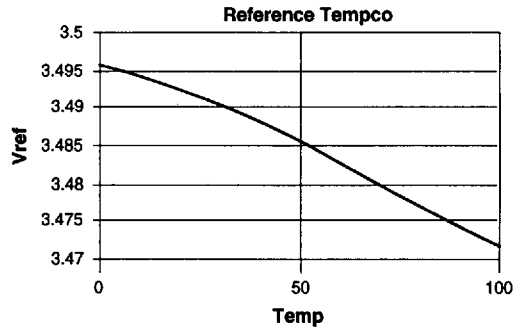
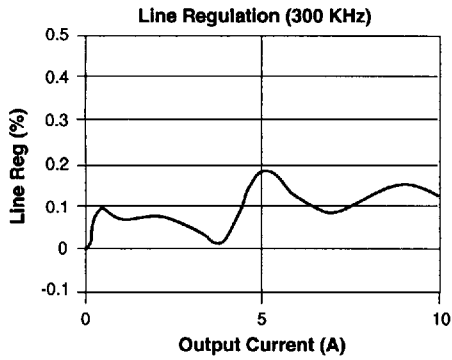


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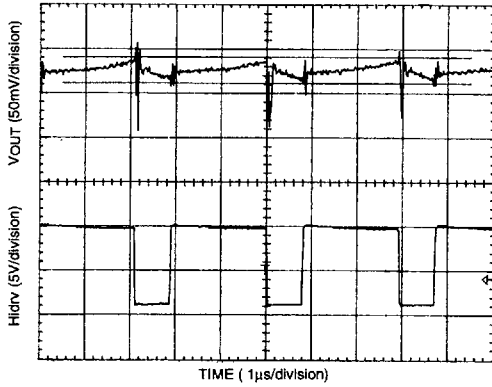
Typical Operating Characteristics (continued)

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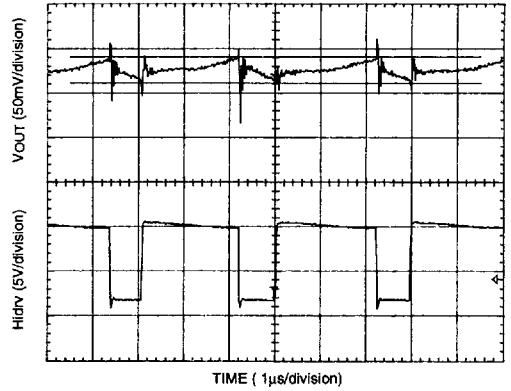


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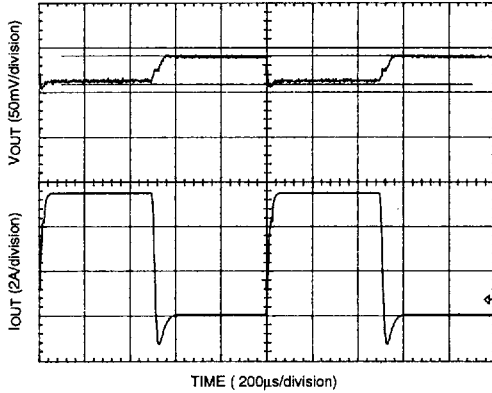
Typical Operating Characteristics (continued)



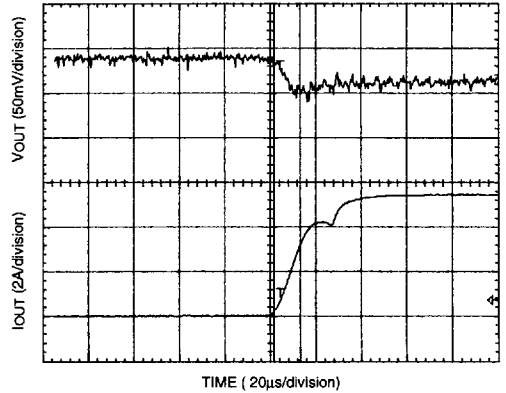
AC Ripple response 2A Load



AC Ripple response 10A Load



Transient Response .2A to 6A Load



Transient Response Magnified

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Test Circuits

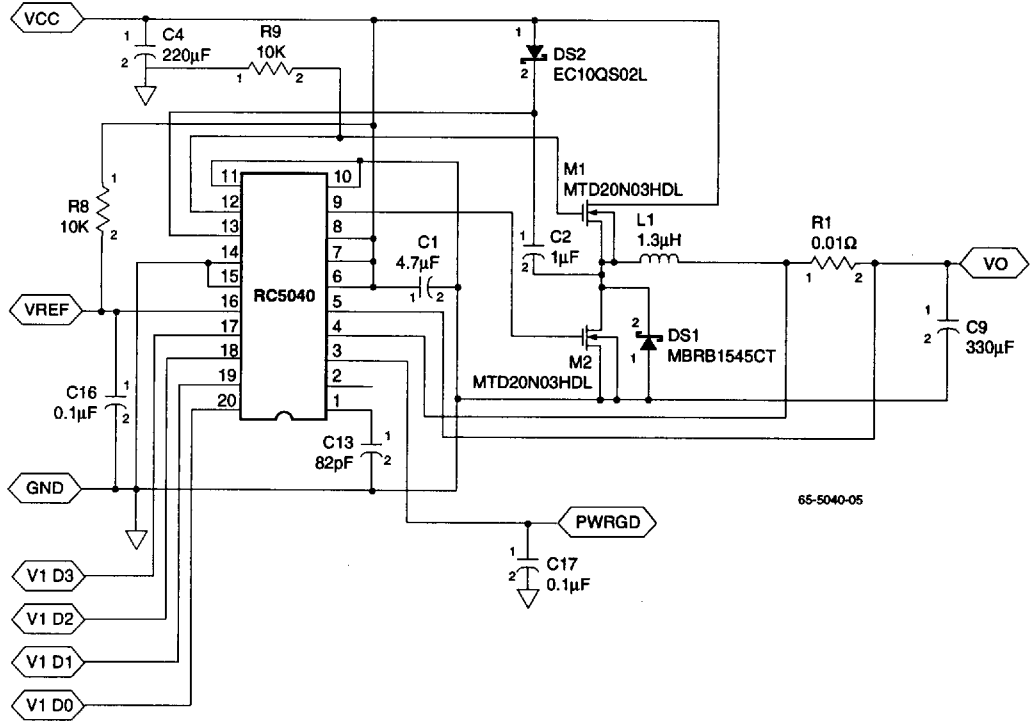
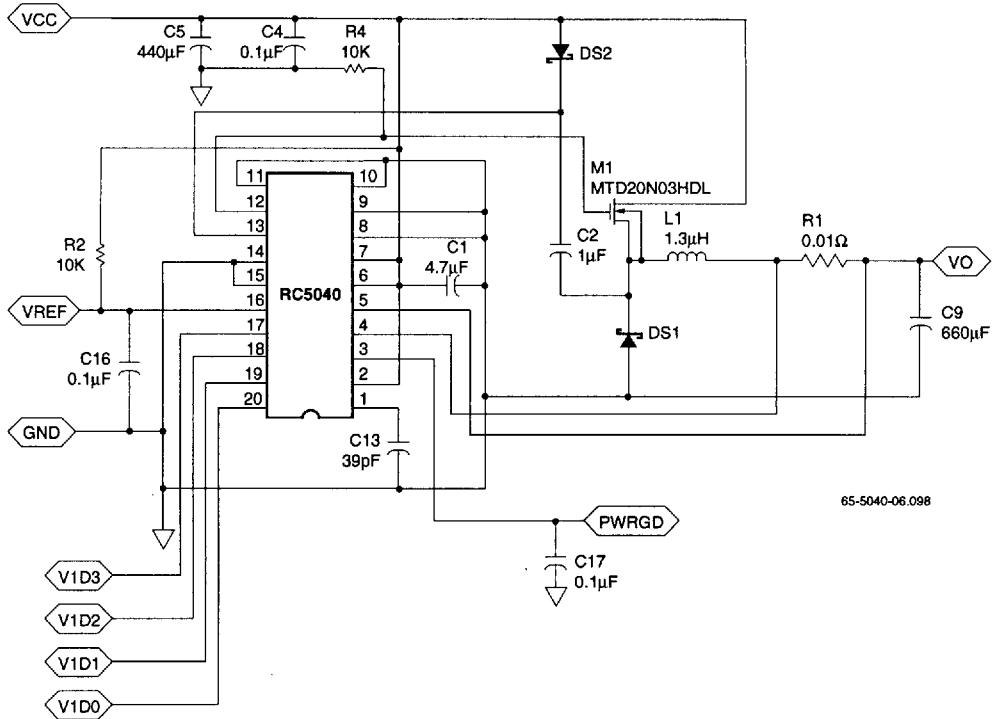


Figure 1. Synchronous DC-DC Conversion Test Configuration

Preliminary Information

Test Circuits (continued)



65-5040-06.098

Figure 2. Non-Synchronous DC-DC Conversion Test Configuration

Table 1. Components for RC5040

RC5040 Standard Application Circuit Bill of Materials			
Ref Designator	Quantity	Part No.	Manufacturer
L1	1	1.3µH CDRH127-1R3NC	Sumida
M1,M2	2	MTD20N03HDL	Motorola
DS1	1	MBRB1545CT	Motorola
DS2	1	EC10QS02L	Nihon
R1	1	.01n LRC-2512	IRC
C4	1	220µF OS-CON 10SA220M	Sanyo
C9	1	330µF OS-CON 10SA330M	Sanyo
C2	1	1µF	Monolithic ceramic Cap
C13	1	82pF	SMD Cap
C16,C17	2	0.1µF	SMD Cap
R8,R9	2	10K	SMD Resistor
C1	1	4.7µF	SMD Cap

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Table 2. Alternate Component Selection

RC5040 Alternate Suppliers of Components			
Ref Designator	Quantity	Alternate Part No.	Alternate Manufacturer
L1	1	PE-53680	Pulse Engineering
M1,M2	2	2SK1388	Fuji
		IRLZ44N	International Rectifier
DS1	1	C10T02QL	Nihon
		SR1620C	Rectron
DS2	1	MBRS140T3	Motorola
R1	1	WSL-2512	DALE
D1	1	6.2V Zener	Motorola
R3	1	100Ω	SMD Resistor

Applications Discussion

Standard Application Circuit

The circuit shown in Figure 1 along with its components and values has been designed as representative of the typical application involving the RC5040 for a Pentium Pro™ CPU. Use of the circuit in Figure 1 will deliver the performance curves shown under the Typical Operating Characteristics section of the data sheet. Many users will want to develop their own DC-DC converter solution that is uniquely tailored to a specific application requirement. In that case, the users should review the detailed information in the Design Procedure and Applications Information section of the data sheet.

Detailed Description

The RC5040 is a programmable voltage synchronous controller. When designed around the appropriate external components, it can be configured to deliver more than 12A of output current. During heavy loading conditions the RC5040 functions as a current-mode PWM step down regulator. Under light loading conditions, the regulator functions in the PFM or pulse skipping mode, thereby increasing its efficiency under light loads.

Main Control Loop

The main control loop of the regulator (see Block Diagram) contains two main blocks, the analog control block and the digital control block. The analog control block consists of signal conditioning amplifiers that feed into a set of fast comparators which provide the inputs to the digital control block. The signal conditioning block takes inputs from the IFB (current feedback) and VFB (voltage feedback) pins and then sets up two controlling signal paths. The voltage control path gains up the VFB signal and presents that signal to one of the summing amplifier inputs. The current control path takes the difference between the IFB and VFB pins and presents that signal to another input of the summing amplifier. These two signals are then summed together with the slope compensation input from the oscillator and the output is then

presented to a comparator. This comparator provides the main PWM control signal to the digital control block.

There are three other comparators in the analog control block. The first two control the thresholds of where the RC5040 goes into its pulse skipping mode during light loads and the second controls the point at which the max current comparator disables the output drive signal to the upper power MOSFET. The third comparator determines when the synchronous mode bottom side power MOSFET will be enabled and disabled.

The digital controller section is designed to take the comparator inputs along with the main clock signal from the oscillator and provide the appropriate pulses to the HIDRV and LODRV output pins that will in turn control the external power MOSFETs. This digital section was designed in high speed schottky transistor logic which allows the RC5040 to clock up to speeds greater than 1MHz. This section is responsible for providing the break-before-make timing that ensures that both external FETs will not be on at the same time.

High Current Output Drivers

The RC5040 contains two identical high current output drivers. These drivers contain high speed bipolar transistors configured in a push-pull configuration. Each output driver is capable of pumping out 1A of current in less than 100ns. Each driver's power and ground are separated from the overall chip power and ground for added switching noise immunity. The HIDRV driver has a power supply, VCCQP, which can be either derived from an external voltage source or can be boot-strapped from a flying-capacitor as is shown in Figure 1. In the boot-strapped mode, C2 is alternately charged from VCC via the schottky diode DS2 and then boosted up when M1 is turned on. This provides a VCCQP voltage equal to 2*VCC - Vds(DS2); or about 9.5V with VCC=5V. This voltage is sufficient to provide the 9V gate drive to the

external MOSFET that will be needed for achieving a low $R_{ds(on)}$. Since the low side synchronous FET is referenced to ground, there is no need to boost the gate drive voltage and its VCCP power pin can just be tied to VCC.

Internal Reference

The reference in the RC5040 is a precision band-gap type reference. Its temperature coefficient is trimmed to provide a near zero TC. Added into the reference is the output from a 4-bit DAC. The DAC is provided in accordance with the Pentium Pro™ specification that requires the DC-DC converter to be able to respond to a VID programming code. This code will change the reference voltage from 2.0V up to 3.5V in 100mV increments. For a guaranteed stable operation under all loading conditions, a 10K pull-up resistor is recommended along with a 0.1µF capacitor on the VREF output pin.

Power Good

The RC5040 Power Good function is designed in accordance with the Pentium Pro™ DC-DC converter specification and provides a constant voltage monitor on the VFB pin. The circuit takes the VFB signal and compares it to the VREF voltage and then will provide a low going interrupt signal to the CPU should the power supply voltage exceed $\pm 7\%$ of its nominal set value. The Power Good flag provides no other control function to the RC5040.

Over-Voltage Protection

The RC5040 provides a constant monitor of the output voltage for over-voltage protection. Should the voltage at the VFB pin exceed 20% of the selected program voltage, then an overvoltage condition will be assumed to exist and the RC5040 will shut down the output drive signals to the power FETs.

Oscillator

The RC5040 oscillator is designed as a fixed current capacitor charging oscillator. An external capacitor allows for maximum flexibility in choosing the associated external components for the RC5040. The oscillator frequency can be set from less than 200KHz to over 1MHz depending on the application requirements.

Design Procedure and Applications Information

Simple Step-Down Converter

Figure 3 shows a step-down DC-to-DC Converter with no feedback controller. The derivation of the basic step-down converter will serve as a basis for the design equations for the RC5040 in Figure 1. In Figure 3, the basic operation begins by closing the switch, S1. When S1 is closed the input voltage V_B is impressed across the inductor L1. The current flowing in the inductor is given by the following equation: $I_L = (V_B - V_o)T_{on}/L$; where T_{on} is the time duration for S1 to be closed. When S1 is open, the diode will conduct the inductor current and the output current will be delivered to the load according to the equation:

$I_L = V_o(T - T_{on})/L$; where $T - T_{on}$ is the time duration for S1 to be off. By solving these two equations we can arrive at the basic relationship for the output voltage of a step-down converter: $V_o = V_B(T_{on}/T)$.

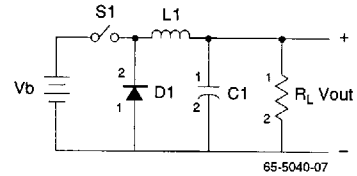


Figure 3. Simple Buck DC-DC Converter

Selecting the Inductor

The inductor is one of the most critical components to be selected in the DC-to-DC converter application. The critical parameters are inductance (L), max DC current (I_{max}), and the coil resistance (Rl). The inductor core material is a critical factor in determining the amount of current that the inductor will be able to handle. As with all engineering designs there are trade-offs for various types of inductor core materials. In general, Ferrites are popular because of their low cost, low EMI, and high frequency (>500kHz) characteristics. Molypermalloy powder (MPP) materials have good saturation characteristics and low EMI with low hysteresis losses; however they tend to be expensive and are more efficiently utilized at frequencies below 400kHz. DC winding resistance is another critical parameter. In general, the DC resistance should be kept as low as possible. The power loss in the DC resistance will degrade the efficiency of the converter by the relationship: Power Loss = $(I_o)^2 * R_l$.

The value of the inductor is a function of the switching frequency (T_{on}) and the maximum inductor current. The max inductor current can be calculated from the relationship:

$$I_{MAX} = \frac{2I_L}{F_o T_{ON} \left(\frac{V_{IN} - V_{OUT}}{V_{OUT} - V_D} \right) + 1}$$

Where : F_o is the desired clock frequency
 T_{on} is the max on time of the M1 FET
 V_d is the forward voltage of the schottky diode D1

Then the inductor value can be calculated with the relationship:

$$L = \frac{V_{IN} - V_{DSON}}{I_{MAX}} (T_{ON})$$

Where : V_{dson} is the voltage across the drain-source of the M1 FET when switched on.
 (this can be calculated by $R_{DSON} * I_{max}$)

Current-Sense Resistor

The current sense resistor will carry all of the peak current of the inductor. This current will be more than the designed for

load current. The RC5040 will begin to limit the output current to the load by turning off the top-side FET driver when the voltage across the current-sense resistor exceeds 100mV. When this happens the output voltage will temporarily go out of regulation. As the voltage across the resistor becomes larger, the top-side FET will turn off more and more until the current limit value is reached and then the RC5040 will continuously deliver the limit current at a reduced output voltage level. To insure that load transient conditions do not momentarily cause deregulation of the output voltage, a 20% margin in the limit voltage is advisable. Thus the resistor should be set by the relationship:

$$R = 100 \text{ mV}/I_{\text{peak}}$$

Where : $I_{\text{peak}} = I_{\text{max}} * 1.33$

Since the value of the sense resistor is generally in the milliohm region, care should be taken in the layout of the PCB. Trace resistance can contribute significant errors. The traces to the IFB and VFB pins of the RC5040 should be Kelvin connected to the pads of the current-sense resistor as shown in the sample layout Figure 4. To minimize the influence of noise the two traces should be run next to each other and the pins should be bypassed with a .1uF to GND as close to the device pins as possible.

Filter Capacitors

Good ripple performance and transient response are functions of the filter capacitors. Since the 5V input for a PC motherboard can be located several inches away from the DC-to-DC converter, input capacitance can play an important role in the load transient response of the RC5040. In general, the higher the input capacitance, the more charge storage is available for improving the current transfer through the top-side FET. A good rule of thumb is that for each watt of output power that you wish to deliver, there should be around 10uF of input capacitance. Low "ESR" capacitors are best suited for this application and can have an influence on the converter's efficiency. The input capacitor should be placed as close to the drain of the top-side FET as possible to reduce the effect of ringing that can be caused by large trace lengths.

The ESR rating of a capacitor is a difficult number to pin down. ESR or Equivalent Series Resistance, is defined at the resonant impedance of that capacitor. Since the capacitor is actually a complex impedance device having resistance, inductance and capacitance, it is quite natural for it to have an associated resonant frequency. As a rule, the lower the ESR, the better suited the capacitor is for use in switching power supply applications. Many capacitor manufacturers do not supply ESR data. A useful estimate of the ESR can be obtained with the following equation: $ESR = Pd/2pfC$. Where Pd is the capacitor's dissipation factor and f is the frequency of measure and C is the capacitance in farads.

With this in mind, calculating the output capacitance correctly is crucial to the performance of the DC-to-DC converter. The output capacitor determines the overall loop stability, output voltage ripple, and the transient load response. The calculation uses the following equation:

$$C (\mu F) = \frac{T_{ON} \left(\frac{(V_{IN} - V_{OUT}) I_{MAX} + I_L}{V_{OUT}} \right)}{V_r}$$

Where: Vr is the desired output ripple voltage

Schottky Diode Selection

The application circuit diagram shows two schottky diodes, DS1 and DS2. DS1 is used in parallel of M2 in order to prevent the lossy body diode in the FET from turning on. DS2 serves a dual purpose. As it is configured, it allows the VCCQP supply pin of the RC5040 to be bootstrapped up to 9V by using the bootstrap capacitor C2. When the lower FET M2 is turned on, one side of the capacitor C2 is connected to GND while the other side of the cap is being charged up through D2 to a voltage that is $V_{in} - V_d$. When the lower FET turns off and the upper one turns on, the voltage that is supplied to the VCCQP pin is $2V_{in} - V_d$. The voltage then that is applied to the gate of the FET is $VCCQP - V_{sat}$, typically around 9V. It is important in the selection of DS1 and DS2 that they have a low forward voltage drop as this directly affects the regulator efficiency. The other job that DS2 performs is that of bootstrapping VCCQP during startup. It is possible to cause the output stage to latchup if the VCCQP supply is brought up before the other VCC supplies of the RC5040. It is therefore advisable that DS2 be connected even in applications that do not utilize the bootstrapping technique for VCCQP. An alternate application could tie the VCCQP supply pin to the +12V power supply in the PC, thus eliminating the need for C2 and forcing the R_{dson} of M1 even lower by increasing its V_{gs}.

MOSFET Switches

The MOSFET switches in the RC5040 applications circuit are N-channel "logic-level" FETs. This means that they will be fully on with a V_{gs} of 4V. Many manufacturers make logic-level FETs and the trick is to choose the one with the lowest R_{dson} at the given I_{max} current level. The value of R_{dson} directly enters into the efficiency equation as a power loss. Also influencing the efficiency is the gate charge of the FET and the clock frequency of the RC5040. At higher clocking rates the amount of charge needed to be delivered to the FET is going to lower the overall efficiency. In higher current applications, the upper FET can be paralleled to provide greater current capability; however, the lower FET doesn't necessarily have to be doubled since it is on only a fraction of the time that the upper FET is on.

PRELIMINARY INFORMATION

PCB Layout and Grounding

As is the case with most analog circuitry, good layout practices are necessary to achieve the optimum in the overall performance of the DC-to-DC converter. In general, it is always a good practice to have a tight layout that attempts to minimize short low inductance wiring to the RC5040.

The use of multilayer PCB is recommended. In particular, it is recommended to have a continuous ground plane beneath the circuit, 2oz copper would be preferred in high current applications. As was stated previously, the current-sense

resistor, R1, should be located as close to the RC5040 as possible and the IFB and VFB traces should be Kelvin connected to the pads of R1. To minimize switching losses and noise, place M1, M2, L and DS2 as close together as possible. Also try to keep the HIDRV and LODRV gate drive signal traces as short as possible. It is recommended that the noisy switching part of the circuit be kept away from the low current pins on the chip such as IFB, VFB, VREF, and CEXT. Keep the 0.1uF bypass capacitors as close to the chip pins as possible. All of the ground pins should be connected to the ground plane directly under the chip. A sample layout is provided in Figure 4.

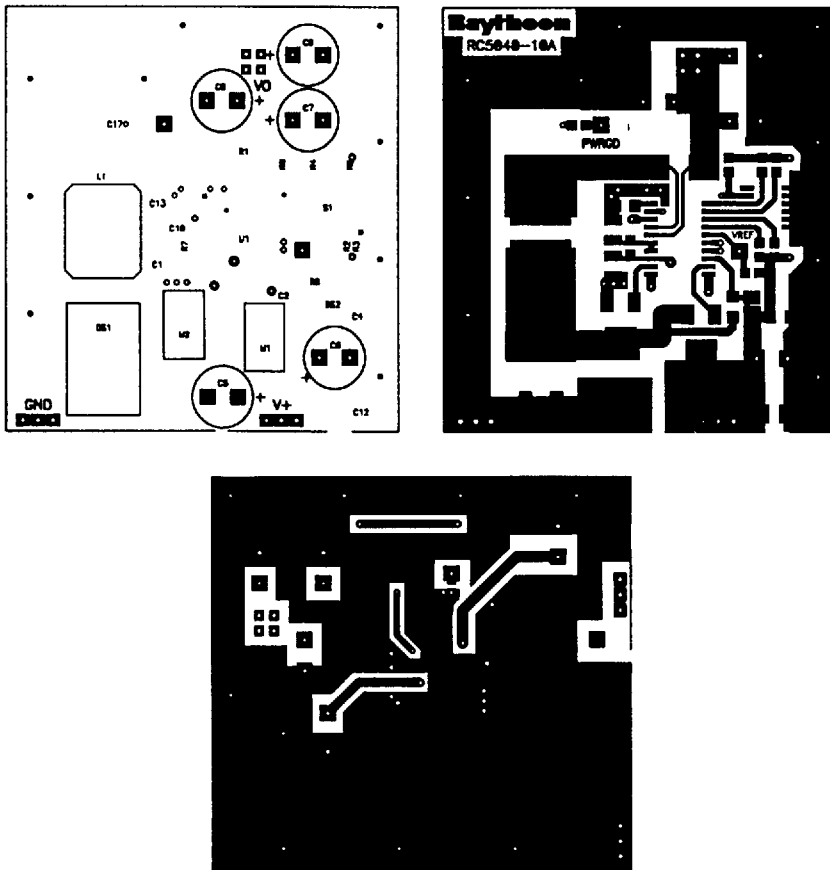


Figure 4. Sample PCB Layout

Ordering Information

Product Number	Package	θJA
RC5040M	20 pin SOIC	80°C/W

Preliminary Information