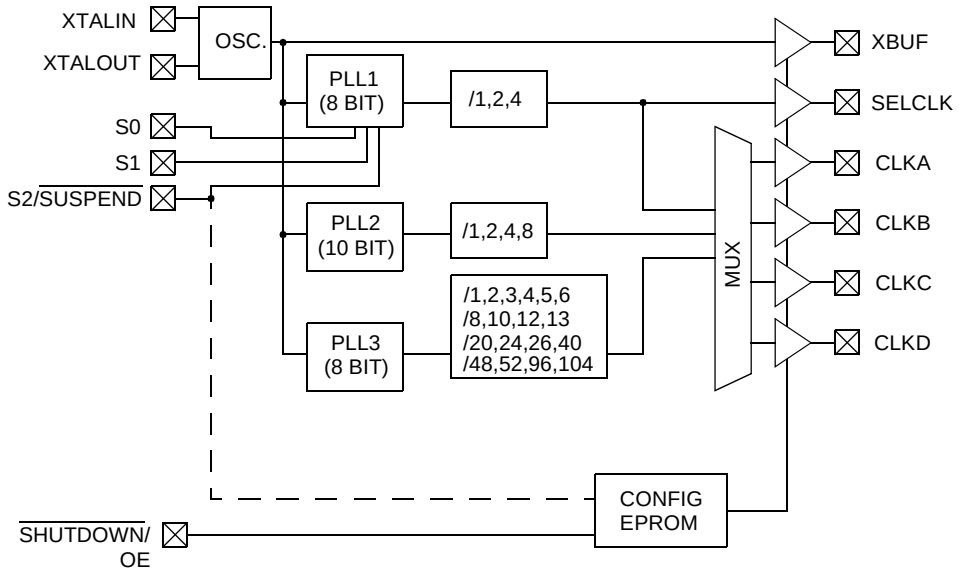
CY2081WAF

Three-PLL General Purpose EPROM Programmable Clock Generator Die

Features	Benefits
• **Three integrated phase-locked loops**	Provides all necessary system clocks in a single package
• **EPROM programmability**	Easy customization and fast turnaround time
• **Low-skew, low-jitter, high-accuracy outputs**	Meets critical timing requirements in complex system designs
• **Power management options (Shutdown, OE, Suspend)**	Supports low power applications
• **Frequency select option**	Enables design flexibility and margin testing
• **Smooth slewing on SELCLK**	Allows downstream PLLs to stay locked on SELCLK output
• **3.3V or 5V operation**	Enables application compatibility

Part Number	Outputs	Input Frequency Range	Output Frequency Range	Specifics
CY2081WAF	6	10 MHz–25 MHz (external crystal)	76.923 kHz–100 MHz (5V) 76.923 kHz–80 MHz (3.3V)	Commercial Temperature

Logic Block Diagram



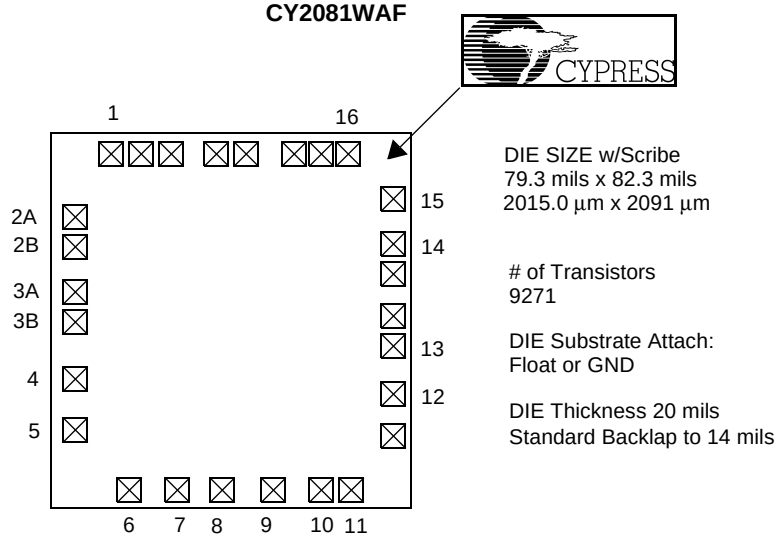
Overview

The CY2081WAF is a standard CY2081 EPROM Programmable clock in die form. The die is intended to be used as a clock generator integrated with a crystal in a single package. This integration can dramatically lower the WIP and Lead Time for Oscillator manufacturing.

All Performance Specifications are based on a CY2081 in a 16-pin SOIC package per Cypress Specification. When the CY2081WAF is placed in packages as commonly used in the oscillator market performance will usually meet or exceed the specifications given in this datasheet. However, Cypress cannot guarantee performance in these packages. Each company that uses Cypress die should test and characterize the performance of their final product.

PAD Configurations

CY2081WAF



Pin Summary

Name	PAD Number	Function	Programming Function
CLKC	1	Configurable clock output C	Serial Data Out
V_{DD}	2A, 2B	Voltage supply	V_{pp}, High Voltage Pin
GND	3A, 3B	Ground	Ground
XTALIN[1]	4	Reference crystal input	Testmode Control
XTALOUT[1]	5	Reference crystal feedback	NC
XBUF	6	Buffered reference clock output	Serial Data Out
CLKD	7	Configurable clock output D	NC
SELCLK[4]	8	SELCLK frequency clock output	NC
CLKB	9	Configurable clock output B	NC
CLKA	10	Configurable clock output A	NC
GND	11	Ground	NC
S0	12	SELCLK select input, bit 0; On Die 50K Pull Up Resistor	Serial Data In
S1	13	SELCLK select input, bit 1; On Die 50K Pull Up Resistor	Shift Enable
Vdd	14	Core Vdd Supply	Vdd Supply
S2/$\overline{\text{SUSPEND}}$	15	SELCLK select input, bit 2. Optionally enables suspend feature when LOW [2] On Die 50K Pull Up Resistor	Program Enable
$\overline{\text{SHUTDOWN}}$/OE	16	Places outputs in three-state[3] condition and shuts down chip when LOW. Optionally, only places outputs in three-state[3] condition and does not shut down chip when LOW. On Die 50K Pull Up Resistor	Serial Data Clock

Notes:
1. For best accuracy, use a parallel-resonant crystal, $C_{LOAD} \approx 17$ pF or 18 pF.
2. Please refer to application note “Understanding the CY2291, CY2292 and CY2295” for more information.
3. The CY2081WAF has weak pull-downs on all outputs. Hence, when a three-state condition is forced on the outputs, the output pins are pulled LOW.
4. SELCLK is shown as CPUCLK on the original CY2292 data sheet and programming guide.

Operation

The CY2081WAF is a third-generation family of clock generators. The part can be configured for either 5V or 3.3V operation. The internal ROM tables use EPROM technology, allowing full customization of output frequencies. The reference oscillator has been designed for 10-MHz to 25-MHz crystals, providing additional flexibility. No external components are required with this crystal.

Output Configuration

The CY2081WAF has four independent frequency sources on chip. These are the reference oscillator and three Phase-Locked Loops (PLLs). Each PLL has a specific function. The PLL3 offers the most output frequency divider options. PLL1 is controlled by the select inputs (S0–S2) to provide eight user-selectable frequencies with smooth slewing between frequencies. PLL2 provides the most accurate clock. It is often used for miscellaneous frequencies not provided by the other frequency sources.

All configurations are EPROM programmable, providing short sample and production lead times. Please refer to the application note “Understanding the CY2291, CY2292 and CY2295” for information on configuring the part.

Power Saving Features

The $\overline{\text{SHUTDOWN}}$/OE input three-states the outputs when pulled LOW. If system shutdown is enabled (the default), a LOW on this pin also shuts off the PLLs, counters, the reference oscillator, and all other active components. The resulting current on the V_{DD} pins will be less than 50 μA and is typically 10 μA. After leaving shutdown mode, the PLLs will have to re-lock. All outputs have a weak pull-down so that the outputs do not float when three-stated.[3]

The S2/$\overline{\text{SUSPEND}}$ input can be configured to shut down a customizable set of outputs and/or PLLs, when LOW. All PLLs and any of the outputs can be shut off in nearly any combination. The only limitation is that if a PLL is shut off, all outputs derived from it must also be shut off. Suspending a PLL shuts off all associated logic, while suspending an output simply forces a three-state condition.[2]

PLL1 can slew (transition) smoothly between 8 MHz and the maximum output frequency (100 MHz at 5V; 80 MHz at 3.3V).

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

Storage Temperature ..... –65°C to +150°C

Max. Soldering Temperature (10 sec) ..... 260°C

Junction Temperature ..... 150°C

Package Power Dissipation ..... 750 mW

Static Discharge Voltage ..... >2000V (per MIL-STD-883, Method 3015)

Operating Conditions[5]

Parameter	Description	Part Numbers	Min.	Max.	Unit
V_{DD}	Supply Voltage, 5.0V (3.3V) operation	All	4.5 (3.0)	5.5 (3.6)	V
T_A	Operating Temperature, Ambient	All	0	+70	°C
C_{LOAD}	Max. Load Capacitance 5.0V (3.3V) Operation	All	18	25 (15)	pF
f_{REF}	Reference Frequency	All	10.0	25.0	MHz

Electrical Characteristics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{OH}[6]	HIGH-Level Output Voltage	I_{OH} = 4.0 mA	2.4			V
V_{OL}[6]	LOW-Level Output Voltage	I_{OL} = 4.0 mA			0.4	V
V_{IH}	HIGH-Level Input Voltage[7]	Except crystal pins	2.0			V
V_{IL}	LOW-Level Input Voltage[7]	Except crystal pins			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}–0.5V		< 1	10	µA
I_{IL}	Input LOW Current	V_{IN} = +0.5V		< 1	10	µA
I_{OZ}	Output Leakage Current	Three-state outputs			250	µA
I_{DD}	V_{DD} Supply Current[8]	V_{DD} = V_{DD} max., 5V (3.3V) operation		75(50)	100(65)	mA
I_{DDS}	V_{DD} Power Supply Current in Shutdown Mode[8]	Shutdown active		10	50	µA

Notes:

5. Electrical parameters are guaranteed with these operating conditions.
6. All outputs swing rail to rail
7. Xtal Inputs have CMOS thresholds
8. Load = Max., V_{IN} = 0V or V_{DD}, Typical (–104) configuration, SELCLK = 66 MHz. Other configurations will vary. Power can be approximated by the following formula (multiply by 0.65 for 3V operation): $I_{DD}=10+0.06\bullet(F_{PLL1}+F_{PLL2}+2\bullet F_{PLL3})+0.27\bullet(F_{SELCLK}+F_{CLKB}+F_{CLKC}+F_{CLKD}+F_{CLKA}+F_{XBUF})$.

Switching Characteristics[9]

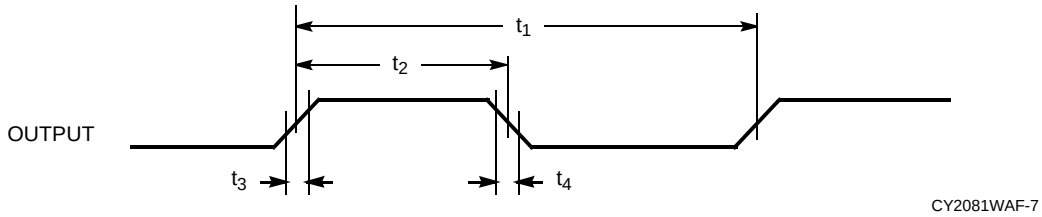
Parameter	Name	Description		Min.	Typ.	Max.	Unit
t_1	Output Period	Clock output range, 5V operation	All	10 (100 MHz)		13000 (76.923 kHz)	ns
t_1	Output Period	Clock output range, 3.3V operation	All	12.5 (80 MHz)		13000 (76.923 kHz)	ns
	Output Duty Cycle[10]	Duty cycle for outputs, defined as $t_2 \div t_1$[11] $f_{OUT} \geq 66$ MHZ		40%	50%	60%	
		Duty cycle for outputs, defined as $t_2 \div t_1$[11] $f_{OUT} < 66$ MHZ		45%	50%	55%	
t_3	Rise Time	Output clock rise time[12]			3	5	ns
t_4	Fall Time	Output clock fall time[12]			2.5	4	ns
t_5	Output Disable Time	Time for output to enter three-state mode after SHUTDOWN/OE goes LOW			10	15	ns
t_6	Output Enable Time	Time for output to leave three-state mode after SHUTDOWN/OE goes HIGH			10	15	ns
t_7	Skew	Skew delay between any identical or related outputs[2, 11]			< 0.25	0.5	ns
t_8	PLL1 Slew	Frequency transition rate		1.0		20.0	MHz/ ms
t_{9A}	Clock Jitter[13]	Peak-to-peak period jitter (t_{9A} max. – t_{9A} min.),% of clock period ($f_{OUT} \leq 4$ MHz)			<0.5	1	%
t_{9B}	Clock Jitter[13]	Peak-to-peak period jitter (t_{9B} max. – t_{9B} min.) (4 MHz $\leq f_{OUT} \leq$ 16 MHz)			<0.7	1	ns
t_{9C}	Clock Jitter[13]	Peak-to-peak period jitter (16 MHz < $f_{OUT} \leq$ 50 MHz)			<400	500	ps
t_{9D}	Clock Jitter[13]	Peak-to-peak period jitter ($f_{OUT} > 50$ MHz)			<250	350	ps
t_{10A}	Lock Time for PLL1	Lock Time from Power-up			<25	50	ms
t_{10B}	Lock Time for PLL2 and PLL3	Lock Time from Power-up			<0.25	1	ms
	Slew Limits	PLL1 Slew Limits	All	8		100 (5V) 80 (3.3V)	MHz

Notes:

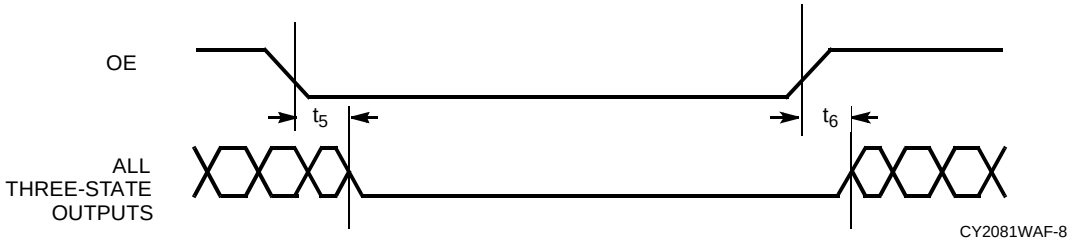
9. Guaranteed by design and characterization, not 100% tested in production.
10. XBUF duty cycle depends on XTALIN duty cycle.
11. Measured at 1.4V.
12. Measured between 0.4V and 2.4V.
13. Jitter varies with configuration. All standard configurations sample tested at the factory conform to this limit. For more information on jitter, please refer to the application note: “Jitter in PLL-Based Systems.

Switching Waveforms

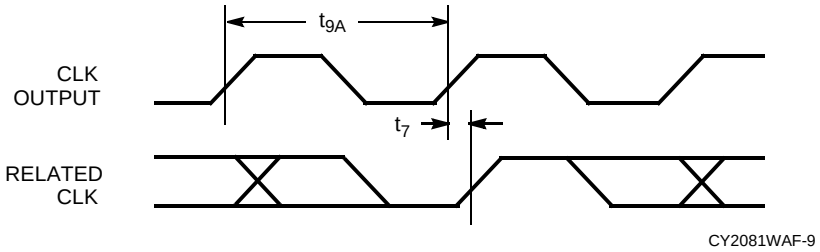
All Outputs, Duty Cycle and Rise/Fall Time



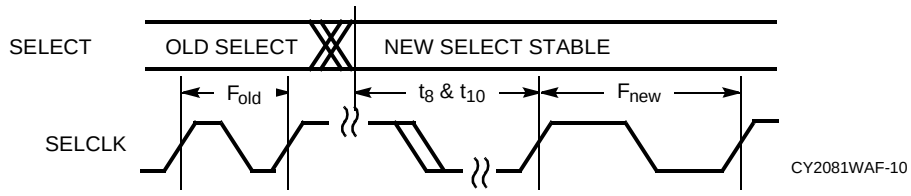
Output Three-State Timing[3]



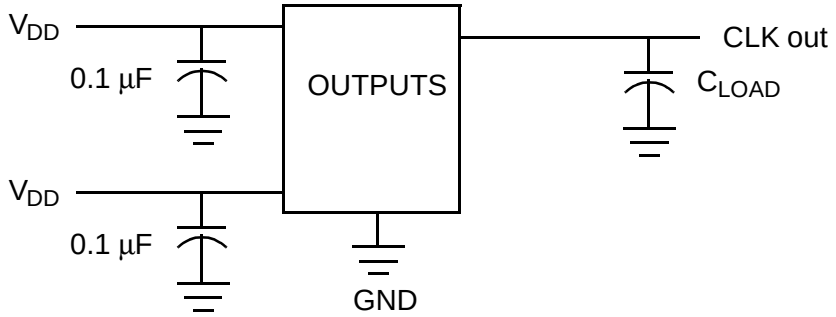
CLK Outputs Jitter and Skew



SELCLK Frequency Change



Test Circuit



CY2081WAF

Ordering Information

Ordering Code	Operating Range	Operating Voltage
CY2081WAF	Commercial	3.3 or 5.0V

The CY2081 wafer yields approximately 3000 die. Therefore, the CY2081WAF must be purchased in multiples of 3000. After sorting the wafer, a certain number of die will be inked mark as bad. The wafer will then be backlapped and shipped. Only the good die will be billed. Assume 3000 good die per wafer for inventory control purposes.

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REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110501	02/01/02	SZV	Change from Spec number: 38-00959 to 38-07236