micross components
transforming specialty electronics

SRAM
AS5LC512K8

512K x 8 SRAM
3.3 VOLT HIGH SPEED SRAM with CENTER POWER PINOUT

AVAILABLE AS MILITARY SPECIFICATIONS
•MIL-STD-883 for Ceramic
•Extended Temperature Plastic (COTS)

FEATURES
- Ultra High Speed Asynchronous Operation
- Fully Static, No Clocks
- Multiple center power and ground pins for improved noise immunity
- Easy memory expansion with CE\ and OE\ options
- All inputs and outputs are TTL-compatible
- Single +3.3V Power Supply +/- 0.3V
- Data Retention Functionality Testing
- Cost Efficient Plastic Packaging
- Extended Testing Over -55ºC to +125ºC for plastics
- RoHS Compliant Options Available

OPTIONS — MARKING

- Timing

10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25

- Operating Temperature Ranges

883C (-55ºC to +125ºC)	/883C
Military (-55ºC to +125ºC)	/XT
Industrial (-40ºC to +85ºC)	/IT

- Package(s)

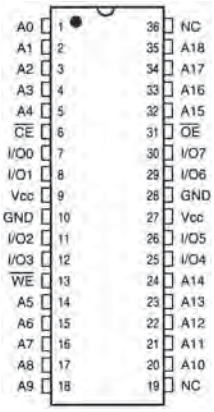
Ceramic Flatpack	F	No. 307
Ceramic LCC	EC	No. 210
Plastic SOJ (400 mils wide)	DJ	

- 2V data retention/low power* — L

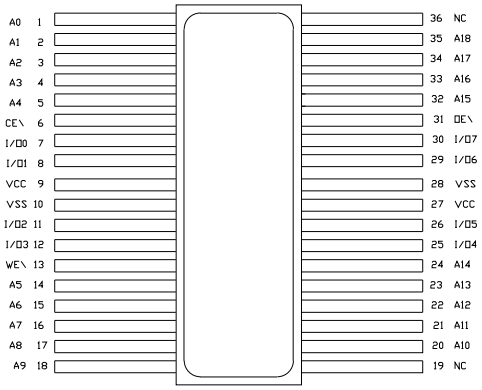
For more products and information please visit our web site at
www.micross.com

PIN ASSIGNMENT
(Top View)

36-Pin PSOJ (DJ)
36-Pin CLCC (EC)



36-Pin Flat Pack (F)



GENERAL DESCRIPTION

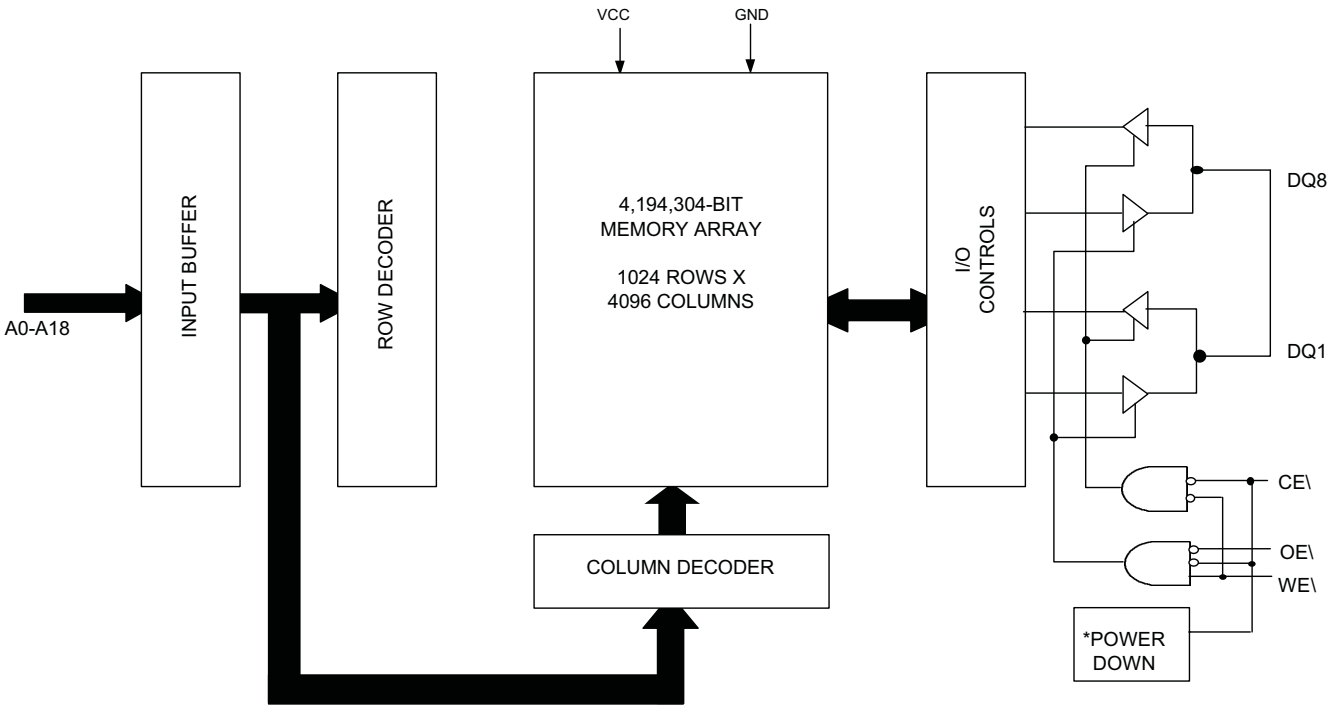
The AS5LC512K8 is a 3.3V high speed SRAM. It offers flexibility in high-speed memory applications, with chip enable (CE\) and output enable (OE\) capabilities. These features can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable (WE\) and CE\ inputs are both LOW. Reading is accomplished when WE\ remains HIGH and CE\ and OE\ go LOW.

As a option, the device can be supplied offering a reduced power standby mode, allowing system designers to meet low standby power requirements. This device operates from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible.

The AS5LC512K8DJ offers the convenience and reliability of the AS5LC512K8 SRAM and has the cost advantage of a plastic encapsulation. TSOPII with copper lead frames offers superior thermal performance.

FUNCTIONAL BLOCK DIAGRAM



**On the low voltage Data Retention option.*

TRUTH TABLE

MODE	OE\	CE\	WE\	I/O	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

X = Don't Care

PIN FUNCTIONS

A0 - A18	Address Inputs
WE\	Write Enable
CE\	Chip Enable
OE\	Output Enable
I/O_0 - I/O_7	Data Inputs/Outputs
V_{CC}	Power
V_{SS}	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss
Vcc .....-.5V to 4.0V
Storage Temperature .....-65°C to +150°C
Short Circuit Output Current (per I/O)….....20mA
Voltage on any Pin Relative to Vss.....-.5V to 4.6V
Maximum Junction Temperature**.....+150°C
Power Dissipation 1W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

** Junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow, and humidity.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-55^oC \le T_A \le +125^oC$ & $-40^oC \le T_A \le +85^oC$; Vcc = 3.3V ±0.3%)

			MAX						
DESCRIPTION	CONDITIONS	SYM	-10	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	CE\ ≤ V_{IL}; Vcc = MAX f = MAX = $1/t_{RC}$ Outputs Open	I_{CCSP}	90	80	70	60	55	mA	3, 2
	"L" Version Only	I_{CCLP}	-	60	50	40	35	mA	
Power Supply Current: Standby	CE\ ≥ V_{IH}, All other inputs ≤ V_{IL}, Vcc = MAX, f = 0, Outputs Open	I_{SBTSP}	30	20	20	20	20	mA	
	"L" Version Only	I_{SBTLP}	-	15	15	15	15	mA	
	CE\ ≥ Vcc -0.2V; Vcc = MAX V_{IN}≤Vss +0.2V or V_{IN}≥Vcc -0.2V; f = 0	I_{SBCSP}	20	15	15	15	15	mA	
	"L" Version Only	I_{SBCLP}	-	9	9	9	9	mA	

DESCRIPTION	CONDITIONS	SYM	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc +0.3	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-2	2	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-2	2	µA	
Output High Voltage	I_{OH} = -4.0 mA	V_{OH}	2.4	---	V	1
Output Low Voltage	I_{OL} = 8 mA	V_{OL}	---	0.5	V	1

CAPACITANCE

PARAMETER	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz V_{IN} = 0	C_I	8	pF	4
Output Capactiance		Co	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($-55^oC \leq T_A \leq +125^oC$ or -40^oC to $+85^oC$; Vcc = 3.3V $\pm$0.3%)

DESCRIPTION	SYM	-10		-12		-15		-20		-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ CYCLE													
Read Cycle Time	t_{RC}	10		12		15		20		25		ns	
Address Access Time	t_{AA}		10		12		15		20		25	ns	
Chip Enable Access Time	t_{ACE}		10		12		15		20		25	ns	
Output Hold From Address Change	t_{OH}	2		2		2		2		2		ns	
Chip Enable to Output in Low-Z	t_{LZCE}	2		2		2		2		2		ns	4, 6, 7
Chip Disable to Output in High-Z	t_{HZCE}		4		6		7		8		9	ns	4, 6, 7
Output Enable Acess Time	t_{AOE}		4.5		6		7		8		9	ns	
Output Enable to Output in Low-Z	t_{LZOE}	0		0		0		0		0		ns	4, 6, 7
Output Disable to Output in High-Z	t_{HZOE}		4		6		7		8		9	ns	4, 6, 7
WRITE CYCLE													
WRITE Cycle Time	t_{WC}	10		12		15		20		25		ns	
Chip Enable to End of Write	t_{CW}	8		8		10		12		13		ns	
Address Valid to End of Write	t_{AW}	8		8		10		12		13		ns	
Address Setup Time	t_{AS}	0		0		0		0		0		ns	
Address Hold From End of Write	t_{AH}	0		0		0		0		0		ns	
WRITE Pulse Width	t_{WP}	8		10		12		15		15		ns	
Data Setup Time	t_{DS}	6		6		7		8		8		ns	
Data Hold Time	t_{DH}	1		1		1		1		1		ns	
Write Disable to Output in Low-Z	t_{LZWE}	2		2		2		2		2		ns	4, 6, 7
Write Enable to Output in High-Z	t_{HZWE}		5		5		6		7		7	ns	4, 6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

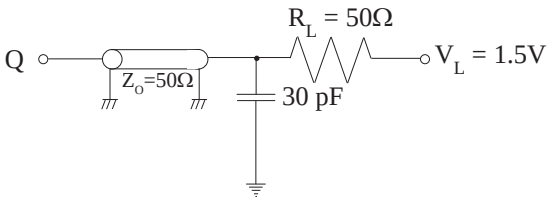


Fig. 1 Output Load Equivalent

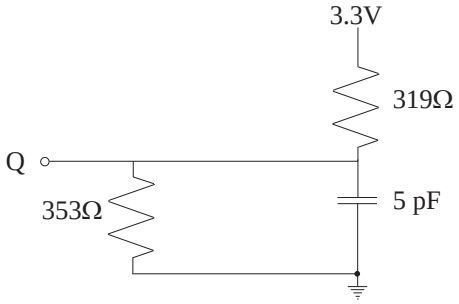


Fig. 2 Output Load Equivalent

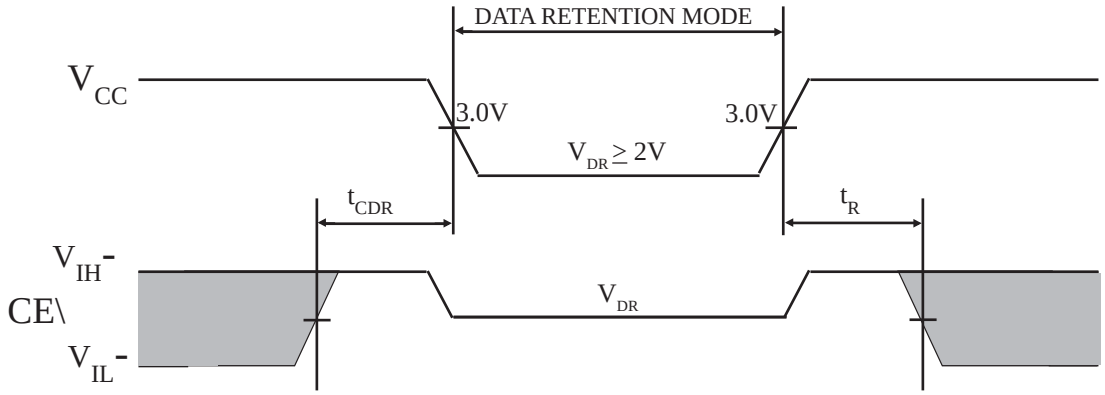
NOTES

1. All voltages referenced to V_{SS} (GND).
2. I_{CC} limit shown is for absolute worst case switching of ADDR, ADDR\, ADDR, etc.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is guaranteed but not tested.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ᵗLZCE, ᵗLZWE, ᵗLZOE, ᵗHZCE, ᵗHZOE and ᵗHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ᵗHZCE is less than ᵗLZCE, and ᵗHZWE is less than ᵗLZWE.
8. WE\ is HIGH for READ cycle.
9. Device is continuously selected. Chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ᵗRC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Output enable (OE\) is inactive (HIGH).
14. Output enable (OE\) is active (LOW).
15. ASI does not warrant functionality nor reliability of any product in which the junction temperature exceeds 150°C. Care should be taken to limit power to acceptable levels.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

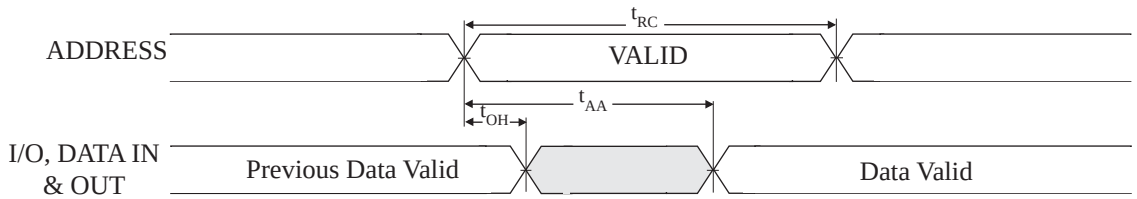
DESCRIPTION	CONDITIONS	SYM	MIN	MAX	UNITS	NOTES
Vcc for Retention Data	CE\ > V_{CC} -0.2V V_{IN} > V_{CC} -0.2 or 0.2V	V_{DR}	2		V	
Data Retention Current	Vcc = 2.0V	I_{CCDR}		6.5	mA	
Chip Deselect to Data		t_{CDR}	0		ns	4
Operation Recovery Time		t_R	20		ms	4, 11

LOW V_{CC} DATA RETENTION WAVEFORM



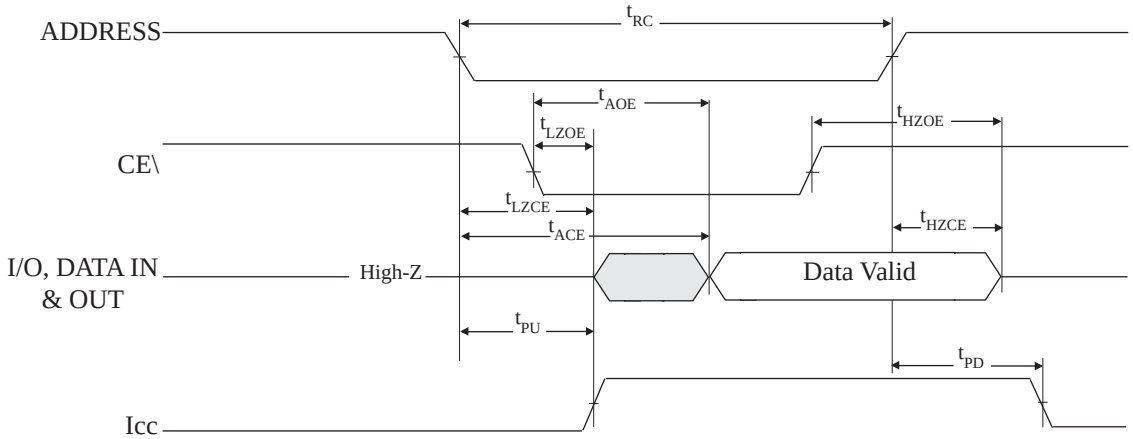
READ CYCLE NO. 1[1, 2]

(Address Controlled, CE\ = OE\ = V_{IL}, WE\ = V_{IH})



READ CYCLE NO. 2

(WE\ = V_{IH})



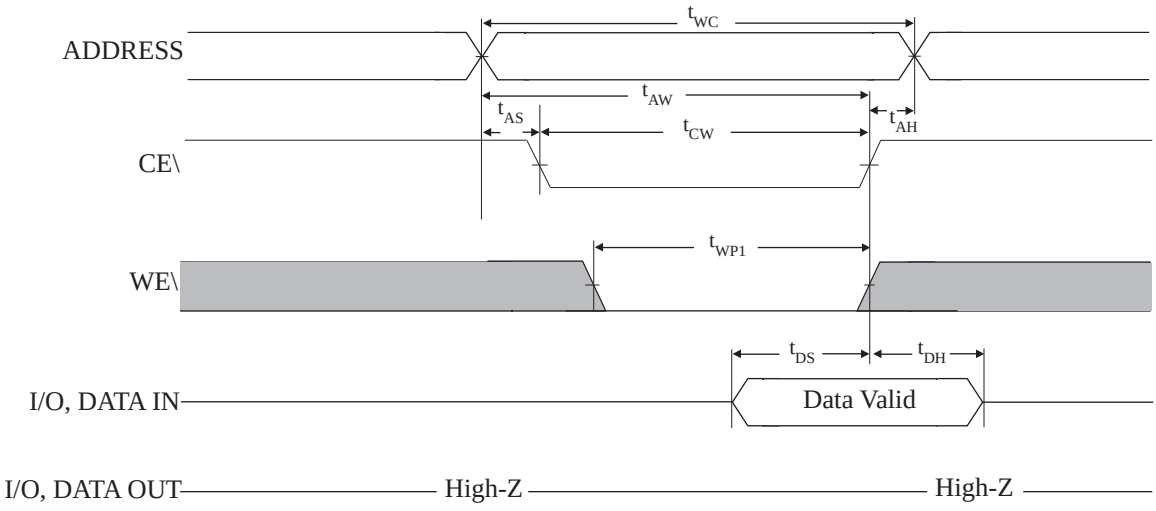
NOTES:

1. WE\ is HIGH for READ cycle.
2. Device is continuously selected. Chip enables and output enables are held in their active state.

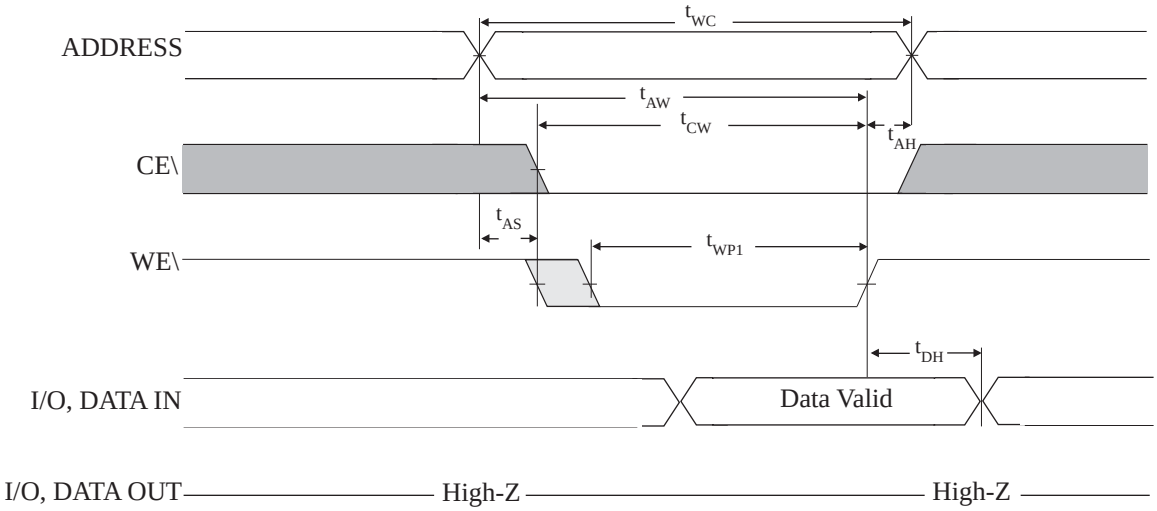
Don't Care

Undefined

WRITE CYCLE NO. 1[1]
(CE Controlled)

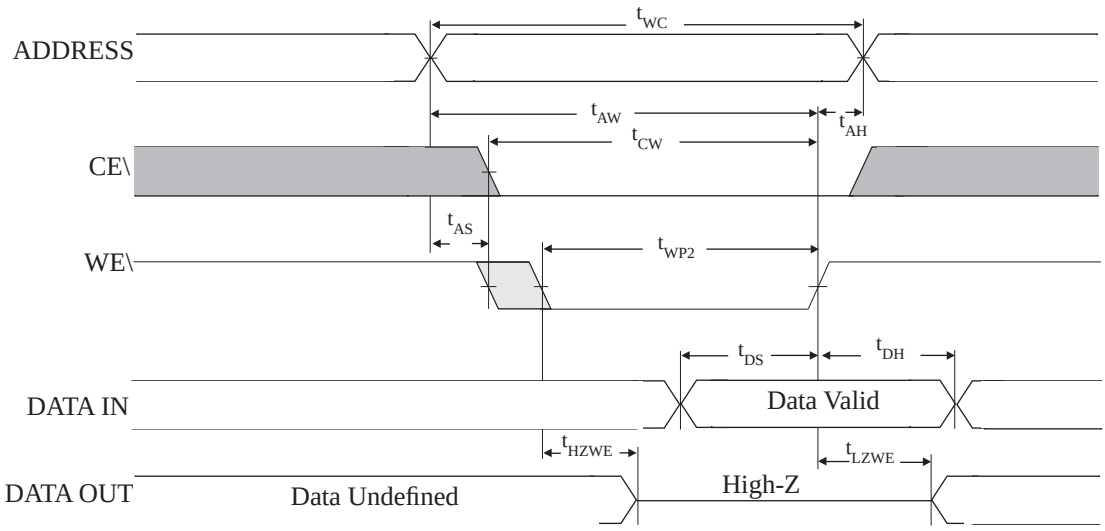


WRITE CYCLE NO. 2[1, 2]
(Write Enabled Controlled)



NOTES:
1. Chip enable and write enable can initiate and terminate a WRITE cycle.
2. Output enable (OE\) is inactive (HIGH).

WRITE CYCLE NO. 3[1, 2, 3]
(WE Controlled)

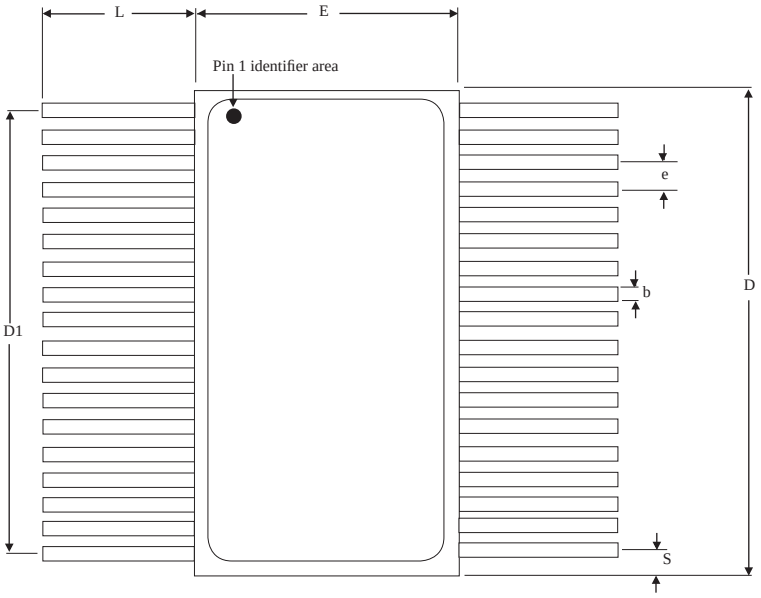


NOTES:

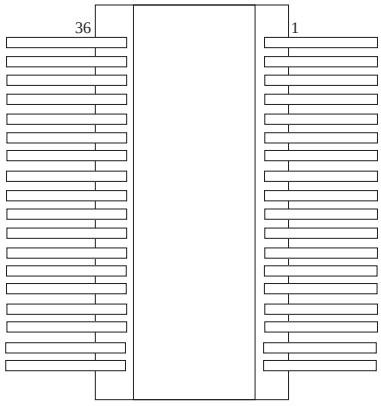
1. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, and t_{HZWE} is less than t_{LZWE}.
2. Chip enable and write enable can initiate and terminate a WRITE cycle.
3. Output enable (OE\) is active (LOW).

MECHANICAL DEFINITIONS*

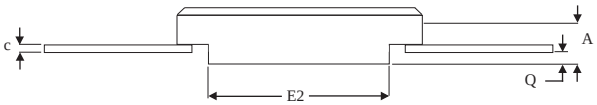
Micross Case #307 (Package Designator F)



Top View



Bottom View

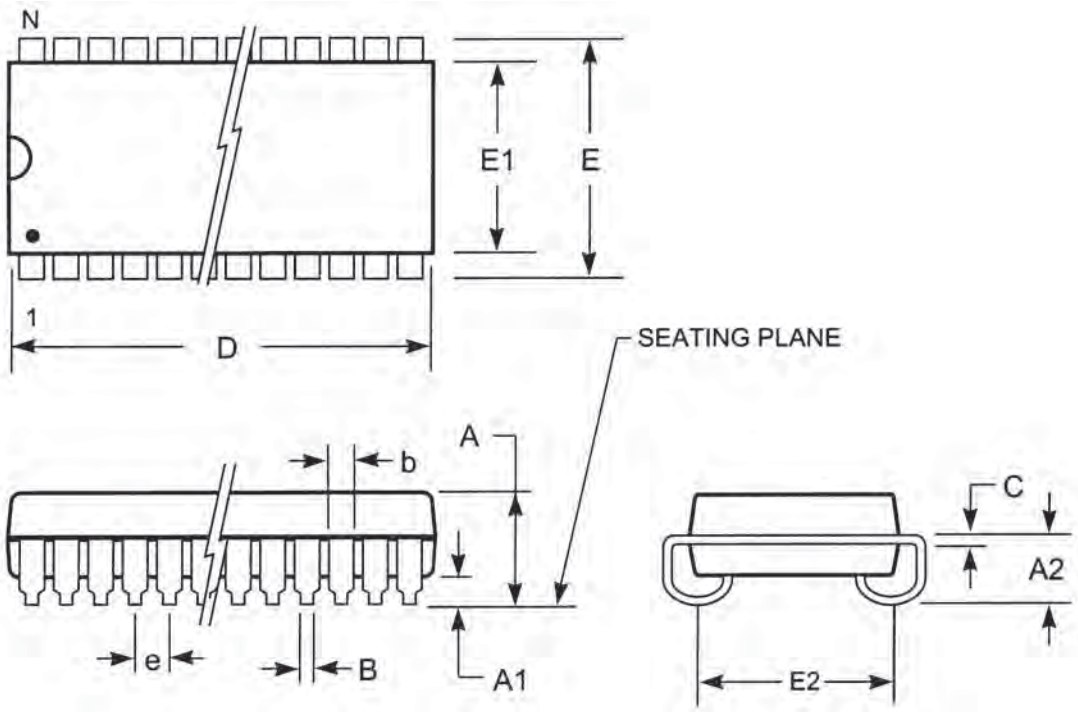


SYMBOL	MICROSS SPECIFICATIONS	
	MIN	MAX
A	0.096	0.125
b	0.015	0.022
c	0.003	0.009
D	0.910	0.930
D1	0.840	0.860
E	0.505	0.515
E2	0.385	0.397
e	0.050 BSC	
L	0.250	0.370
Q	0.020	0.045

All measurements are in inches.

MECHANICAL DEFINITIONS*

Package Designator DJ

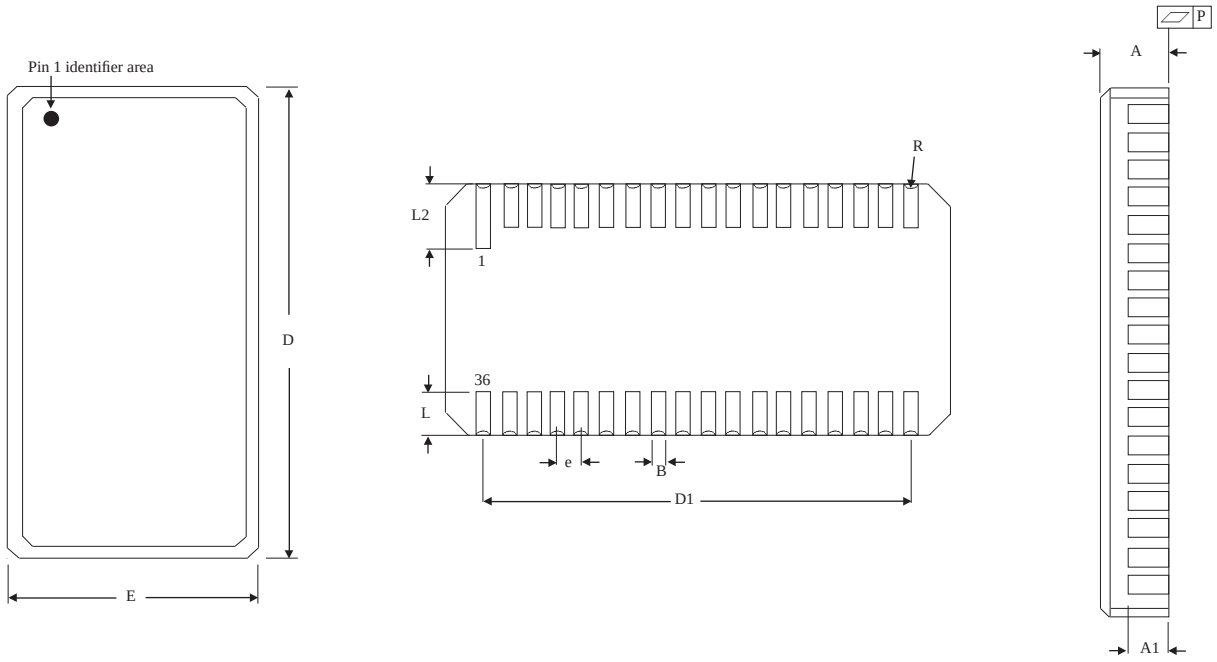


SYMBOL	MICROSS SPECIFICATIONS	
	MIN	MAX
A	0.128	0.148
A1	0.025	---
A2	0.082	---
B	0.015	0.020
b	0.026	0.032
C	0.007	0.013
D	0.920	0.930
E	0.435	0.445
E1	0.395	0.405
E2	0.370 BSC	
e	0.050 BSC	

All measurements are in inches.

MECHANICAL DEFINITIONS*

Micross Case #210 (Package Designator EC)



SYMBOL	MICROSS SPECIFICATIONS	
	MIN	MAX
A	0.080	0.100
A1	0.054	0.066
B	0.022	0.028
D	0.910	0.930
D1	0.840	0.860
E	0.445	0.460
e	0.050 BSC	
L	0.100 TYP	
L2	0.115	0.135
P	---	0.006
R	0.009 TYP	

All measurements are in inches.

ORDERING INFORMATION

36-Pin Ceramic Flat Pack
EXAMPLE: AS5LC512K8F-12L/XT

Device Number	Package Type	Speed ns	Options**	Process
AS5LC512K8	F	-10	L	/*
AS5LC512K8	F	-12	L	/*
AS5LC512K8	F	-15	L	/*
AS5LC512K8	F	-25	L	/*

36-Pin Plastic PSOJ
EXAMPLE: AS5LC512K8DJ-20L/IT

Device Number	Package Type	Speed ns	Options**	Process
AS5LC512K8	DJ	-12	L	/*
AS5LC512K8	DJ	-15	L	/*
AS5LC512K8	DJ	-20	L	/*
AS5LC512K8	DJ	-25	L	/*

36-Pin Ceramic CLCC
EXAMPLE: AS5LC512K8EC-15L/IT

Device Number	Package Type	Speed ns	Options**	Process
AS5LC512K8	EC	-12	L	/*
AS5LC512K8	EC	-15	L	/*
AS5LC512K8	EC	-20	L	/*
AS5LC512K8	EC	-25	L	/*

*AVAILABLE PROCESSES

IT = Industrial Temperature Range -40°C to +85°C
XT = Extended Temperature Range -55°C to +125°C
883C = Full Military Processing[1] -55°C to +125°C

**OPTIONS DEFINITIONS

L = 2V Data Retention / Low Power

NOTES: 1. 883C process available with ceramic packaging only.

DOCUMENT TITLE

512K x 8 SRAM 3.3 VOLT HIGH SPEED SRAM with CENTER POWER PINOUT

Rev #	History	Release Date	Status
2.1	Pg 1: Changed 0.3% to 0.3V	August 2009	Release
2.2	Updated Micross Information	January 2010	Release
2.3	Expanded package offering to include Copper Lead Frames and RoHS Compliancy, added -10 speed option, Reduced C_L from 9pF to 8pF, corrected t_{HZWE} from min's to max's on page 4, corrected 4.5V reference points on data retention waveform to 3.0V, pg. 6	March 2011	Release
2.4	Removed Cu-lead frame option	October 2013	Release