November 1992
Edition 2.1A

FUJITSU

DATA SHEET

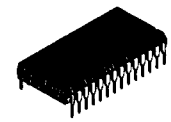
MB8464R-70LL, -10LL
CMOS 64K Low Power SRAM with Data Retention

The Fujitsu MB8464R is an 8,192–word x 8–bit static random access memory fabricated with a CMOS silicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible when using +5V power supply. The MB8464R operates with both +5V and +3V power supplies.

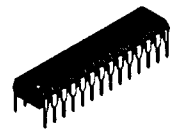
The MB8464R is ideally suited for use in microprocesser systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.

Parameter	LL-version	
	-70LL	-10LL
Access Time (5V Operation)	70 ns	100 ns
Access Time (3V Operation)	200 ns	
Standby Power Dissipation	0.11 mW	
Data Retention Current	10 µA	
Data Retention Current (T_A = 0°C to +40°C)	1 µA	

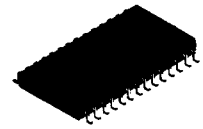
- Organization:
  8,192 words x 8 bits
- Operating supply voltage:
  +5V power supply ±10% tolerance
  +3V power supply +20%, –10% tolerance
- Data retention voltage: 2.0V minimum
- Static operation: no clock required
- Package and ordering information:
  - 28-pin plastic DIP (600 mil), order as MB8464R-xxLLP
  - 28-pin plastic Skinny DIP (300 mil), order as MB8464R-xxLLPSK
  - 28-pin plastic SOP, order as MB8464R-xxLLPF
  - 28-pin plastic TSOP (normal bend), order as MB8464R-xxLLPFTN
  - 28-pin plastic TSOP (reverse bend), order as MB8464R-xxLLPFTR



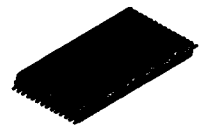
Plastic DIP
(DIP-28P-M02)

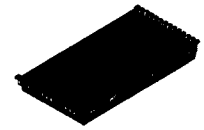


Plastic Skinny DIP
(DIP-28P-M04)



Plastic SOP
(FPT-28P-M02)



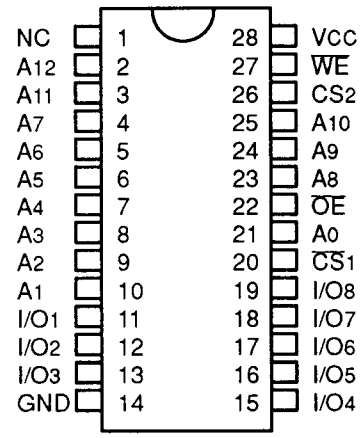


Plastic TSOP

(normal leads) **(reverse bend)**
(FPT-28P-M03) **(FPT-28P-M04)**

Pin Assignment

TOP VIEW



DIP and SOP

ABSOLUTE MAXIMUM RATINGS

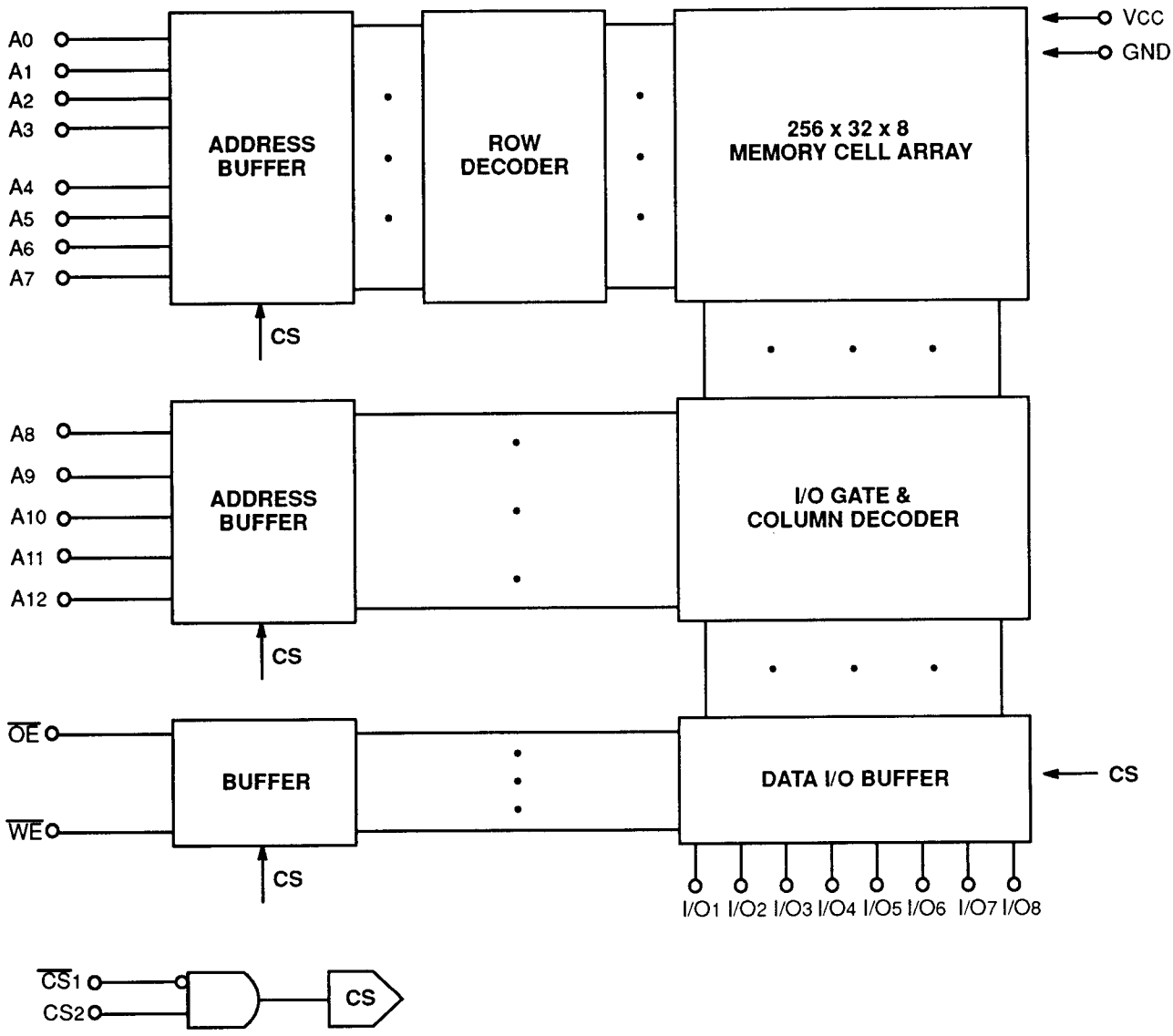
Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–0.5 to V_{CC} +0.5	V
Output Voltage	$V_{I/O}$	–0.5 to V_{CC} +0.5	V
Temperature Under Bias	T_{BIAS}	–10 to +85	°C
Storage Temperature	T_{STG}	–45 to +125	°C

— Note —

Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MB8464R BLOCK DIAGRAM



CAPACITANCE (TA= 25° C, f = 1MHZ)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance (VI/O = 0V)	CI/O			8	pF
Input Capacitance (VIN = 0V)	CIN			7	pF

PIN DESCRIPTION

Symbol	Pin name	Symbol	Pin name
A0 to A12	Address Input	$\overline{WE}$	Write Enable
I/O1 to I/O8	Data Input/Output	VCC	Power Supply (5V±10%, or 3V+20%, −10%)
$\overline{OE}$	Output Enable	GND	Ground
$\overline{CS1}$	Chip Select 1	NC	No Connection
CS2	Chip Select 2		

FUNCTION TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	X	Not Selected	ISB	High–Z
X	L	X	X	Not Selected	ISB	High–Z
L	H	H	H	DOUT Disable	ICC	High–Z
L	H	L	H	Read	ICC	DOUT
L	H	X	L	Write	ICC	DIN

Legend: H: High Level, L: Low Level, X: Don't Care

RECOMMENDED OPERATING CONDITION

(Referenced to GND)

Parameter	Symbol	5V Operation			3V Operation			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	VCC	4.5	5.0	5.5	2.7	3.0	3.6	V
Ambient Temperature	TA	0		70	0		70	°C

DC CHARACTERISTICS

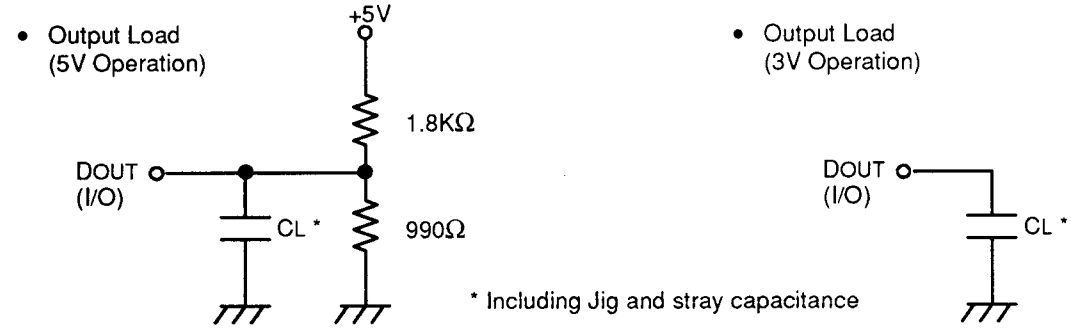
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	5V Operation		3V Operation		Unit
			Min	Max	Min	Max	
Standby Supply Current	CS2 ≤ 0.2V or $\overline{CS1}$ ≥ VCC–0.2V (CS2 ≤ 0.2V or CS2 ≥ VCC–0.2V)	ISB1		0.02		0.01	mA
	$\overline{CS1}$ = VIH or CS2 = VIL	ISB2		1		0.01	mA
Active Supply Current	VIN = VIH or VIL, $\overline{CS1}$ = VIL, CS2 = VIH, IOUT = 0mA	ICC		25		10	mA
Operating Supply Current	Cycle = Min., Duty = 100% IOUT = 0mA	ICC1		60		30	mA
Intput Leakage Current	VIN = 0V to VCC	ILI	–1	1	–1	1	µA
Output Leakage Current	VI/O = 0V to VCC, $\overline{CS1}$ = VIH or CS2 = VIL or $\overline{OE}$ = VIH or $\overline{WE}$ = VIL	ILI/O	–1	1	–1	1	µA
Input High Voltage		VIH	2.2	VCC +0.3	VCC –2.2	VCC +0.3	V
Input Low Voltage		VIL	–0.3*	0.8	–0.3*	0.2	V
Output High Voltage	IOH = –1.0mA (5V Operation) IOH = –0.5mA (3V Operation)	VOH	2.4		VCC –0.5		V
Output Low Voltage	IOL = 2.1mA (5V Operation) IOL = 1.0mA (3V Operation)	VOL		0.4		0.5	V

Note * : –3.0V min. for pulse width less than 20 ns. (VIL min. = –0.3V at DC level.)
: All voltages are referenced to GND.

Parameter		5V Operation	3V Operation
Input Pulse Levels		0.6V to 2.4V	0V to VCC
Input Pulse Rise & Fall Times		5ns (0.8V to 2.2V)	5ns (0.2V to VCC–0.2V)
Timing Reference Levels	Input	VIL=0.8V, VIH=2.2V	VIL=0.2V, VIH=VCC–0.2V
	Output	VOL=0.8V, VOH=2.0V	VOL=1.5V, VOH=1.5V

Fig.2 – AC TEST CONDITIONS



	CL	Parameters Measured
Load I	100pF	except tCLZ, tOLZ, tCHZ, tOHZ, tWLZ and tWHZ
Load II	5pF	tCLZ, tOLZ, tCHZ, tOHZ, tWLZ and tWHZ

AC CHARACTERISTICS

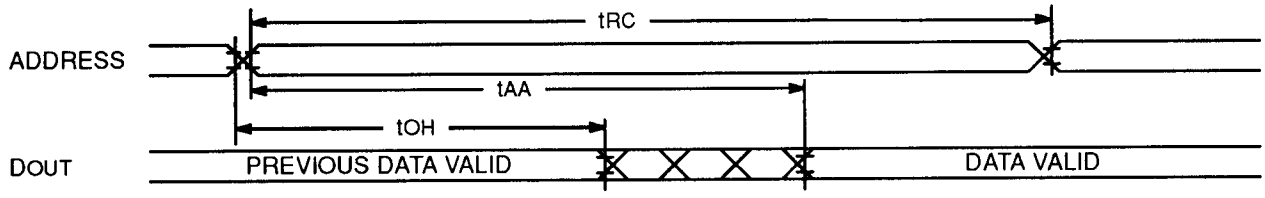
(Recommended operating conditions unless otherwise noted.)

READ CYCLE *1

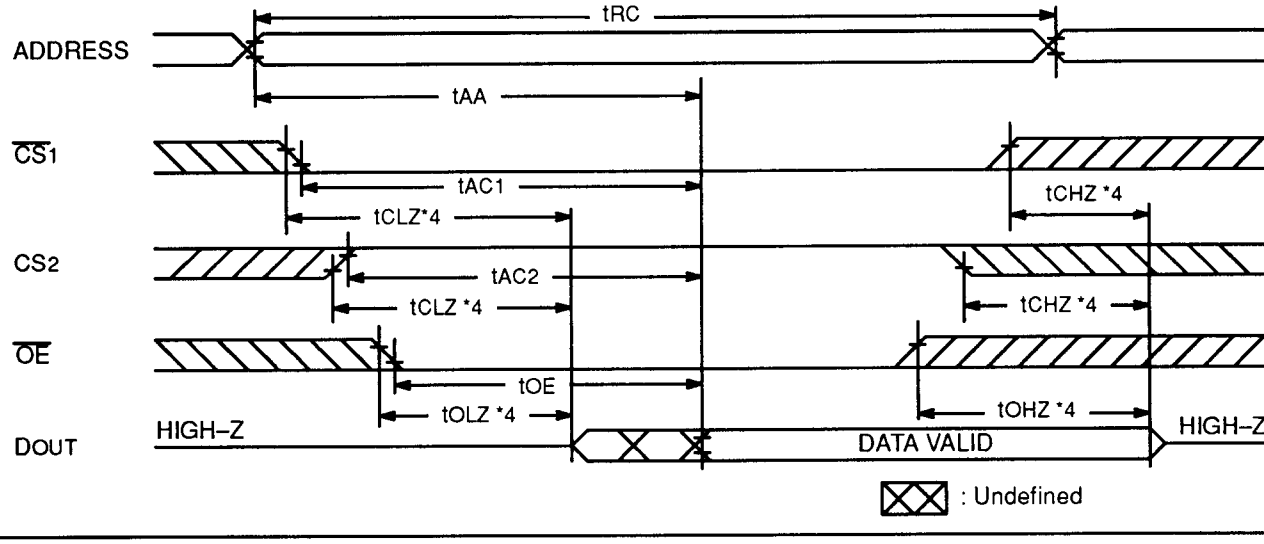
Parameter	Symbol	5V Operation				3V Operation		Unit
		MB8464R-70LL		MB8464R-10LL		MB8464R-70LL /-10LL		
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	70		100		200		ns
Address Access Time *2	tAA		70		100		200	ns
$\overline{CS1}$ Access Time *3	tAC1		70		100		200	ns
CS2 Access Time *3	tAC2		70		100		200	ns
Output Enable to Output Valid	tOE		35		40		80	ns
Output Hold from Address Change	tOH	20		20		20		ns
Chip Select to Output Low–Z *4	tCLZ	10		10		10		ns
Output Enable to Output Low–Z *4	tOLZ	5		5		5		ns
Chip Select to Output High–Z *4	tCHZ		25		35		60	ns
Output Enable to Output High–Z *4	tOHZ		25		35		60	ns

READ CYCLE TIMING DIAGRAM *1

READ CYCLE 1: ADDRESS CONTROLLED *2



READ CYCLE 2: $\overline{CS1}$, CS2 CONTROLLED *3



Notes: *1 $\overline{WE}$ is high for Read Cycle.
*2 Device is continuously selected, $\overline{CS1}$ = $\overline{OE}$ = VIL, CS2 = VIH.
*3 Address valid prior to or coincident with $\overline{CS1}$ transition low, CS2 transition high.
*4 Transition is measured at the point of ±500mV from steady state voltage with load II as specified in Fig. 2.

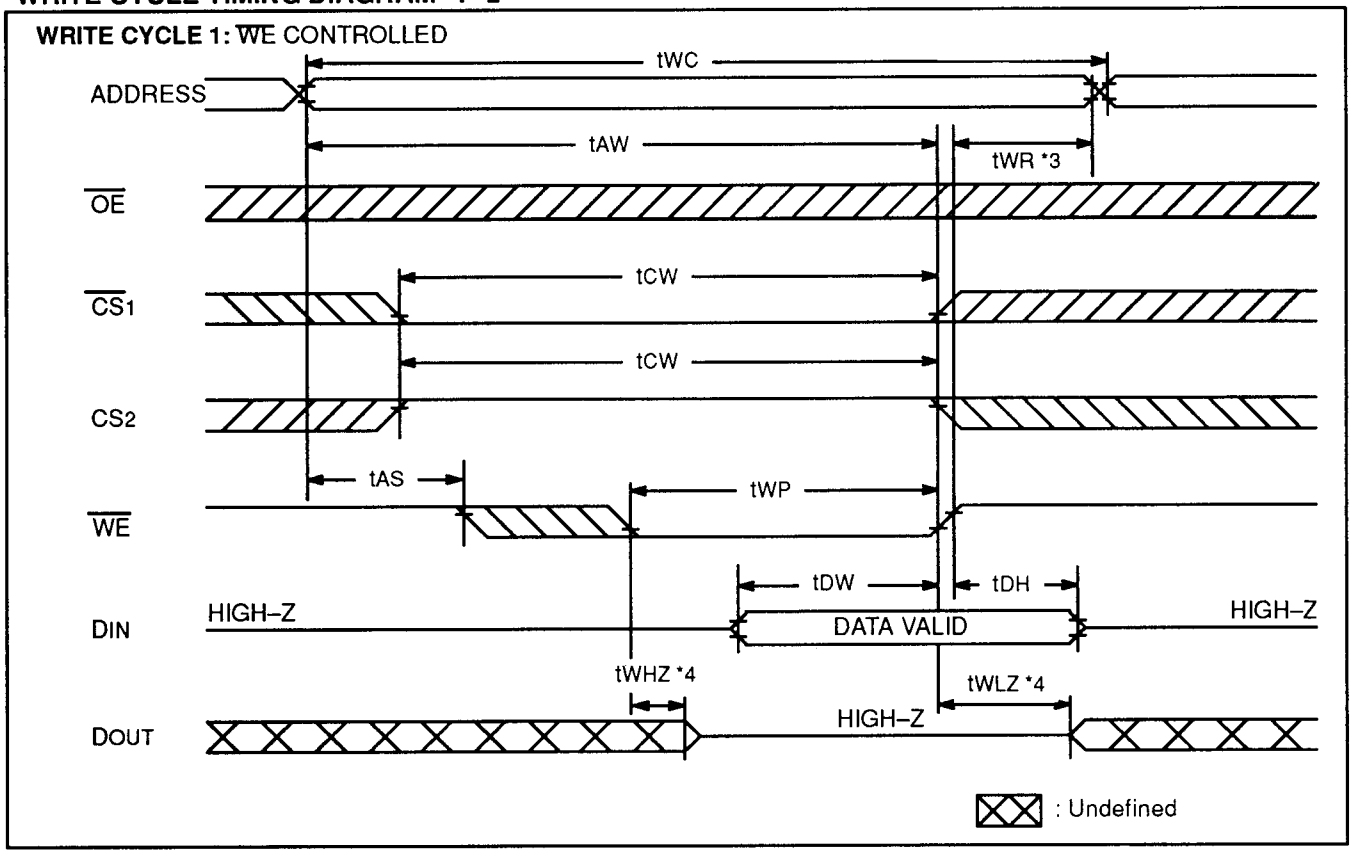
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

WRITE CYCLE *1*2

Parameter	Symbol	5V Operation				3V Operation		Unit
		MB8464R-70LL		MB8464R-10LL		MB8464R-70LL/ -10LL		
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	70		100		200		ns
Address Valid to End of Write	tAW	50		80		120		ns
Chip Select to End of Write	tCW	50		80		120		ns
Data Valid to End of Write	tDW	25		35		60		ns
Data Hold Time	tDH	0		0		0		ns
Write Pulse Width	tWP	50		60		80		ns
Address Setup Time	tAS	0		0		0		ns
Write Recovery Time *3	tWR	5		5		10		ns
Write Enable to Output Low–Z *4	tWLZ	5		5		5		ns
Write Enable to Output High–Z *4	tWHZ		25		35		60	ns

WRITE CYCLE TIMING DIAGRAM *1 *2

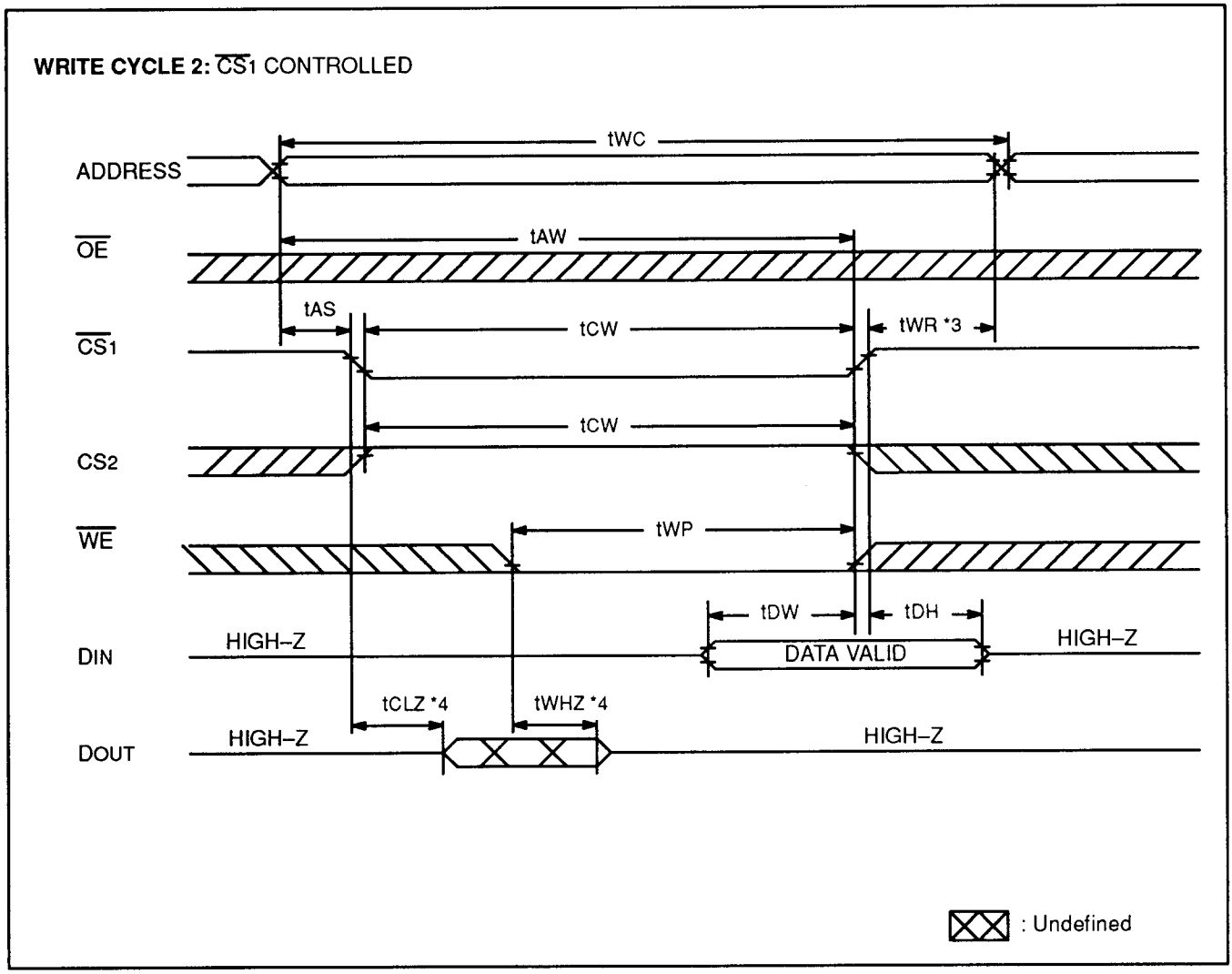


Notes: *1 If $\overline{OE}$, $\overline{CS1}$ and CS2 are in the READ Mode during this period, the I/O pins are in the output state and the input signals of opposite phase to the outputs must not be applied.
*2 If $\overline{CS1}$ goes high or CS2 goes low simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 tWR is defined from the end point of WRITE Mode.
*4 Transition is measured at the point of ±500mV from steady state voltage with Load II as specified in Fig. 2.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

WRITE CYCLE TIMING DIAGRAM *1 *2



Notes: *1 If $\overline{OE}$, $\overline{CS1}$ and CS2 are in the READ Mode during this period, the I/O pins are in the output state and the input signals of opposite phase to the outputs must not be applied.

*2 If CS1 goes high or CS2 goes low simultaneously with WE high, the output remains in high impedance state.

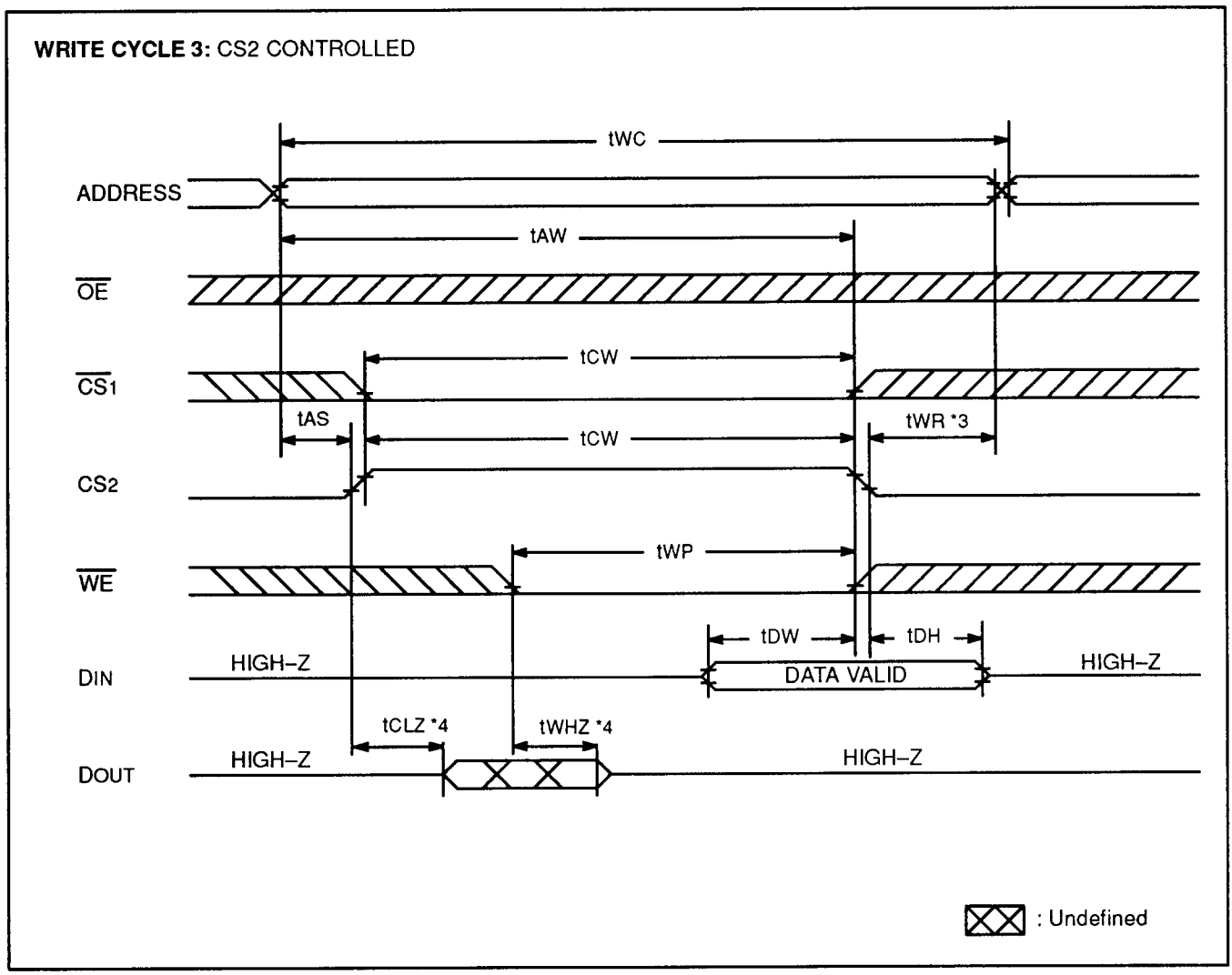
*3 tWR is defined from the end point of WRITE Mode.

*4 Transition is measured at the point of ±500mV from steady state voltage with Load II as specified in Fig. 2.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

WRITE CYCLE TIMING DIAGRAM *1 *2



Notes: *1 If $\overline{OE}$, $\overline{CS1}$ and CS2 are in the READ Mode during this period, the I/O pins are in the output state and the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{CS1}$ goes high or CS2 goes low simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*3 tWR is defined from the end point of WRITE Mode.

*4 Transition is measured at the point of ±500mV from steady state voltage with Load II as specified in Fig. 2.

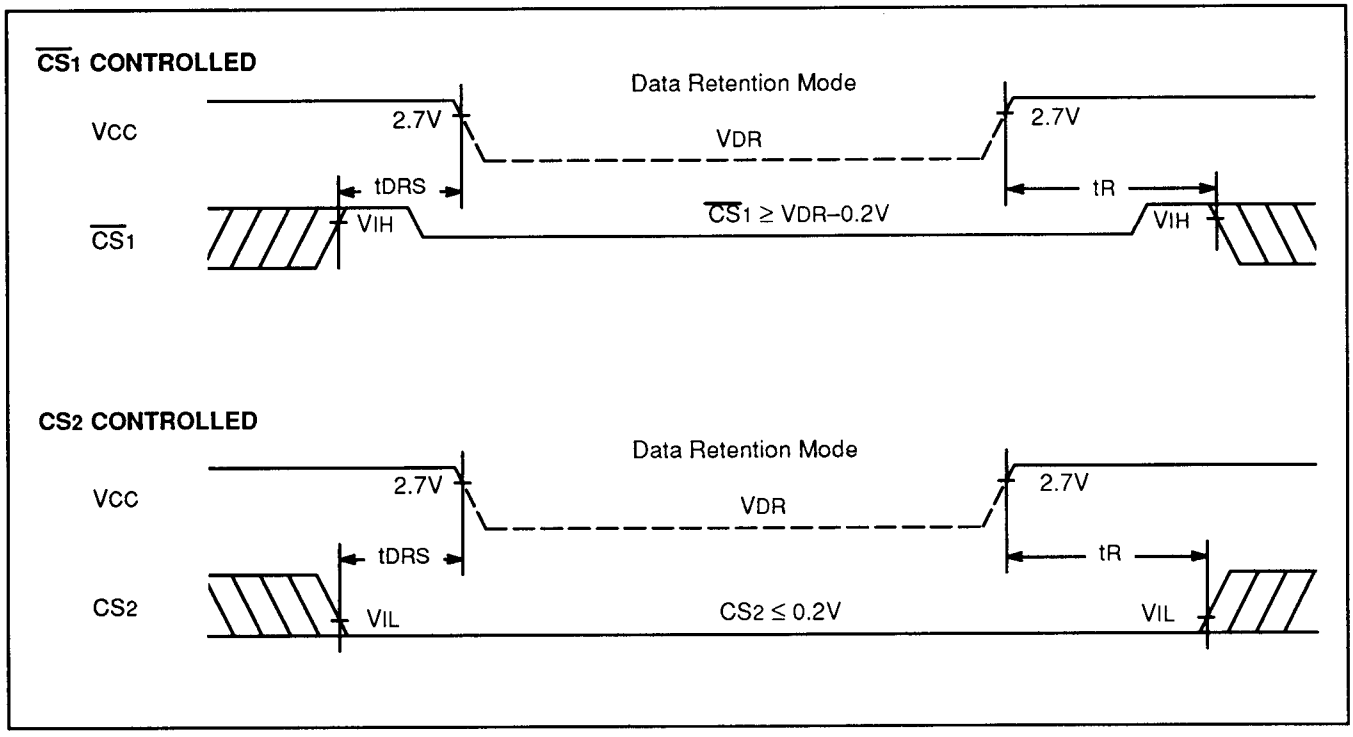
DATA RETENTION CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Data Retention Supply Voltage *1	VDR	2.0		5.5	V
Data Retention SupplyCurrent *1	IDR		0.0006	0.01 *2	mA
Data Retention Setup Time	tDRS	0			ns
Operation Recovery Time	tR	5			ms

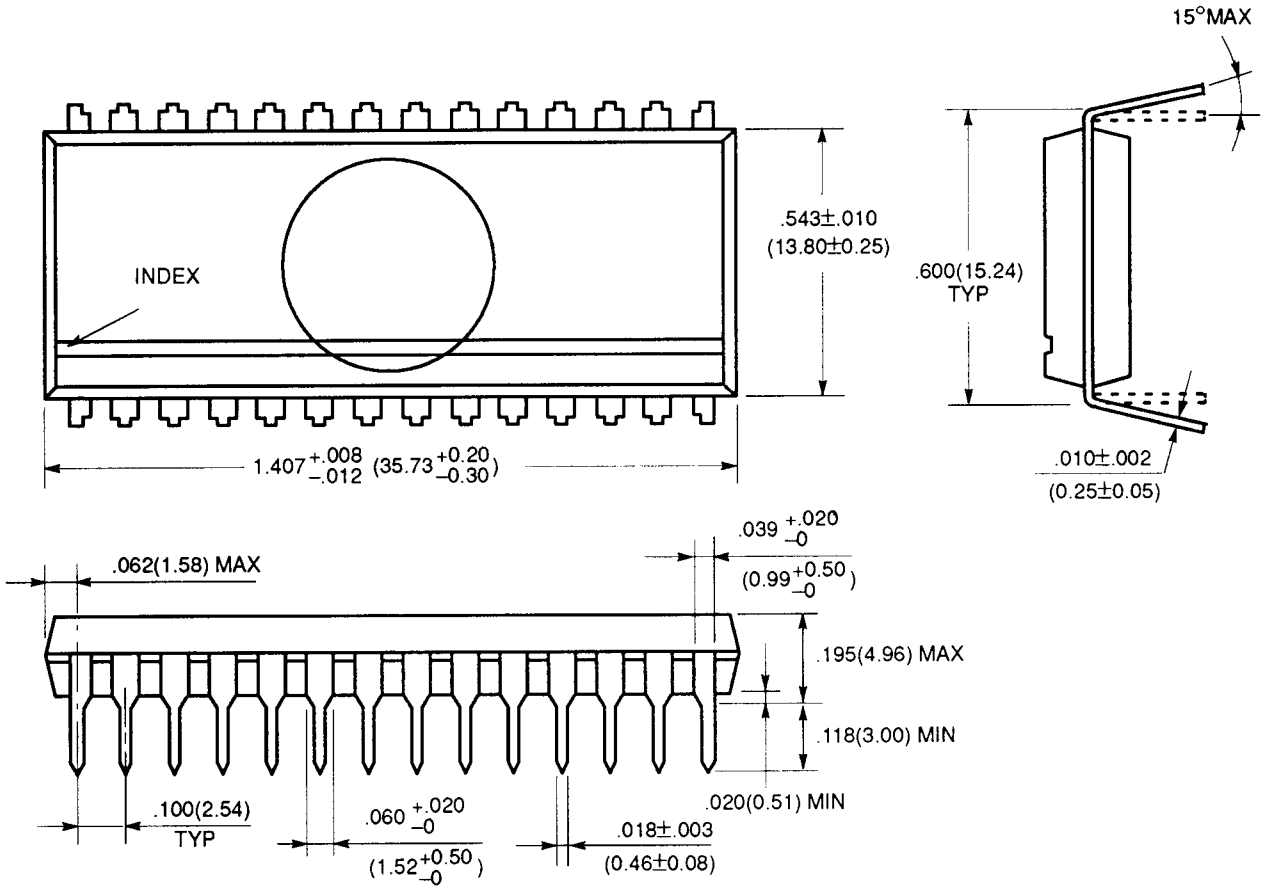
Notes: *1 $V_{CC} = V_{DR} = 3.0V$
$\overline{CS_1} \geq V_{DR}-0.2V$, $CS_2 \geq V_{DR}-0.2V$ or $CS_2 \leq 0.2V$ (at $\overline{CS_1}$ CONTROLLED)
$CS_2 \leq 0.2V$ (at CS_2 CONTROLLED)
*2 $I_{DR} = 1\mu A$ max. at $V_{DR} = 3V$, $T_A = 0°C$ to $+40°C$

DATA RETENTION TIMING



PACKAGE DIMENSIONS
(Suffix: P)

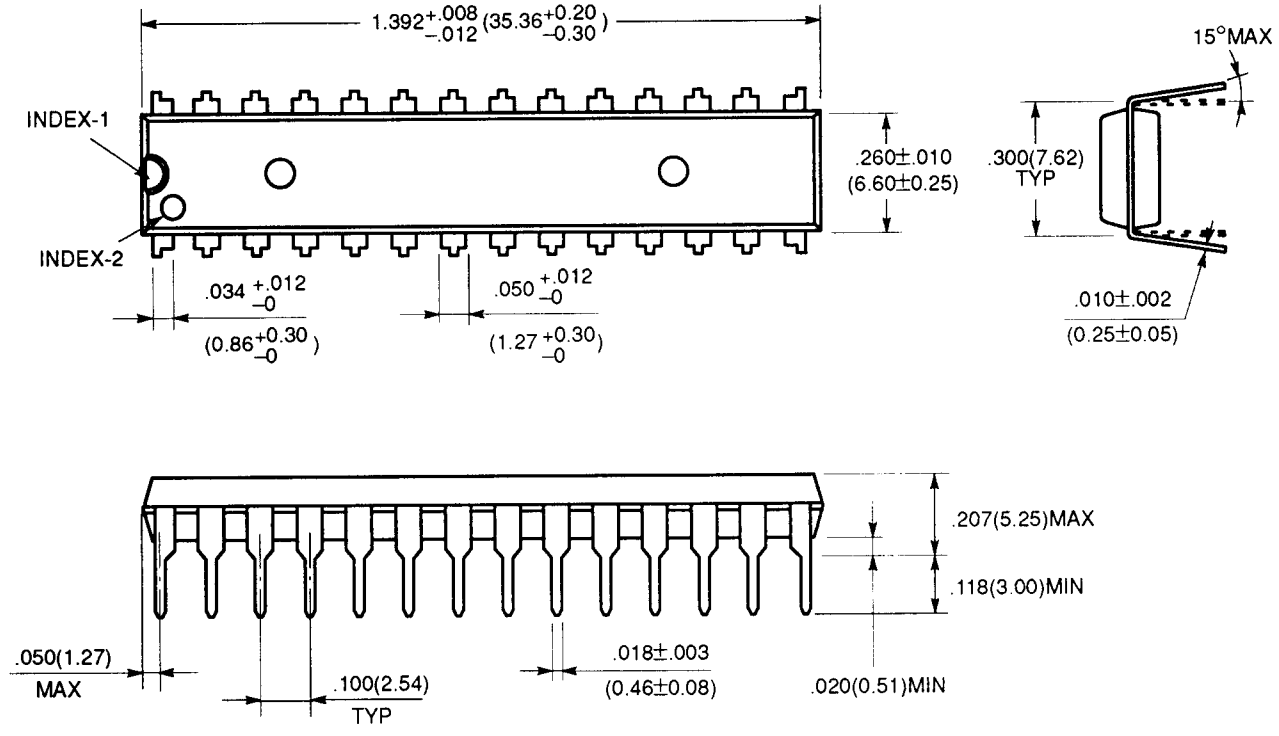
28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-28P-M02)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)
(Suffix: P–SK)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-28P-M04)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)
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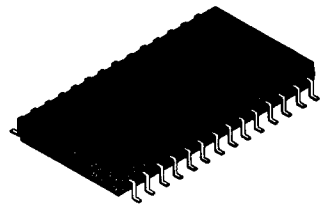
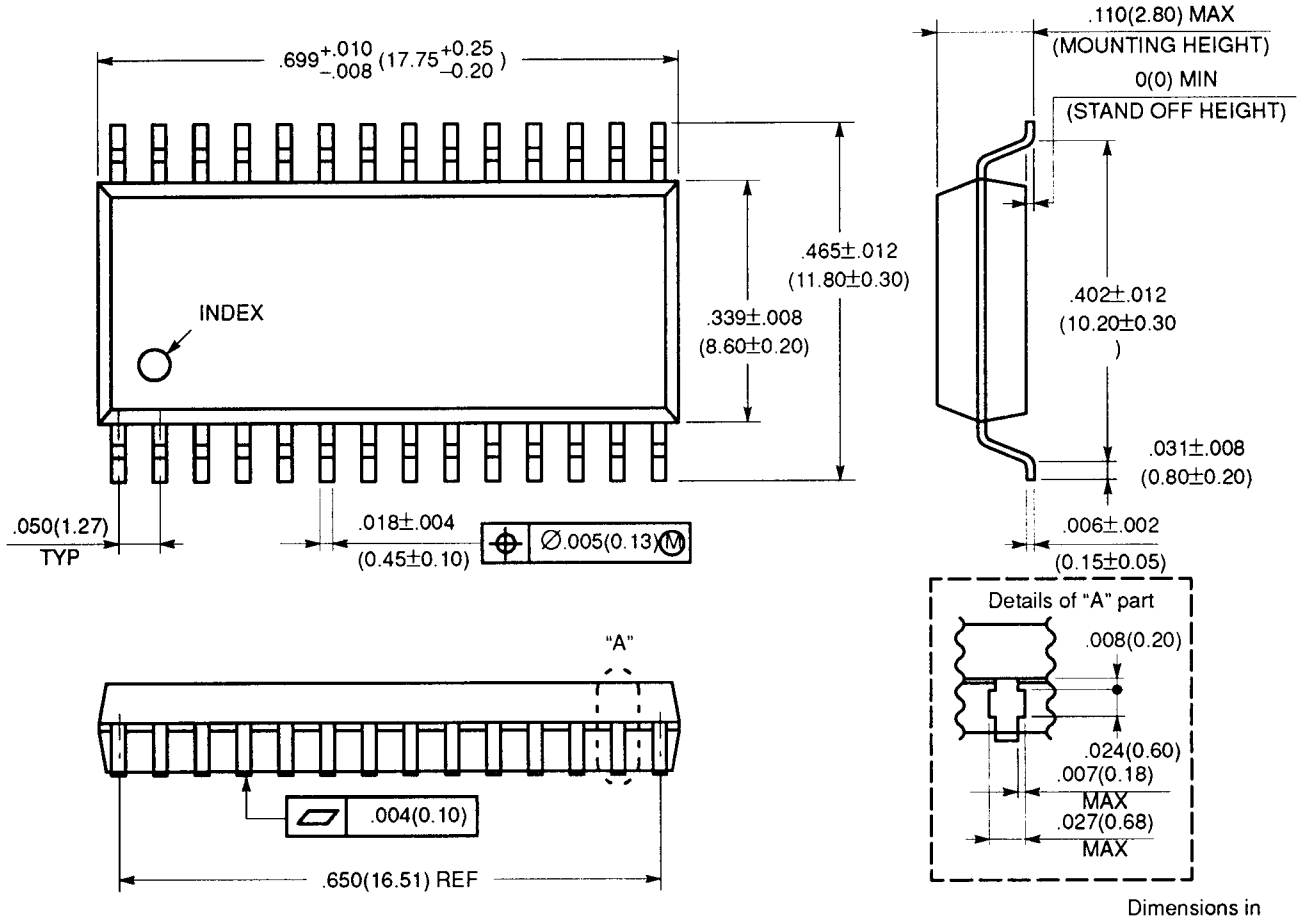


FPT-28P-M02

28-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-28P-M02)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

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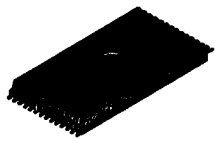
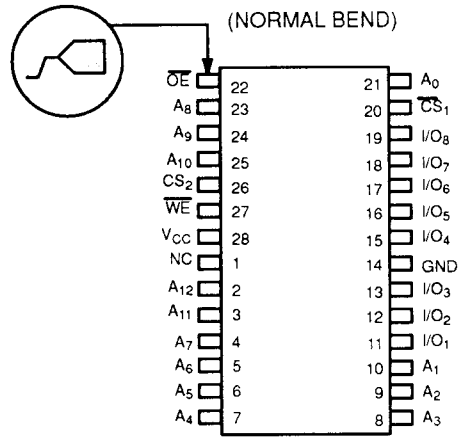


FPT-28P-M03

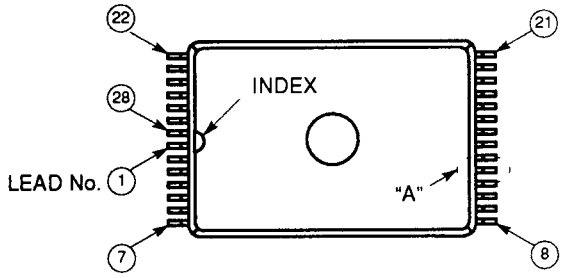
PIN ASSIGNMENT

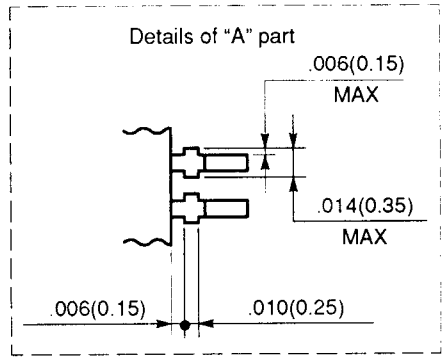
(NORMAL BEND)

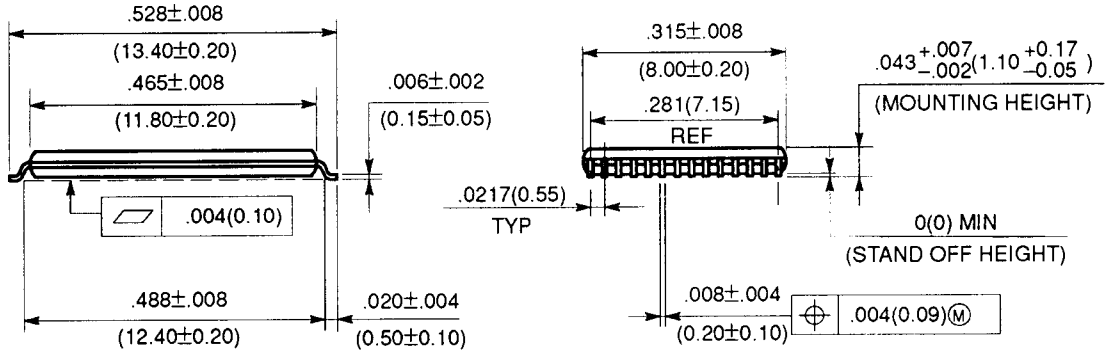


TOP VIEW

28-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-28P-M03)



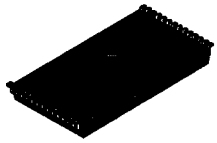




Dimensions in inches (millimeters)

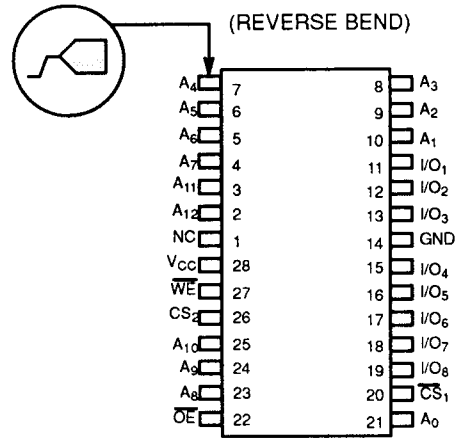
PACKAGE DIMENSIONS (Continued)

(Suffix: PFTR)



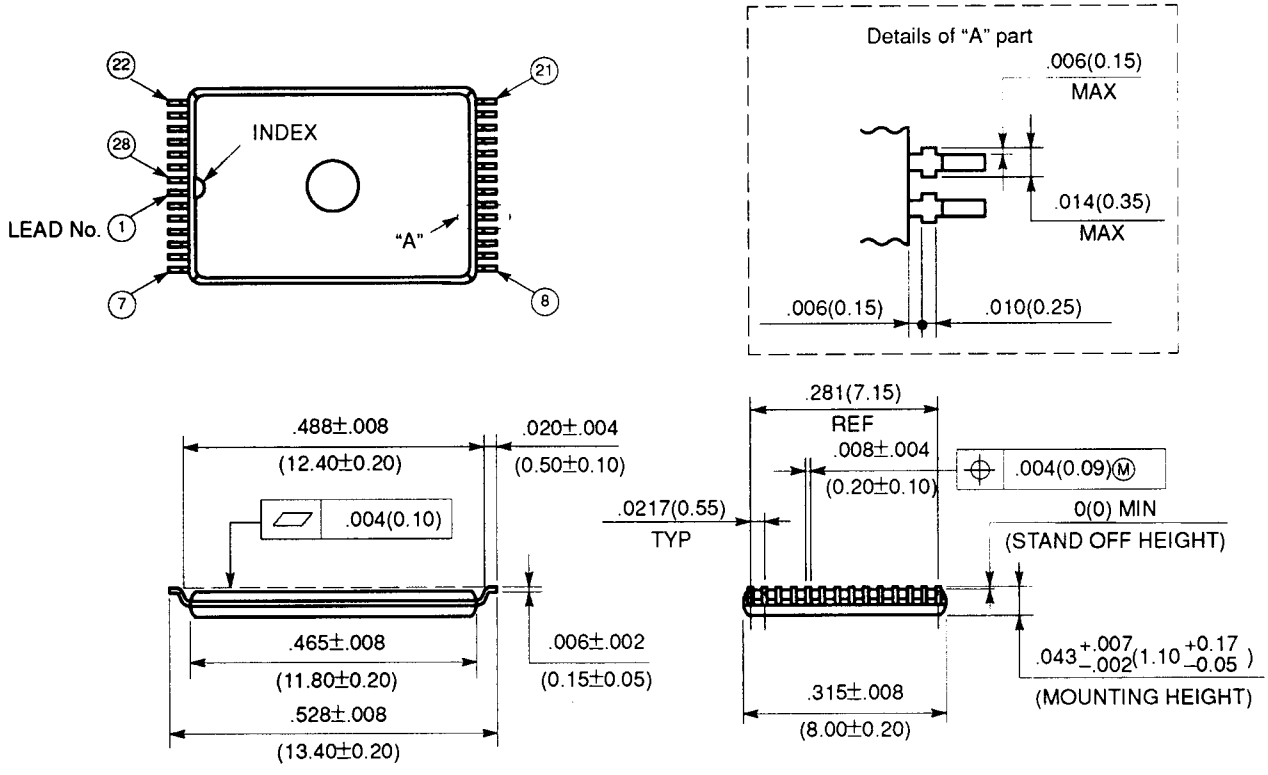
FPT-28P-M04

PIN ASSIGNMENT
(REVERSE BEND)



TOP VIEW

28-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-28P-M04)



Dimensions in
inches (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications. Complete Information sufficient for construction purposes is not necessarily given.

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