Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS INTERFACE REGISTERS

IDT54/74FCT821/2821AT/BT/CT/DT
IDT54/74FCT823/2823AT/BT/CT/DT
IDT54/74FCT825/2825AT/BT/CT

FEATURES:

- **Common features:**
  - A, B, C and D speed grades
  - Low input and output leakage ≤1μA (max.)
  - CMOS power levels
  - True TTL input and output compatibility
    - V_{OH} = 3.3V (typ.)
    - V_{OL} = 0.3V (typ.)
  - Meets or exceeds JEDEC standard 18 specifications
  - Product available in Radiation Tolerant and Radiation Enhanced versions
  - Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
  - Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages
- **Features for FCT821/823/825T:**
  - High drive outputs (-15mA I_{OH}, 48mA I_{OL})
  - Power off disable outputs permit "live insertion"
- **Features for FCT2821/2823/2825T:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise

DESCRIPTION:

The IDT54/74FCT8xx series is built using an advanced dual metal CMOS technology. The IDT54/74FCT820 series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT821/2821AT/BT/CT/DT are buffered, 10-bit wide versions of the popular '374 function. The IDT54/74FCT823/2823AT/BT/CT/DT are 9-bit wide buffered registers with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high-performance microprogrammed systems. The IDT54/74FCT825/2825AT/BT/CT are 8-bit buffered registers with all the '823 controls plus multiple enables ($\overline{OE}1$, $\overline{OE}2$, $\overline{OE}3$) to allow multi-user control of the interface, e.g., $\overline{CS}$, DMA and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

The IDT54/74FCT8xx high-performance interface family can drive large capacitive loads, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

The IDT54/74FCT2821AT/BT/CT/DT, IDT54/74FCT2823AT/BT/CT/DT, IDT54/74FCT2825AT/BT/CT have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. The IDT54/74FCT2xxxT parts are plug-in replacements for IDT54/74FCTxxxT parts.

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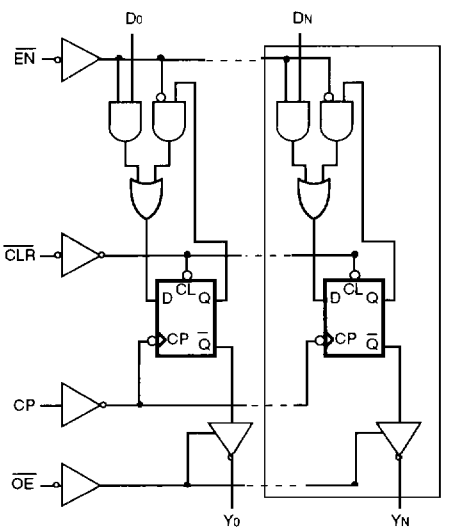
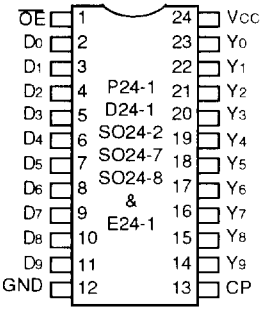
FUNCTIONAL BLOCK DIAGRAM



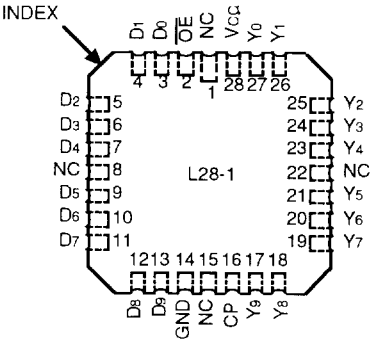
2567 drw 01

PIN CONFIGURATIONS

FCT821/2821T 10-BIT REGISTER



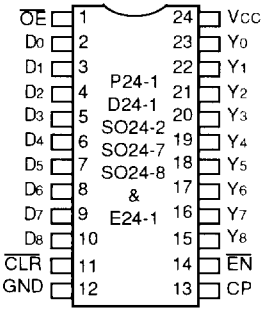
DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW



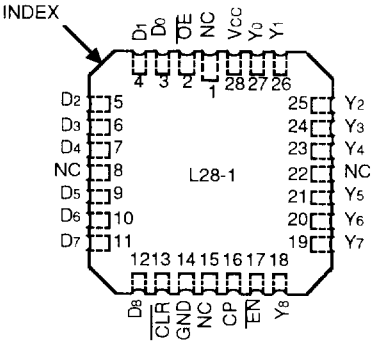
2567 drw 02

LCC
TOP VIEW

FCT823/2823T 9-BIT REGISTER



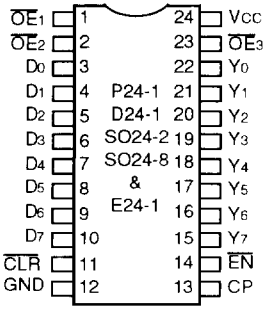
DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW



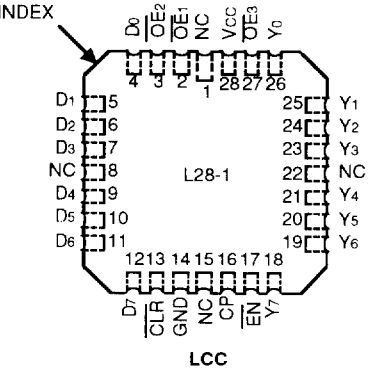
2567 drw 03

LCC
TOP VIEW

FCT825/2825T 8-BIT REGISTER



DIP/SOIC/QSOP/CERPACK
TOP VIEW



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LCC
TOP VIEW

PIN DESCRIPTION

Names	I/O	Description
DI	I	The D flip-flop data inputs.
$\overline{CLR}$	I	When the clear input is LOW and $\overline{OE}$ is LOW, the QI outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
YI	O	The register 3-state outputs.
$\overline{EN}$	I	Clock Enable. When the clock enable is LOW, data on the D I input is transferred to the QI output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the QI outputs do not change state, regardless of the data or clock input transitions.
$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the Y I outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the YI outputs.

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FUNCTION TABLE[1]

Inputs					Internal/ Outputs		
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	DI	CP	QI	YI	Function
H	H	L	L	↑	L	Z	High Z
H	H	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

NOTE:
2567 tbl 02

1. H = HIGH
   L = LOW
   X = Don't Care
   NC = No Change
   ↑ = LOW-to-HIGH Transition
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
2567 lnk 06

1. This parameter is measured at characterization but not tested.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]		V_I = 0.5V	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[4]		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = −18mA		—	−0.7	−1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		−60	−120	−225	mA
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.01	1	mA

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OUTPUT DRIVE CHARACTERISTICS FOR FCT821/823/825T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −6mA MIL. I_{OH} = −8mA COM'L.	2.4	3.3	—	V
			I_{OH} = −12mA MIL. I_{OH} = −15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

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OUTPUT DRIVE CHARACTERISTICS FOR FCT2821/2823/2825T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		−60	−115	−150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −16mA MIL. I_{OH} = −24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

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NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = −55°C.
5. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]			Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]			—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = $\overline{EN}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	0.15	0.25	mA/ MHz
				FCT2xxxT	—	0.06	0.12	
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle $\overline{OE}$ = $\overline{EN}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	1.5	3.5	mA
				FCT2xxxT	—	0.6	2.2	
			V_{IN} = 3.4 V_{IN} = GND	FCTxxxT	—	2.0	5.5	
				FCT2xxxT		1.1	4.2	
		V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle $\overline{OE}$ = $\overline{EN}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	3.8	7.3[5]	
				FCT2xxxT	—	1.5	4.0[5]	
			V_{IN} = 3.4 V_{IN} = GND	FCTxxxT	—	6.0	16.3[5]	
				FCT2xxxT	—	3.8	13.0[5]	

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NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT821/823/825AT FCT2821/2823/2825AT				FCT821/823/825BT FCT2821/2823/2825BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to Yi ($\overline{OE}$ = LOW)	C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	11.5	1.5	7.5	1.5	8.5	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	20.0	1.5	20.0	1.5	15.0	1.5	16.0	
t_{SU}	Set-up Time HIGH or LOW Di to CP	C_L = 50pF R_L = 500Ω	4.0	—	4.0	—	3.0	—	3.0	—	ns
t_H	Hold Time HIGH or LOW Di to CP		2.0	—	2.0	—	1.5	—	1.5	—	ns
t_{SU}	Set-up Time HIGH or LOW $\overline{EN}$ to CP		4.0	—	4.0	—	3.0	—	3.0	—	ns
t_H	Hold Time HIGH or LOW $\overline{EN}$ to CP		2.0	—	2.0	—	0	—	0	—	ns
t_{PHL}	Propagation Delay, $\overline{CLR}$ to Yi		1.5	14.0	1.5	15.0	1.5	9.0	1.5	9.5	ns
t_{REM}	Recovery Time $\overline{CLR}$ to CP		6.0	—	7.0	—	6.0	—	6.0	—	ns
t_W	Clock Pulse Width HIGH or LOW		7.0	—	7.0	—	6.0	—	6.0	—	ns
t_W	$\overline{CLR}$ Pulse Width LOW		6.0	—	7.0	—	6.0	—	6.0	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Yi	C_L = 50pF R_L = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	23.0	1.5	25.0	1.5	15.0	1.5	16.0	
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Yi	C_L = 5pF[4] R_L = 500Ω	1.5	7.0	1.5	8.0	1.5	6.5	1.5	7.0	ns
		C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	9.0	1.5	7.5	1.5	8.0	

NOTES:

2567 tbl 11

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. This condition is guaranteed but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			FCT821/823/825CT FCT2821/2823/2825CT				FCT821DT FCT2821DT		FCT823DT FCT2823DT		
			Com'l.		Mil.		Com'l.		Com'l.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
tPLH tPHL	Propagation Delay CP to Yi ($\overline{OE}$ = LOW)	C_L = 50pF R_L = 500Ω	1.5	6.0	1.5	7.0	1.5	4.2	1.5	5.0	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	12.5	1.5	13.5	1.5	8.0	1.5	8.5	
tSU	Set-up Time HIGH or LOW Di to CP	C_L = 50pF R_L = 500Ω	3.0	—	3.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW Di to CP		1.5	—	1.5	—	1.0	—	1.0	—	ns
tSU	Set-up Time HIGH or LOW $\overline{EN}$ to CP		3.0	—	3.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW $\overline{EN}$ to CP		0	—	0	—	0	—	0	—	ns
tPHL	Propagation Delay, $\overline{CLR}$ to Yi		1.5	8.0	1.5	8.5	1.5	5.0	1.5	5.0	ns
tREM	Recovery Time $\overline{CLR}$ to CP		6.0	—	6.0	—	3.0	—	3.0	—	ns
tW	Clock Pulse Width HIGH or LOW[3]		6.0	—	6.0	—	3.0	—	3.0	—	ns
tW	$\overline{CLR}$ Pulse Width LOW[3]		6.0	—	6.0	—	3.0	—	3.0	—	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to Yi	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	8.0	1.5	4.8	1.5	4.8	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	12.5	1.5	13.5	1.5	9.0	1.5	9.0	
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to Yi	C_L = 5pF[4] R_L = 500Ω	1.5	6.0	1.5	6.0	1.5	4.0	1.5	4.0	ns
		C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	6.5	1.5	4.0	1.5	4.0	

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. This condition is guaranteed but not tested.

2567 tbl 12

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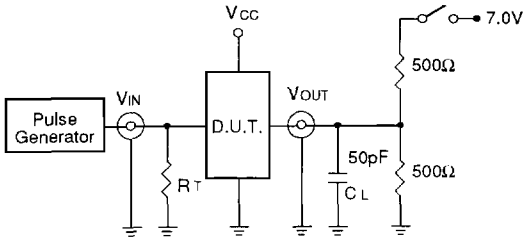
TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2567 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

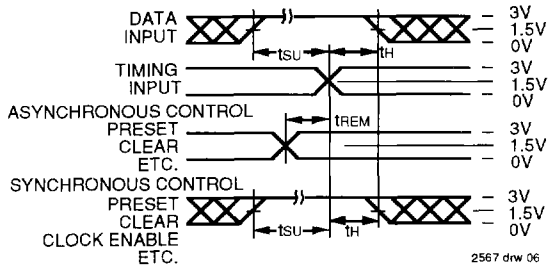
2567 lnk 13

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

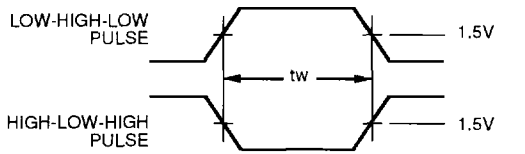
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



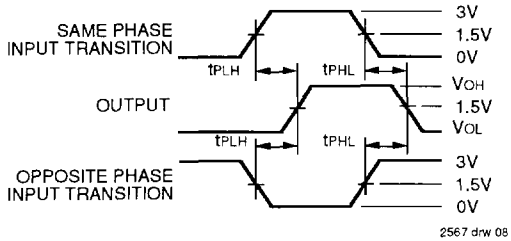
2567 drw 06

PULSE WIDTH



2567 drw 07

PROPAGATION DELAY



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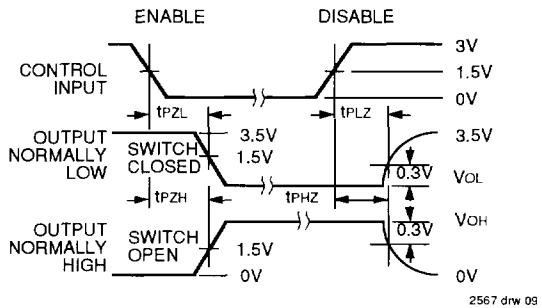
ENABLE AND DISABLE TIMES



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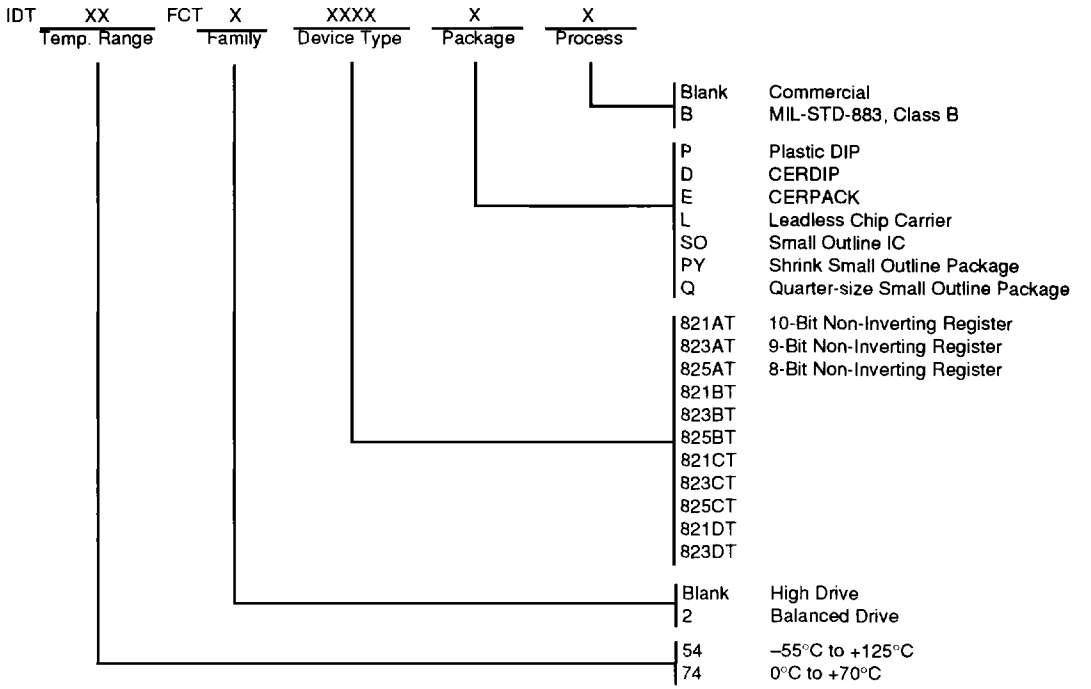
NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



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