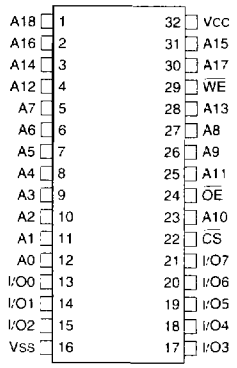
512Kx8 MONOLITHIC SRAM, SMD 5962-95613 *PRELIMINARY**

EVOLUTIONARY PINOUT

32 DIP
32 CSOJ (DE)

TOP VIEW



PIN DESCRIPTION

A_{0-18}	Address Inputs
I/O_{0-7}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	+5.0V Power
V_{SS}	Ground

FEATURES

- Access Times 70, 85, 100, 120nS
- MIL-STD-883 Compliant Devices Available
- Evolutionary, Corner Power/Ground Pinout JEDEC Approved
  - 32 pin Ceramic DIP (Package 300)
  - 32 lead Ceramic SOJ (Package 101)
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs

* *This data sheet describes a product under development, not fully characterized and is subject to change without notice*

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	Vcc+0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	TA	-55	+125	°C

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C_{IN}	V_{IN} = 0V, f = 1.0MHz	20	pF
Output capicitance	C_{OUT}	V_{OUT} = 0V, f = 1.0MHz	20	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		50	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		1	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA, V_{CC} = 4.5		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA, V_{CC} = 4.5	2.4		V

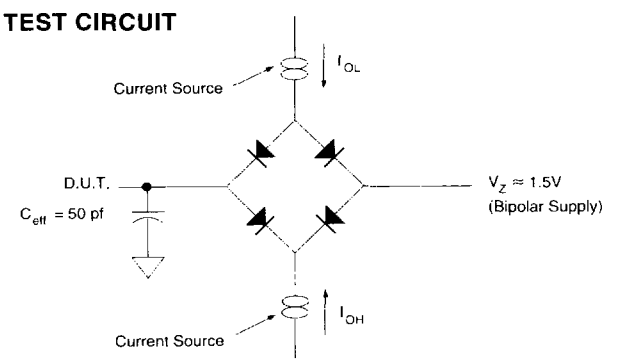
NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

DATA RETENTION CHARACTERISTICS

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data Retention Supply Voltage	V_{DR}	$\overline{CS}$ V_{CC} -0.2V	2.0		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		0.1	0.4	mA

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V
I_{OL} & I_{OH} programmable from 0 to 16mA
Tester Impedance Z_0 = 75 Ω
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit
ATE tester includes jig capacitance

AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter Read Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		85		100		120		nS
Address Access Time	t_{AA}		70		85		100		120	nS
Output Hold from Address Change	t_{OH}	5		5		5		5		nS
Chip Select Access Time	t_{ACS}		70		85		100		120	nS
Output Enable to Output Valid	t_{OE}		35		40		50		60	nS
Chip Select to Output in Low Z	t_{CLZ}[1]	10		10		10		10		nS
Output Enable to Output in Low Z	t_{OLZ}[1]	5		5		5		5		nS
Chip Disable to Output in High Z	t_{CHZ}[1]		25		25		35		35	nS
Output Disable to Output in High Z	t_{OHZ}[1]		25		25		35		35	nS

1. This parameter is guaranteed by design but not tested.

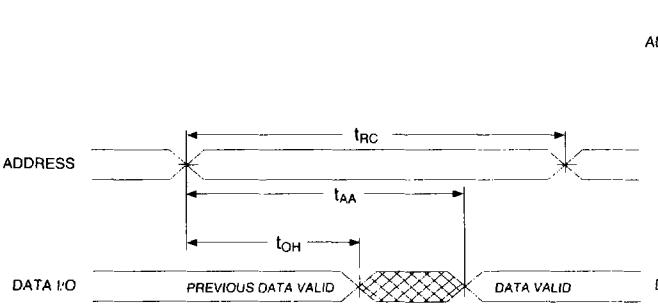
AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

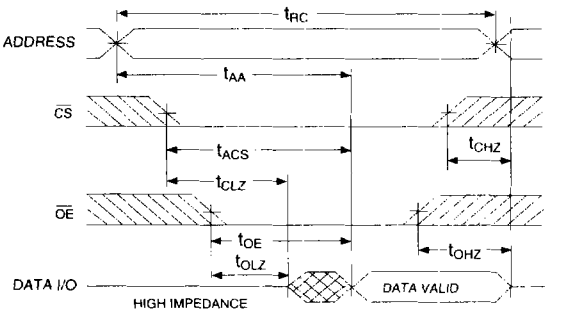
Parameter Write Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		85		100		120		nS
Chip Select to End of Write	t_{CW}	60		75		80		100		nS
Address Valid to End of Write	t_{AW}	60		75		80		100		nS
Data Valid to End of Write	t_{DW}	30		30		40		40		nS
Write Pulse Width	t_{WP}	50		50		60		60		nS
Address Setup Time	t_{AS}	0		0		0		0		nS
Address Hold Time	t_{AH}	5		5		5		5		nS
Output Active from End of Write	t_{OW}[1]	5		5		5		5		nS
Write Enable to Output in High Z	t_{WHZ}[1]		25		25		35		35	nS
Data Hold from Write Time	t_{DH}	0		0		0		0		nS

1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM - READ CYCLE

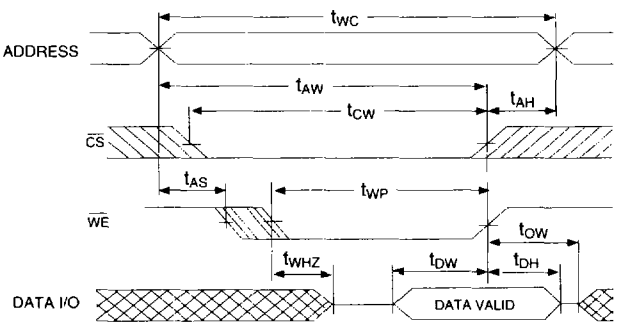


READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



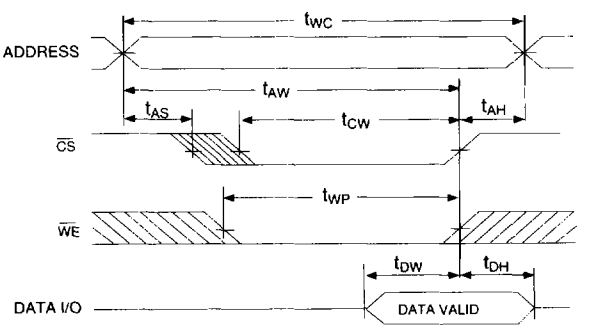
READ CYCLE 2 ($\overline{WE}$ = V_{IH})

WRITE CYCLE - $\overline{WE}$ CONTROLLED



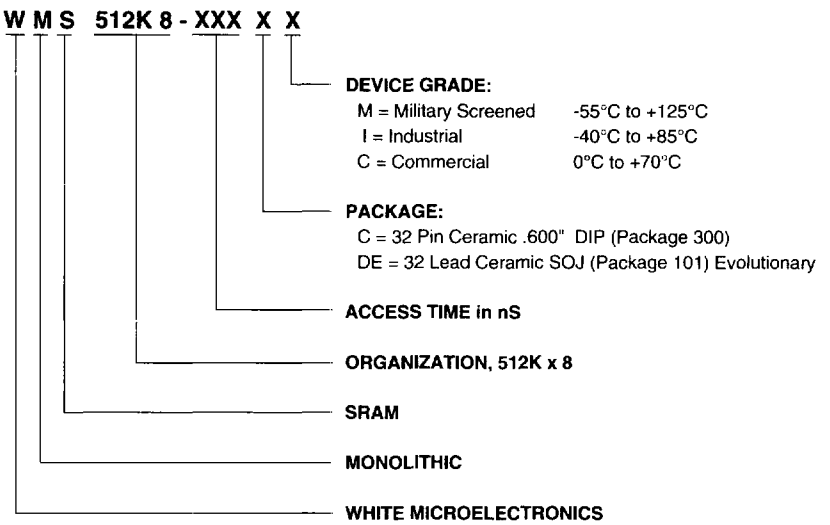
WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

WRITE CYCLE - $\overline{CS}$ CONTROLLED



WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

ORDERING INFORMATION



DEVICE TYPE	SPEED	PACKAGE	SMD NO.
512K x 8 SRAM Monolithic	120nS	32 pin DIP (C)	5962-95613 01HYX
512K x 8 SRAM Monolithic	**100nS**	**32 pin DIP (C)**	**5962-95613 02HYX**
512K x 8 SRAM Monolithic	85nS	32 pin DIP (C)	5962-95613 03HYX
512K x 8 SRAM Monolithic	70nS	32 pin DIP (C)	5962-95613 04HYX
512K x 8 SRAM Monolithic	120nS	32 lead SOJ Evol (DE)	5962-95613 01HTX
512K x 8 SRAM Monolithic	**100nS**	**32 lead SOJ Evol (DE)**	**5962-95613 02HTX**
512K x 8 SRAM Monolithic	85nS	32 lead SOJ Evol (DE)	5962-95613 03HTX
512K x 8 SRAM Monolithic	70nS	32 lead SOJ Evol (DE)	5962-95613 04HTX